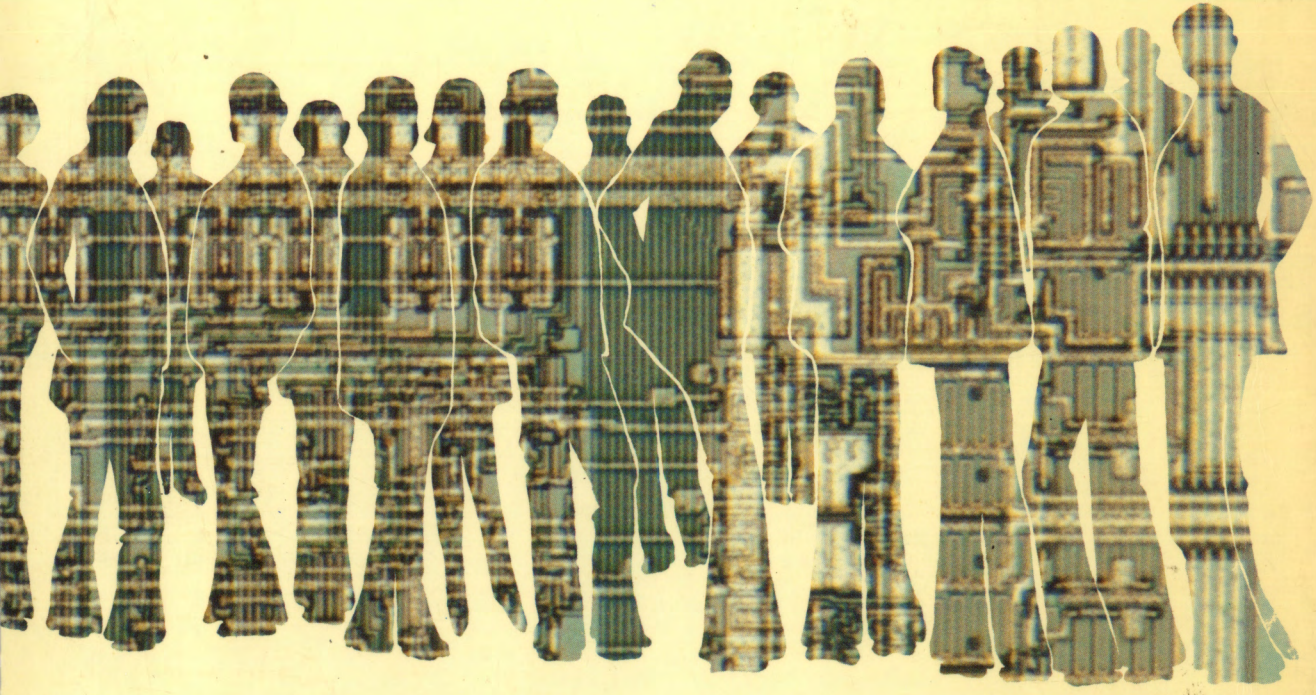
the european consumer selection



MOTOROLA Semiconductors

the european consumer selection

Printed in Switzerland — 230/K77/15.

Introduction

Since the publication of the previous European Consumer Device Data-Book in 1974 the face of consumer electronics has changed considerably. Innovation and technological advancement on both sides of the industry has created the need for new and more sophisticated devices.

The devices within these pages have been especially selected for European Consumer Applications, matching cost effectiveness with performance and reliability.

The data is set out in product groups with the accent on ease of access. An alpha-numeric list of devices precedes each section and is listed by application or device sub-group. In addition, an alpha-numeric list of all devices in the data book is to be found in Section 1. Mechanical data is to be found in Section 2 and includes outline package dimensions as well as a case cross reference guide for JEDEC/MOTOROLA case numbers.

The increasing number of new devices facing the design engineer makes the task of selection extremely difficult and time consuming. We hope that this volume will help to alleviate this problem. Of course, the devices listed here represent only a small part of the Motorola product range and in the event that you are unable to find the device to meet your particular application, please consult the comprehensive Motorola Data Library or your nearest Motorola Sales Office. A list of Motorola Sales Offices and Franchised Distributors is to be found in Section 10.

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Registered case number cross reference

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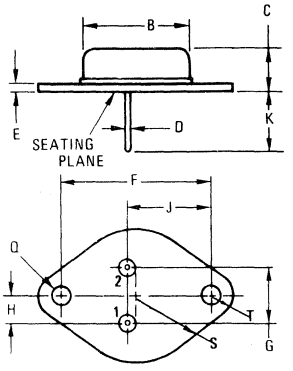
Case outline dimensions

CASE 1-03 (TO-3)

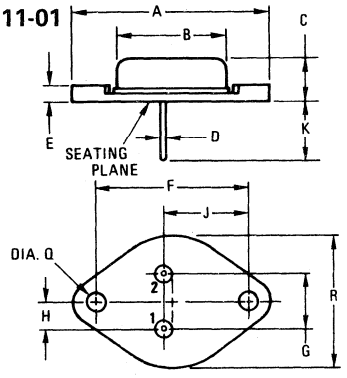
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE:COLLECTOR
STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE-EMITTER



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 11-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

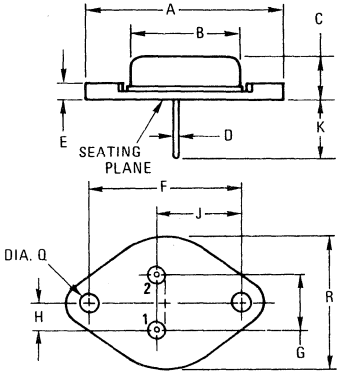
Collector connected to case.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

CASE 11-03



DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	39.37	—	1.550
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

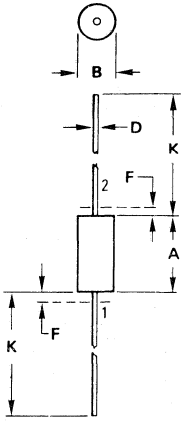
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

Collector connected to case

CASE 17-02

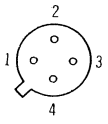


STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.38	8.89	0.330	0.350
B	3.30	3.68	0.130	0.145
D	0.94	1.09	0.037	0.043
F	–	1.27	–	0.050
K	25.40	31.75	1.000	1.250

NOTE:
1. LEAD DIAMETER & FINISH NOT CONTROLLED WITHIN DIM "F".

CASE 20-03 (TO-72)



STYLE 1
PIN 1. SOURCE
2. DRAIN
3. GATE
4. CASE LEAD

STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

STYLE 3
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE LEAD

STYLE 4
PIN 1. SOURCE
2. GATE
3. DRAIN
4. GATE 2 – SUBSTRATE AND CASE

STYLE 5
PIN 1. SOURCE
2. GATE 1
3. DRAIN
4. CASE

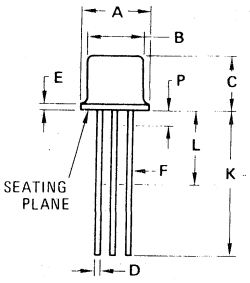
STYLE 6
PIN 1. DRAIN
2. SOURCE AND SUBSTRATE
3. GATE
4. SOURCE AND SUBSTRATE

STYLE 7
PIN 1. DRAIN
2. SOURCE
3. GATE
4. CASE AND SUBSTRATE

STYLE 8
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR
4. EMITTER 1 BASE 2

STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

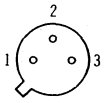
STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 22A-01



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. SOURCE,SUBSTRATE AND CASE
2. GATE
3. DRAIN

STYLE 3:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE &CASE

STYLE 5:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

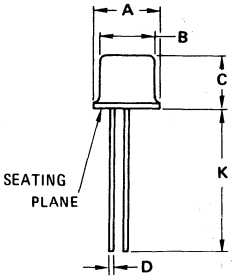
STYLE 7:
PIN 1. ANODE
2. BASE
3. CATHODE

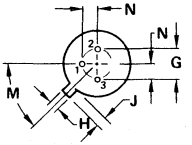
STYLE 8:
PIN 1. GATE
2. ANODE 1
3. ANODE 2

STYLE 9:
PIN 1. ANODE 2
2. ANODE 1
3. GATE (CONNECTED TO CASE)

STYLE 10:
PIN 1. BASE
2. EMITTER
3. BASE

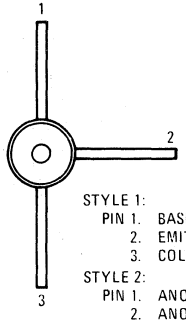
STYLE 11:
PIN 1. DRAIN
2. GATE
3. SOURCE, SUBSTRATE





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 28-01



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE 2
2. ANODE 1
3. CATHODE

STYLE 3:
PIN 1. CATHODE 2
2. CATHODE 1
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. COMMON CATHODE ANODE

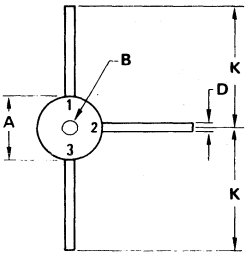
STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

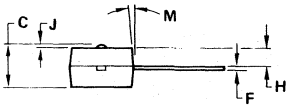
STYLE 6:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 7:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 8:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 9:
PIN 1. SOURCE
2. GATE
3. DRAIN





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.98	2.34	0.078	0.092
B	0.38	0.64	0.015	0.025
C	1.24	1.55	0.049	0.061
D	0.25	0.41	0.010	0.016
F	0.10	0.15	0.004	0.006
H	0.51	0.76	0.020	0.030
J	0.03	0.08	0.001	0.003
K	4.19	4.45	0.165	0.175
M	3°	7°	3°	7°

CASE 29-02 (TO-92)

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

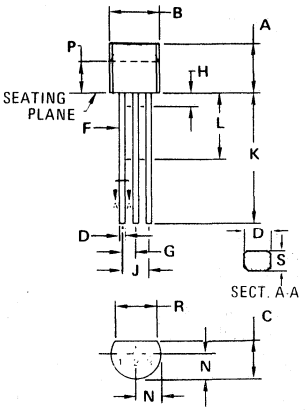
STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

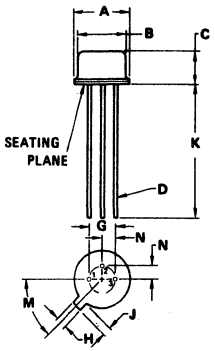


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 31-01

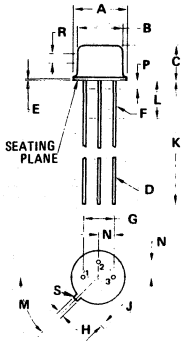
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.57	0.150	0.180
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

NOTE:
1. LEADS WITHIN 0.36 mm (0.014) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 31-03 (TO-05)



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	–	1.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.179	–	0.007

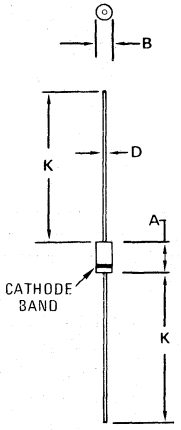
All JEDEC dimensions and notes apply.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. GATE
3. ANODE

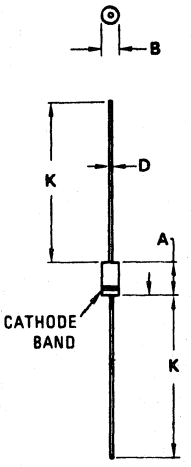
STYLE 3:
PIN 1. GATE
2. CATHODE
3. ANODE

CASE 59-01 (DO-41)



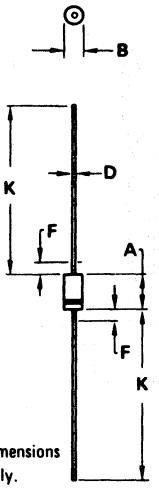
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.70	5.20	0.185	0.205
B	2.54	2.71	0.100	0.107
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.13	8.38	0.320	0.330
B	3.73	3.99	0.147	0.157
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

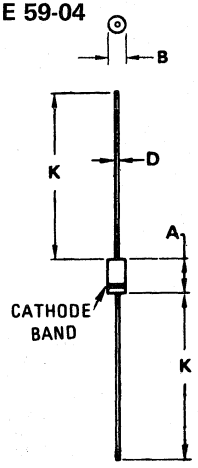
CASE 59-03 (DO-41)



All JEDEC dimensions and notes apply.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	–	1.27	–	0.050
K	27.94	–	1.100	–

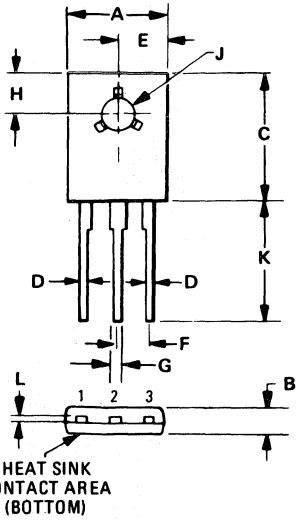
CASE 59-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

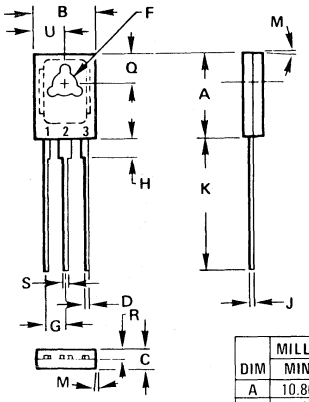
CASE 77-02

PIN 1. CATHODE
2. ANODE
3. GATE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.860	8.380	0.270	0.330
B	1.770	3.300	0.070	0.130
C	9.910	11.430	0.390	0.450
D	0.508	0.660	0.020	0.026
E	3.810 NOM		0.150 NOM	
F	2.290 TP		0.090 TP	
G	0.635	0.889	0.025	0.035
H	3.300	4.450	0.130	0.175
J	2.910	3.000	0.115	0.118
K	15.110	16.650	0.595	0.655
L	0.381	0.635	0.015	0.025

CASE 77-03

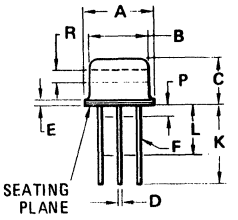


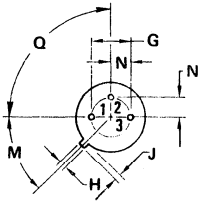
STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE
STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE
STYLE 3
PIN 1. BASE
2. COLLECTOR
3. EMITTER
STYLE 4
PIN 1. ANODE 1
2. ANODE 2
3. GATE
STYLE 5
PIN 1. MT1
2. MT2
3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

NOTES:
1. MT = MAIN TERMINAL
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT MAXIMUM MATERIAL CONDITION.

CASE 79-02 (TO-39)



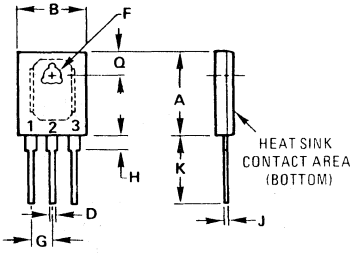


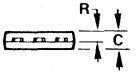
STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR
STYLE 2
PIN 1. DRAIN
2. SOURCE
3. GATE
STYLE 3
PIN 1. CATHODE
2. GATE
3. ANODE
STYLE 4
PIN 1. MAIN TERM. 1
2. GATE
3. MAIN TERM. 2
STYLE 5
PIN 1. COLLECTOR
2. BASE
3. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 90-04

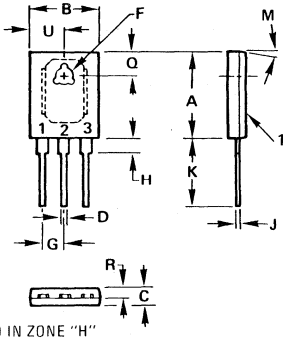




STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.95	16.71	0.628	0.658
B	12.45	13.21	0.490	0.520
C	3.05	3.81	0.120	0.150
D	1.09	1.25	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	–	3.18	–	0.125
J	0.76	0.86	0.030	0.034
K	14.99	16.51	0.590	0.650
Q	4.50	5.00	0.177	0.197
R	1.91	2.16	0.075	0.085

CASE 90-05

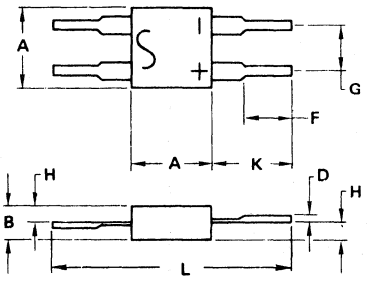


NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE
STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE
STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE
STYLE 4:
PIN 1. MT 1
2. MT 2
3. GATE
MT = MAIN TERMINAL

CASE 109-02



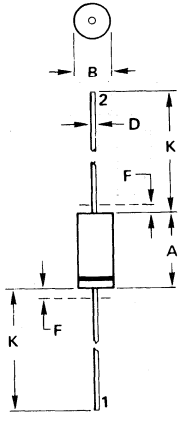
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.73	0.240	0.265
B	2.29	2.79	0.090	0.110
D	0.51	1.02	0.020	0.040
F	3.81	5.08	0.150	0.200
G	3.68	3.94	0.145	0.155
H	1.02	1.27	0.040	0.050
K	6.60	8.64	0.260	0.340
L	19.30	24.00	0.760	0.945

NOTES:
1. LEAD DIM "D" TO BE MEASURED WITHIN "F"
2. LEADS ARE TO BE TIN DIPPED WITHIN "F"
3. LEADS FORMED TO FIT INTO HOLE 0.94 mm (0.037) MIN.

CASE 109-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.73	0.240	0.265
B	2.29	2.79	0.090	0.110
D	0.51	0.94	0.020	0.037
F	3.56	6.35	0.140	0.250
G	3.68	3.94	0.145	0.155
H	1.02	1.27	0.040	0.050
K	6.60	10.16	0.260	0.400
L	19.30	27.05	0.760	1.065

CASE 146-01 (DO-14)

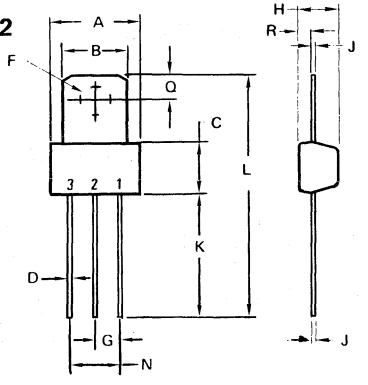


STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.74	3.56	0.108	0.140
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply.

CASE 152-02

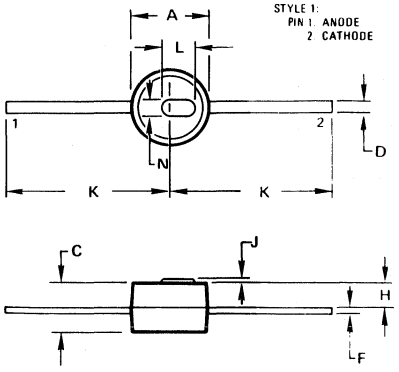


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

NOTE:
1. LEADS WITHIN 0.15 mm (0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

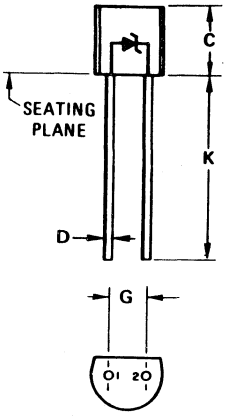
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 166-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.98	2.34	0.078	0.092
C	1.22	1.47	0.048	0.058
D	0.25	0.41	0.010	0.016
F	0.10	0.15	0.004	0.006
H	0.51	0.76	0.020	0.030
J	0.03	0.08	0.001	0.003
K	4.19	4.45	0.165	0.175
L	0.89	1.14	0.035	0.045
N	0.38	0.64	0.015	0.025

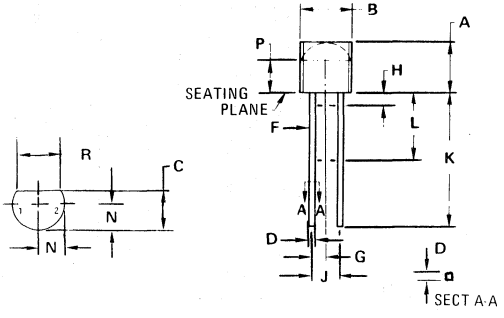
CASE 182-01



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
C	0.175	0.185	4.45	4.70
D	0.016	0.019	0.406	0.483
G	0.090	0.110	2.29	2.79
K	0.594		15.09	

CASE 182-02 (TO-92)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

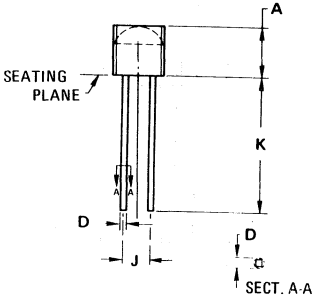
All JEDEC dimensions and notes apply

STYLE 1:
PIN 1. ANODE
2. CATHODE

STYLE 2:
PIN 1. CATHODE
2. ANODE

STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

CASE 182-03



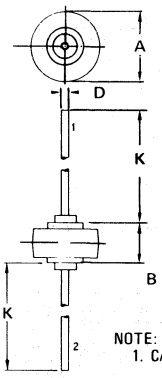
STYLE 1:
PIN 1. ANODE
2. CATHODE

STYLE 2:
PIN 1. CATHODE
2. ANODE

STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 194-02

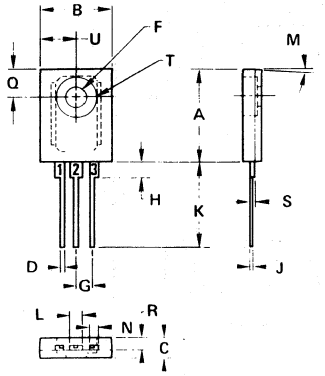


STYLE 1:
PIN 1. CATHODE
2. ANODE

NOTE:
1. CATHODE SYMBOL ON PKG.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.03	10.29	0.395	0.405
B	5.94	6.25	0.234	0.246
D	1.27	1.35	0.050	0.053
K	25.15	25.65	0.990	1.010

CASE 199-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

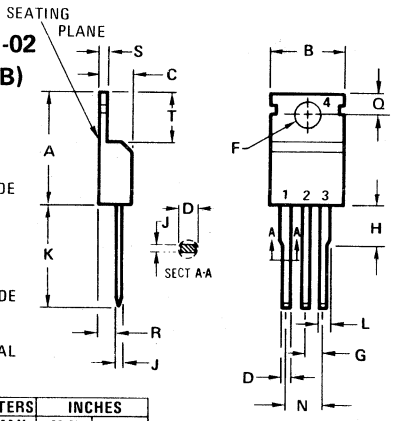
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 3:
PIN 1. ANODE 1
2. ANODE 2
3. GATE

NOTES:
1. DIM "G" IS TO CENTER OF LEADS
2. LEADS WITHIN 0.25 mm (0.010") TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
3. LEADS MUST GO INTO 0.86 mm (0.034") DIA HOLE & NOT GO INTO 0.64 mm (0.025") DIA HOLE.
4. DIM "T" TO BE MEASURED AT BOTTOM OF HOLE.

CASE 221-02 (TO-220AB)



STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. NEUTRAL

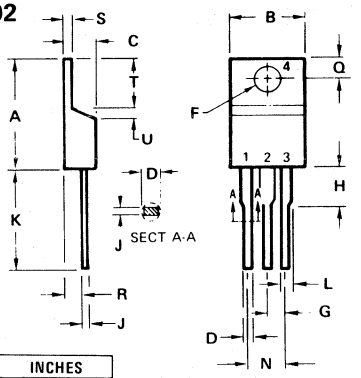
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	--	6.35	--	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NEUTRAL

All JEDEC dimensions and notes apply

CASE 221A-02 (TO-220AB)

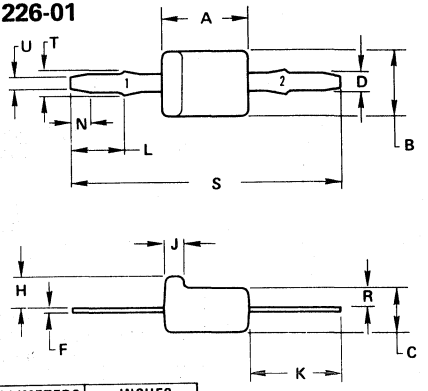


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

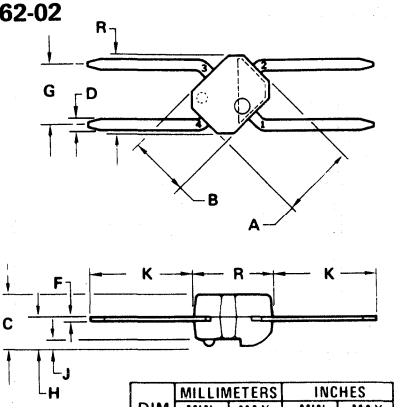
CASE 226-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.86	4.11	0.152	0.162
B	2.92	3.18	0.115	0.125
C	1.91	2.16	0.075	0.085
D	0.64	0.89	0.025	0.035
F	0.08	0.18	0.003	0.007
H	1.30	1.55	0.051	0.061
J	0.64	0.89	0.025	0.035
K	4.06	4.32	0.160	0.170
L	2.36	2.62	0.093	0.103
N	1.12	1.37	0.044	0.054
R	0.79	1.04	0.031	0.041
S	11.99	12.75	0.472	0.502
T	1.14	1.40	0.045	0.055
U	0.43	0.69	0.017	0.027

PIN 1. CATHODE
2. ANODE

CASE 262-02



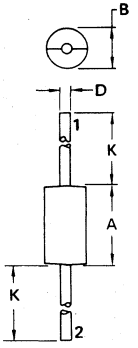
STYLE 1:
PIN 1. SOURCE
2. DRAIN
3. GATE 2
4. GATE 1

STYLE 2:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.95	5.21	0.195	0.205
B	3.94	4.19	0.155	0.165
C	2.67	2.92	0.105	0.115
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	4.06 BSC		0.160 BSC	
H	1.57	1.83	0.062	0.072
J	0.51	0.76	0.020	0.030
K	6.35	7.62	0.250	0.300
R	5.21	5.46	0.205	0.215

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

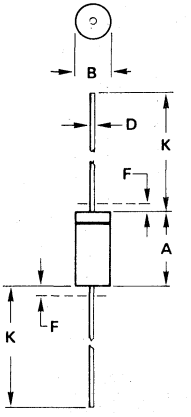
CASE 267-01



STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 299-01

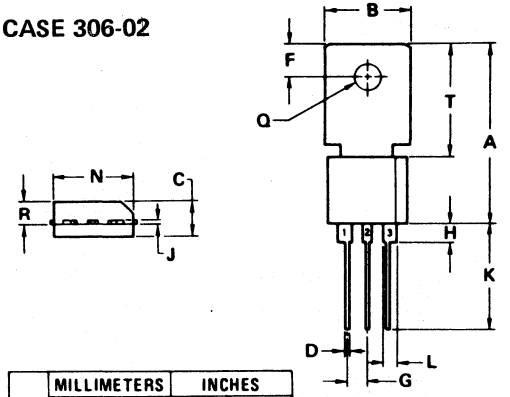


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	12.70	–	0.500	–

All JEDEC dimensions and notes apply.

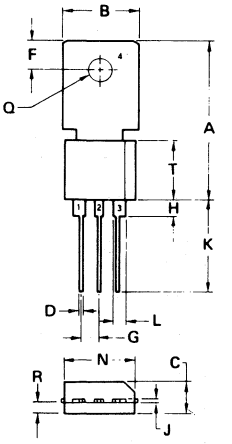
NOTE:
1. POLARITY DENOTED BY CATHODE BAND.
2. LEAD DIAMETER IS NOT CONTROLLED WITHIN DIMENSION "F".

CASE 306-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04



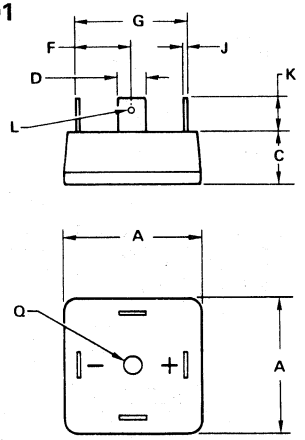
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

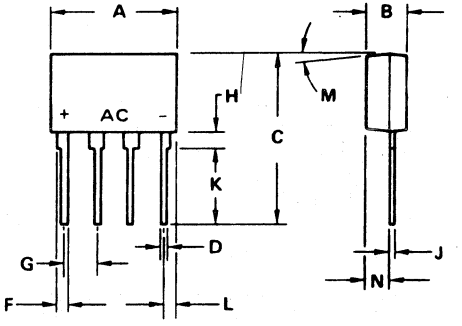
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 309-01



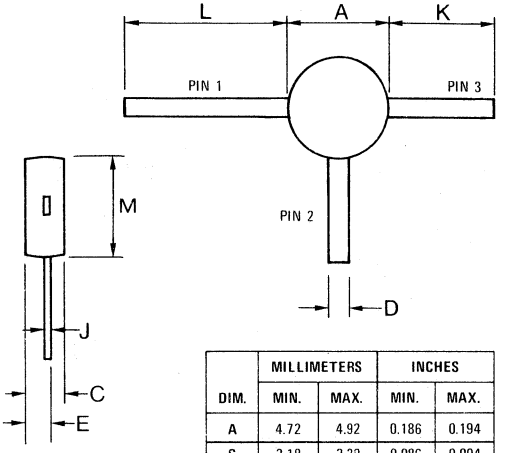
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.80	35.18	1.370	1.385
C	12.70	13.97	0.500	0.550
D	6.10	6.60	0.240	0.260
F	12.70	13.97	0.500	0.550
G	25.40	27.94	1.000	1.100
J	0.71	0.86	0.028	0.034
K	8.89	10.16	0.350	0.400
L	1.52	2.06	0.060	0.081
Q	4.44	4.70	0.175	0.185

CASE 312-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	4.57	5.08	0.180	0.200
C	–	20.57	–	0.810
D	0.64	0.89	0.025	0.035
F	1.02	1.27	0.040	0.050
G	3.68	3.94	0.145	0.155
H	1.90	2.16	0.075	0.085
J	0.56	0.71	0.022	0.028
K	–	9.02	–	0.355
L	1.78	2.03	0.070	0.080
M	–	6^0	–	6^0
N	2.54	2.79	0.100	0.110

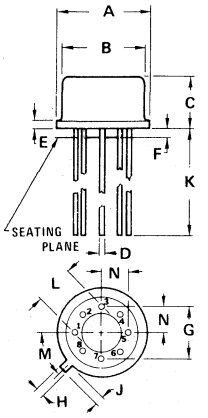
CASE 317A



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.72	4.92	0.186	0.194
C	2.18	2.39	0.086	0.094
D	0.83	0.99	0.033	0.039
E	1.16	1.36	0.046	0.054
J	0.24	0.26	0.009	0.010
K	4.95	5.45	0.195	0.215
L	8.25	8.76	0.325	0.345
M	–	0.50	–	0.020

PIN 1: COLLECTOR
PIN 2: BASE
PIN 3: EMITTER

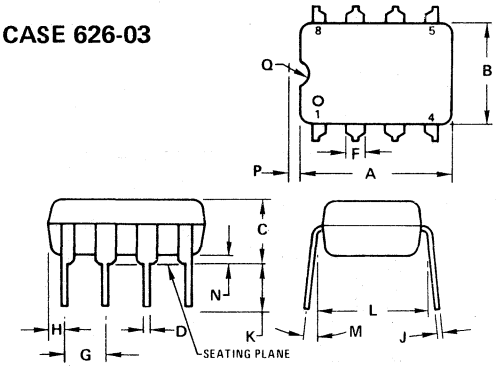
CASE 601-04



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

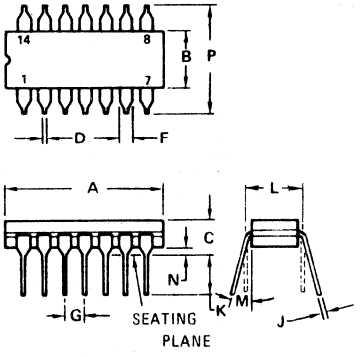
CASE 626-03



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

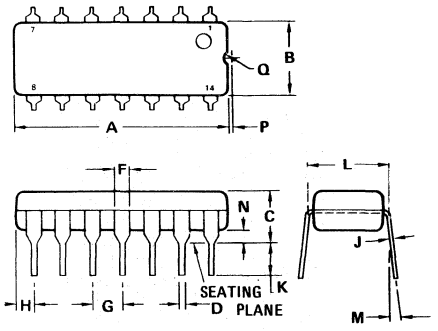
CASE 632-02 (TO-116)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

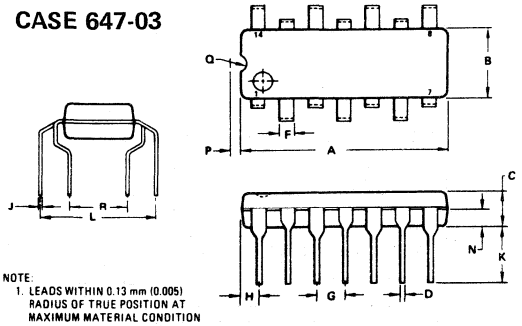
CASE 646-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

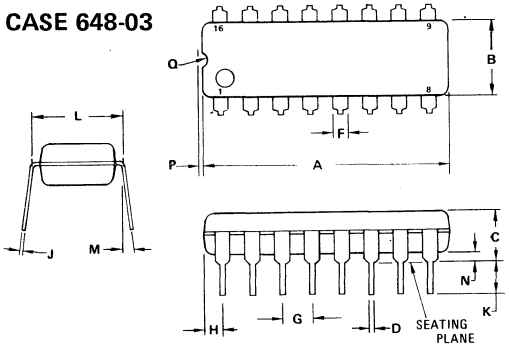
CASE 647-03



NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	3.30	3.81	0.130	0.150
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	3.81	–	0.150	–
L	9.52	10.92	0.375	0.430
N	1.02	1.52	0.040	0.060
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030
R	4.70	5.97	0.185	0.235

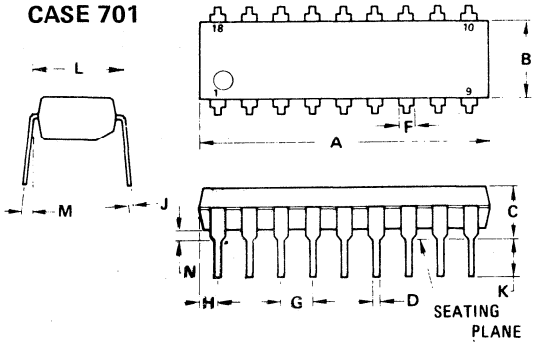
CASE 648-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

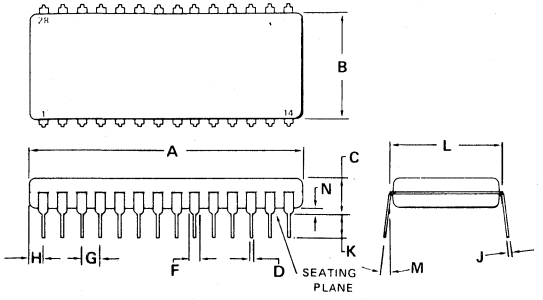
CASE 701



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

CASE 710-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

Lead tape packaging standards for axial-lead components

1.0. SCOPE

This section covers packaging requirements for the following axial-lead components for use in automatic testing and assembly equipment: Motorola Case 51 (DO-7), Case 52 (DO-13), Case 59 (DO-41), Case 267, Case 299 (DO-35), Case 59-04, Case 169-02 and Case 17. Packaging, as covered in this document, shall consist of axial-lead components mounted by their leads on pressure-sensitive tape, either wound onto a reel of folded in an oriented manner in a container (ammunition pack).

2.0. PURPOSE

This document establishes Motorola standard practices for lead-tape packaging of axial-lead components and meets the requirements of EIA Standard RS-296-C, "Reel Packaging of Components with Axial Leads".

3.0. REQUIREMENTS

3.1. *Component Leads*

3.1.1. Component leads shall not be bent beyond dimension E from their nominal position. See Figure 2.

3.1.2. The "C" dimension shall be governed by the overall length of the reel packaged component. The distance between flanges shall be 0.318 cm to 0.635 cm greater than the overall component length. See Figures 2 and 3.

3.2. *Orientation*

All polarized components must be oriented in one diretion. The cathode lead tape shall be blue, and the anode tape shall be white. See Figure 1.

3.3. *Reeling*

3.3.1. Components on any reel shall not represent more than two date codes when date code identification is required.

3.3.2. Component leads shall be positioned perpendicularly between pairs of 0.635 cm tape. See Figure 2.

3.3.3. A minimum 30.5 cm leader of tape shall be provided before the first and last component on the reel.

3.3.4. 50 lb. Kraft paper must be wound between layers of components as far as necessary for component protection. Width of paper is 0.158 cm to 1.905 cm less than "C" dimension of reel. See Figure 3.

3.3.5. A row of components must be centered between the tapes ±0.119 cm. In addition, individual components may deviate from center of component row ±0.079 cm. See Figure 2.

3.3.6. Staples shall not be used for splicing. No more than 4 layers of tape shall be used in any splice area and no tape shall be offset from another by more than 0.079 cm noncumulative. Tape splices shall overlap at least 15.24 cm for butt joints and at least 7.62 cm for lap joints, and shall not be weaker than unspliced tape.

3.3.7. Quantity per reel shall be as indicated in Table 1. When reeling quantity is less than the established minimum of a suitable sized reel, an ammunition pack will be used. Quantities less than the ammunition pack munimum will not be lead-taped.

3.3.8. A maximum of 10 components may be missing from any 3 metre section. A maximum of 2 consecutive components may be missing, provided this gap is followed by 6 consecutive components.

3.3.9. The single face roll pad shall be placed around the finished reel and taped securely. Each reel shall then be placed in an appropriate container.

3.4. *Marking*

Minimum reel and carton marking shall consist of the following: See Figure 3.

Customer Part Number
Purchase Order Number
Quantity
Date of Reeling (when applicable)
Manufacturer's Name
Electrical Value (when applicable)
Date Codes (when applicable; see Note 3.3.1.)
Tape (when applicable)

4.0. EXCEPTIONS

Requirements differing from this Motorola standard shall be negotiated with the factory.
Complies with DIN 40810 for Case 59.04, Case 267 Rectifier Diodes.

TABLE 1 – PACKAGING

Component Type (Case)	Quantity Per Reel Min/Max	Ammunition Pack Quantity Min	Component Spacing A	Tape Spacing B	Reel Dimensions C	Reel Dimensions D(Max)	Max. Off Alignment E
Case 51 (DO-7) Case 299 (DO-35)	1000/3000	500	0.508 ± 0.079	5.16 ± 0.079	7.62	26.67	0.158
Case 17 Case 59 (DO-41) Case 59-04 Case 169-02	1000/5500	500	0.508 ± 0.038	5.16 ± 0.079	7.62	35.56	0.119
Case 52 (DO-13)	500/1500	250	0.953 ± 0.038	6.033 ± 0.051	9.68	35.56	0.119
Case 267	500/1500	250	0.953 ± 0.038	0.953 ± 0.079	7.62	35.56	0.119

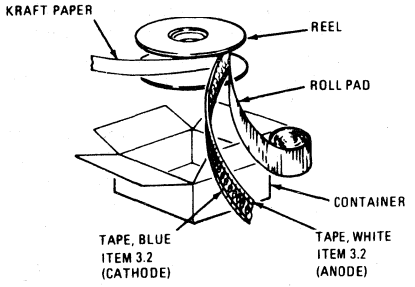


FIGURE 1 – REEL PACKING

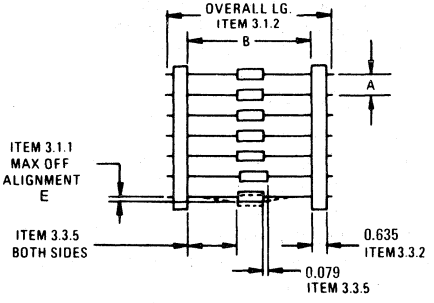


FIGURE 2 – COMPONENT SPACING

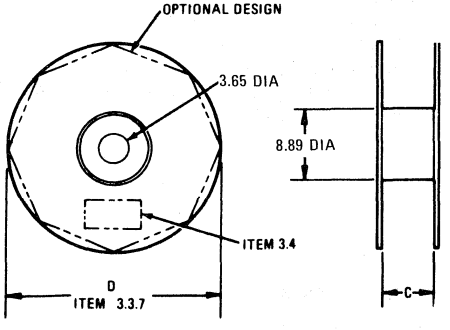


FIGURE 3 – REEL DIMENSIONS

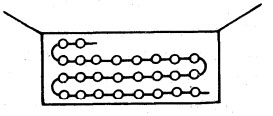


FIGURE 4 – AMMUNITION PACK

POWER TRANSISTORS

Power Plastic Transistor in Order of I_C (max.)		I_C (cont.) A	H_{FE} @ → I_C → V_{CE} (min.)	A	V	P_D W	V_{CEO} V	Polarity	Package	Page
BF457, 458, 459	TV Video Output Stages	0.1	25	0.03	10	12.5	160-300	NPN	77	3-127
BD157, 158, 159	TV Radio Power Output Stages	0.5	30	0.05	10	20	250-350	NPN	77	3-7
BD232	TV Power Output and Line Driving	0.5	25	0.05	5	20	300	NPN	77	3-29
MJE340	High Voltage General	0.5	30	0.05	10	20.8, 30	300	NPN	77	3-185
MJE 350	High Voltage General	0.5	30	0.05	10	20	300	PNP	77	3-187
TIP29	General Purpose	1	40	0.2	4	30	40-100	NPN	TO-220	3-225
TIP30	General Purpose	1	40	0.2	4	30	40-100	PNP	TO-220	3-225
TIP47, 48, 49, 50	High Voltage General	1	30	0.3	10	40	250-400	NPN	TO-220	3-235
BD135, 137, 139	Audio Amplifier and Driver	1.5	25	0.5	2	12.5	45-80	NPN	77	3-1
BD136, 138, 140	Audio Amplifier and Driver	1.5	25	0.5	2	12.5	45-80	PNP	77	3-3
BD165, 167, 169	Audio Amplifier and Driver	1.5	40	0.15	2	20	45-80	NPN	77	3-9
BD166, 168, 170	Audio Amplifier and Driver	1.5	40	0.15	2	20	45-80	PNP	77	3-11
MJE13002, 13003	Fast Switch Mode Applications	1.5	8	0.5	2	40	300-400	NPN	77	3-193
BD233, 235, 237	Audio Amplifier and Driver	2	40	0.15	2	25	45-80	NPN	77	3-31
BD234, 236, 238	Audio Amplifier and Driver	2	40	0.15	2	25	45-80	PNP	77	3-33
TIP110, 111, 112	General Purpose Darlington	2	1000	1	4	50	60-100	NPN	TO-220	3-239
TIP115, 116, 117	General Purpose Darlington	2	1000	1	4	50	60-100	PNP	TO-220	3-239
BD175, 177, 179	Audio Amplifier and Driver	3	40	0.15	2	30	45-80	NPN	77	3-13
BD176, 178, 180	Audio Amplifier and Driver	3	40	0.15	2	30	45-80	PNP	77	3-15
TIP31	General Purpose	3	25	1	4	40	40-100	NPN	TO-220	3-227
TIP32	General Purpose	3	25	1	4	40	40-100	PNP	TO-220	3-227
BD185, 187, 189	Audio Amplifier	4	40	0.5	2	40	30-60	NPN	77	3-17
BD186, 188, 190	Audio Amplifier	4	40	0.5	2	40	30-60	PNP	77	3-19
BD361, 361A	General Purpose	4	80	0.5	1	15	20	NPN	77	3-45
BD362, 362A	General Purpose	4	80	0.5	1	15	20	PNP	77	3-47
BD561	Audio Amplifier, General	4	60	0.5	1	40	40	NPN	77	3-88
BD562	Audio Amplifier, General	4	60	0.5	1	40	40	PNP	77	3-90
BD675, 677, 679, 681	General Purpose Darlington	4	750	1.5	3	40	45-100	NPN	77	3-92
BD676, 678, 680, 682	General Purpose Darlington	4	750	1.5	3	40	45-100	PNP	77	3-94
BD775, 777, 779	High Speed Switching Darlington	4	750	2	3	15	45-80	NPN	77	3-96
BD776, 778, 780	High Speed Switching Darlington	4	750	2	3	15	45-80	PNP	77	3-96
BD785, 787	Switch and Amplifier	4	40	0.2	3	15	45-60	NPN	77	3-98
BD786, 788	Switch and Amplifier	4	40	0.2	3	15	45-60	PNP	77	3-98
BD789, 791	High Speed Switching and Audio	4	40	0.2	3	15	80-100	NPN	77	3-102
BD790, 792	High Speed Switching and Audio	4	40	0.2	3	15	80-100	PNP	77	3-102
BD195, 197, 199	Audio Amplifier, General	6	30	1	2	65	30-60	NPN	90	3-21
BD196, 198, 200	Audio Amplifier, General	6	30	1	2	65	30-60	PNP	90	3-23
BD243	Switching and Amplifier	6	30	0.3	4	65	45-100	NPN	TO-220	3-35
BD244	Switching and Amplifier	6	30	0.3	4	65	45-100	PNP	TO-220	3-35
TIP41	General Purpose	6	30	0.3	4	65	40-100	NPN	TO-220	3-231
TIP42	General Purpose	6	30	0.3	4	65	40-100	PNP	TO-220	3-231
BD795, 797, 799, 801	Audio Amplifier, General	8	30	1	2	65	45-100	NPN	TO-220	3-106
BD796, 798, 800, 802	Audio Amplifier, General	8	30	1	2	65	45-100	PNP	TO-220	3-108
BD895, 897, 899, 901	General Purpose Darlington	8	750	3	3	70	45-100	NPN	TO-220	3-114
BD896, 898, 900, 902	General Purpose Darlington	8	750	3	3	70	45-100	PNP	TO-220	3-116
BDX53	General Purpose Darlington	8	750	3	3	60	60-100	NPN	TO-220	3-118
BDX54	General Purpose Darlington	8	750	3	3	60	60-100	PNP	TO-220	3-118
MJE13006, 13007	High Voltage, High Speed Switching	8	8	2	5	80	300-400	NPN	TO-220	3-201
TIP120, 121, 122	General Purpose Darlington	8	1000	0.5	3	65	60-100	NPN	TO-220	3-244
TIP125, 126, 127	General Purpose Darlington	8	1000	0.5	3	65	60-100	PNP	TO-220	3-244
BD205, 207	High Power Audio Amplifier	10	30	2	2	90	45-60	NPN	90	3-25
BD206, 208	High Power Audio Amplifier	10	30	2	2	90	45-60	PNP	90	3-27
BD805, 807, 809	High Power Audio Amplifier	10	30	2	2	90	45-80	NPN	TO-220	3-110
BD806, 808, 810	High Power Audio Amplifier	10	30	2	2	90	45-80	PNP	TO-220	3-112
MJE2955, 2955T	General Purpose	10	20	4	4	90	60	PNP	90/TO-220	3-189
MJE3055, 3055T	General Purpose	10	20	4	4	90	60	NPN	90/TO-220	3-191
MJE13008, 13009	High Voltage, High Speed Switching	12	8	5	5	100	300-400	NPN	TO-220	3-209

Power Metal Transistor in Order of I_C (max.)		I_C (cont.) A	H_{FE} @ → I_C (min.)	A	→ V_{CE} V	P_D W	V_{CEO} V	Polarity	Package	Page
BU205	TV Horizontal Deflection	2.5	2	3	5	56	700	NPN	11	3-164
BU126, 126A	Switch Mode Power Supplies	4	15	1	5	50	250-300	NPN	11	3-161
BU208, 208A	TV Horizontal Deflection	5	2.25	4.5	5	56	700	NPN	TO-3	3-166
BU311, 312	TV Horizontal Deflection	6	10	5	1.5	50	125-150	NPN	11-03	3-168
BU326, 326A	Switch Mode Power Supplies	6	10	2.5	10	75	375-400	NPN	11-03	3-175
BU104	TV Horizontal Deflection	7	10	5	1.75	85	150	NPN	11-03	3-153
BU322, 322A	Automotive Ignition Darlington	7	50	4	1.7	100	400-475	NPN	11-01	3-170
MJ900, 901	Amplifier Output Darlington	8	1000	3	3	90	60-80	PNP	11	3-177
MJ1000, 1001	Amplifier Output Darlington	8	1000	3	3	90	60-80	NPN	11	3-177
BD311, 313	Audio Amplifier Output	10	5	5.4	4	150	60-80	NPN	11	3-39
BD312, 314	Audio Amplifier Output	10	5	5.4	4	150	60-80	PNP	11	3-39
BU109	TV Horizontal Deflection	10	15	5	1.5	85	120	NPN	11-03	3-156
BU110	TV Horizontal Deflection	10	5	7	1.5	90	150	NPN	11-03	3-159
BU323, 323A	Automotive Ignition Darlington	10	50	6	1.7	125	400-475	NPN	11-01	3-173
MJ2500, 2501	Amplifier Darlington	10	1000	5	3	150	60-80	PNP	11	3-179
MJ3000, 3001	Amplifier Darlington	10	1000	5	3	150	60-80	NPN	11	3-179
BD142	Switching and Amplifier	15	120	0.5	4	117	40	NPN	11	3-5
MJ2955	Switching and Amplifier	15	20	4	4	150	60	PNP	11	3-181
2N3055	High Power Audio, Switching	15	20	4	4	115	60	NPN	11-03	3-249
BD315, 317	Audio Amplifier Output	16	15	8.5	4	200	80-100	NPN	11	3-42
BD316, 318	Audio Amplifier Output	16	15	8.5	4	200	80-100	PNP	11	3-42
2N3773	High Power Audio, Switching	16	15	8	4	150	140	NPN	11-03	3-253
2N6609	High Power Audio, Switching	16	15	8	4	150	140	PNP	11-03	3-253
2N5629, 30, 31	High Power Audio, Switching	16	15-25	8	2	200	100-140	NPN	11	3-258
2N6029, 30, 31	High Power Audio, Switching	16	15-25	10	2	200	100-140	PNP	11-03	3-262
BD364, 366, 368	Audio Amplifier Output	20	20	10	4	200	50-80	NPN	11	3-49
BD365, 367, 369	Audio Amplifier Output	20	20	10	4	200	50-80	PNP	11	3-49

Uniwatt and Duowatt Transistors		I_C (cont.) A	H_{FE} @ (min.)	I_C mA	V_{CE} V	P_D W	V_{CEO} V	Polarity	Package	Page
BD385, 387, 389	General Purpose	1	80	50	1	2	60-100	NPN	306	3-52
BD386, 388, 390	General Purpose	1	80	50	1	2	60-100	PNP	306	3-56
BD411, 412	Amplifier and Driver Darlington	2	15, 25K	200	5	2	40	NPN	306	3-60
BD413, 414	Amplifier and Driver Darlington	2	15, 25K	200	5	2	40	PNP	306	3-64
BD415, 417, 419	General Purpose	1	80	50	1	2	60-100	NPN	306	3-68
BD416, 418, 420	General Purpose	1	80	50	1	2	60-100	PNP	306	3-72
BD505, 507, 509	Comp. Symmetry Audio	2	60	250	2	1	20-40	NPN	152	3-76
BD506, 508, 510	Comp. Symmetry Audio	2	60	250	2	1	20-40	PNP	152	3-78
BD515, 517, 519	General Purpose	2	60	150	2	1	45-80	NPN	152	3-80
BD516, 518, 520	General Purpose	2	60	150	2	1	45-80	PNP	152	3-82
BD525, 527, 529	General Purpose	2	60	50	2	1	60-100	NPN	152	3-84
BD526, 528, 530	General Purpose	2	60	50	2	1	60-100	PNP	152	3-86
BF380, 381, 382	TV Video and Luminance Output	0.5	25	30	10	1	180-300	NPN	152	3-123
BF460, 461, 462	TV Video and Chroma Output	0.5	40	30	10	2	250-350	NPN	306	3-129
BF463, 464, 465	TV Video and Chroma Output	0.5	40	30	10	2	250-350	PNP	306	3-133
BF466, 467, 468	TV Horizontal Deflection Driver	1	30	10	10	2	150-250	NPN	306	3-137
BF666, 667, 668	TV Horizontal Deflection Driver	1	40	10	10	2	150-250	NPN	306	3-141
BF757, 758, 759	TV Video and Chroma Output	0.5	40	30	10	2	250-350	NPN	306	3-145
BF760, 761, 762	TV Video and Chroma Output	0.5	40	30	10	2	250-350	PNP	306	3-149
MPSU45	Amplifier Darlington	2	25K	200	5	1	40	NPN	152	3-217
MPSU95	Amplifier Darlington	2	25K	200	5	1	40	PNP	152	3-221

BD135, -6, -10, -16
BD137, -6, -10 • BD139, -6, -10

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

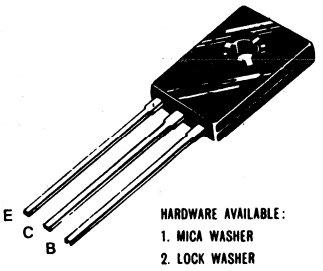
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
10 WATTS



3

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

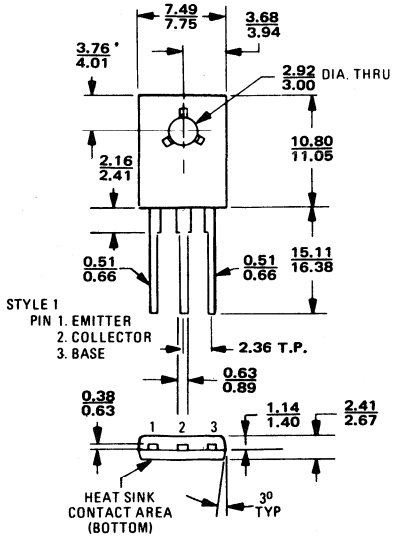
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5A V_{CE} = 2 V)	h_{FE}*	All BD135 BD137,139 All	25 40 40 25	— 250 160 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

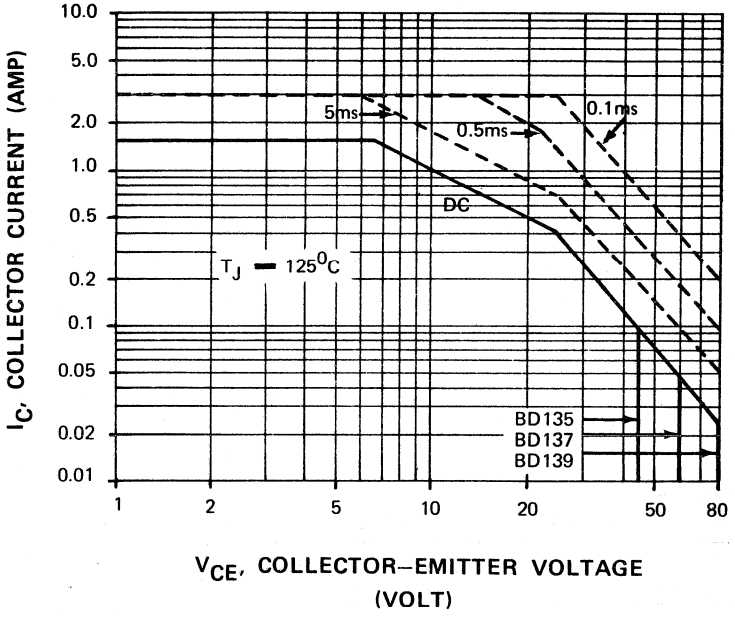


When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

CASE 77-03
(SOT-32/TO-126)
Dimensions in millimeters

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



		Min.	Max.
Available in H_{FE} groups			
(At I_C = 0.15 A, V_{CE} = 2 V) H_{FE} group:	-6	40	100
	-10	63	160
	-16	100	250

BD136, -6, -10, -16
BD138, -6, -10, -16 • BD140, -6, -10

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

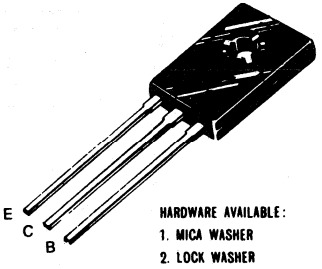
- Available in H_{FE} groups -6, -10, -16
- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
10 WATTS

3



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150	°C

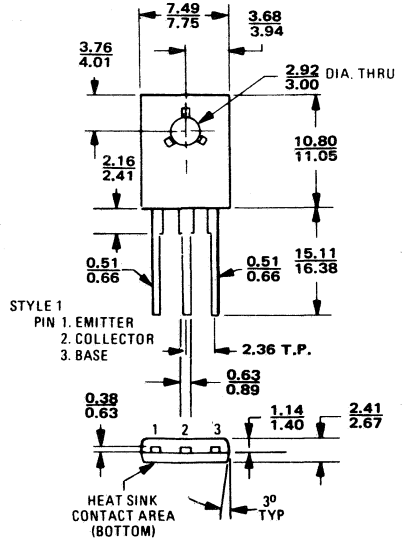
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 136 BD 138 BD 140	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125° C)	I_{CBO}		— — —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005A, V_{CE} = 2 V) (I_C = 0.15A, V_{CE} = 2 V) (I_C = 0.5A, V_{CE} = 2 V)	h_{FE}*	All BD136 BD138,140 All	25 40 40 25	— 250 160 —	—
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



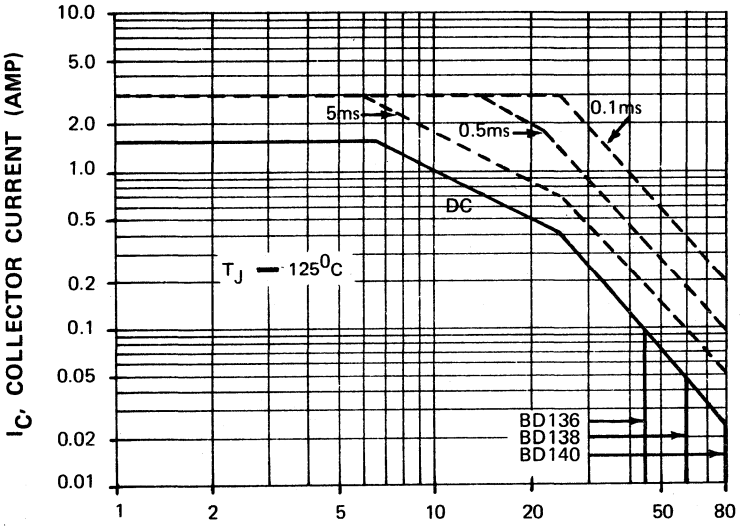
When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

CASE 77-03
(SOT-32/TO-126)
Dimensions in millimeters

3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



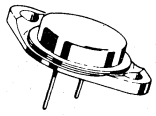
Available in H_{FE} groups (at I_C = 0.15 A, V_{CE} 2 V) H_{FE} group:		Min.	Max.
	-6	40	100
	-10	63	160
	-16	100	250

NPN SILICON POWER TRANSISTOR

. . . designed for general-purpose, moderate speed, switching and amplifier applications

- DC Current Gain
  h_{FE} up to 160 @ I_C = 4 A.dc
- Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4.0 Adc

15 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
117 WATTS



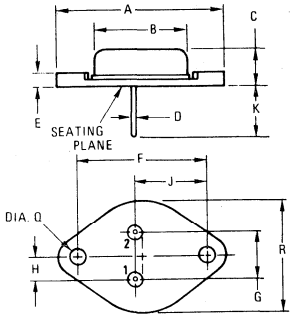
3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage (V_{BE} =—1.5 V)	V_{CEV}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current — Continuous	I_B	7.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	117	Watts
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	°C/W



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

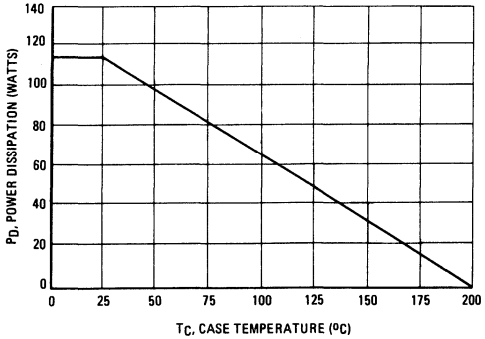
NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	--	39.37	--	1.550
B	--	21.08	--	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43	--	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	--	26.67	--	1.050

Collector connected to case.

CASE 11 (TO-3)

POWER TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO\ (sus)}$	40	–	Vdc
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 100 mAdc, V_{BE} = −1.5V)	BV_{CEV}	50	–	Vdc
Collector-Emitter Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	–	2	mAdc
Emitter-Base Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			
(I_C = 500 mAdc−V_{CE} = 4Vdc)		20	50	
(I_C = 500 mAdc−V_{CE} = 4Vdc)		35	75	
(I_C = 500 mAdc−V_{CE} = 4Vdc)		60	145	
(I_C = 500 mAdc−V_{CE} = 4Vdc)		120	250	
(I_C = 4Adc−V_{CE} = 4Vdc) (note 1)		12.5	160	
Collector emitter saturation voltage− (I_C = 4Adc, I_B = 0.4Adc)	$V_{CE\ (sat)}$		1.1	Vdc
Base-Emitter voltage (I_C = 4Adc−V_{CE} = 4Vdc) (note 1)	$V_{BE\ (on)}$		1.8	Vdc
Power rating test (I_C = 3Adc−V_{CE} = 39Vdc)	P.R.T.	1		s

Note 1: Pulse Width ≈300 μs, Duty Cycle ≦2.0%

BD157
BD158 • BD159

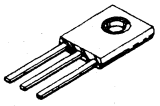
PLASTIC MEDIUM POWER NPN
SILICON TRANSISTOR

. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad† Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON

250-300-350 VOLTS
20 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

*MAXIMUM RATINGS

Rating	Symbol	BD 157	BD 158	BD 159	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0			Adc
Base Current	I_B	0.25			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20 0.16			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			^oC

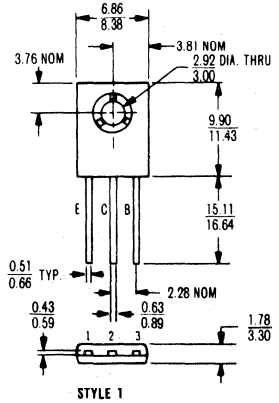
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	BD 157 BD 158 BD 159	250 300 350	–	Vdc
Collector Cutoff Current (At rated voltage)	I_{CBO}		–	100	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}		–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}		30	240	–

†Trademark of Motorola Inc.



STYLE 1
Pin 1. Emitter
2. Collector
3. Base

When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77

FIGURE 1 – POWER TEMPERATURE DERATING CURVE

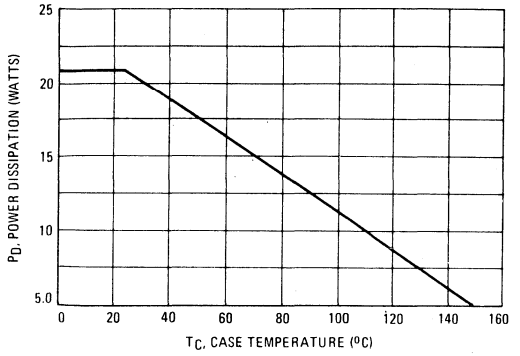


FIGURE 2 – "ON" VOLTAGES

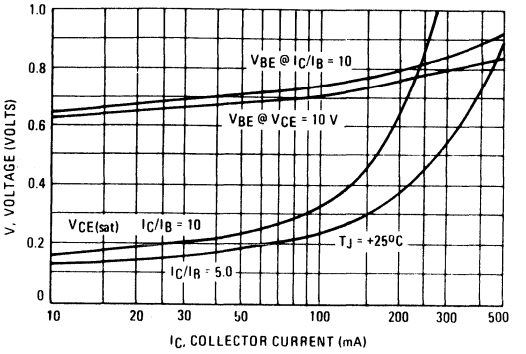
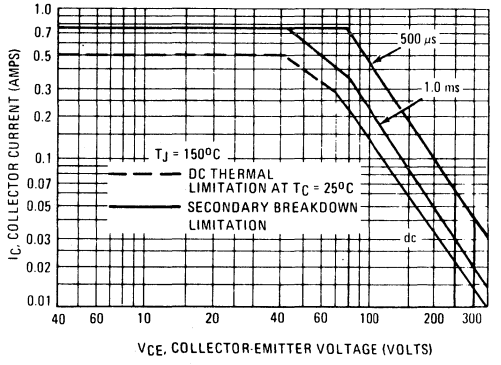
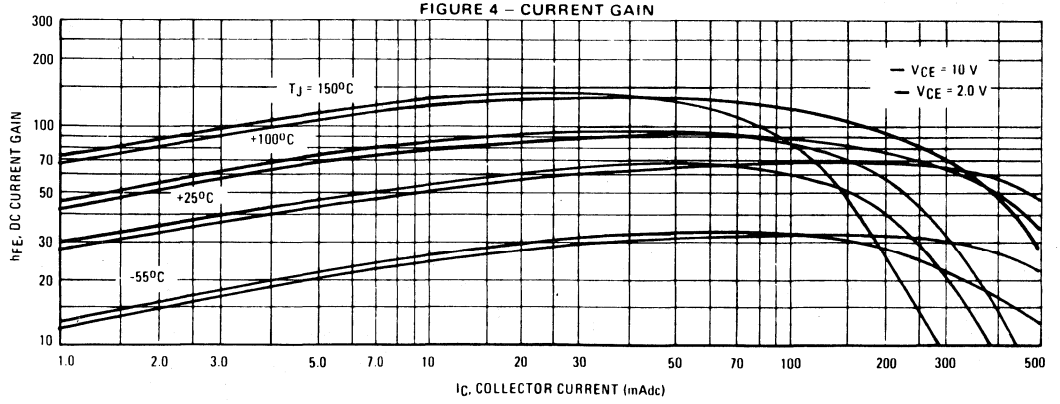


FIGURE 3 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 4 – CURRENT GAIN



BD165
BD167 • BD169

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

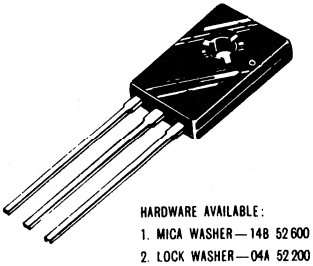
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 165, 167, 169 are complementary with BD 166, 168, 170

1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
20 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 165 BD 167 BD 169	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D		1.25 10	Watts mW/^oC
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D		20 160	Watt mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	^oC

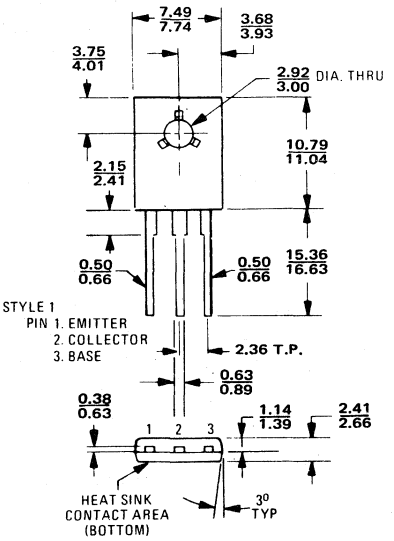
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	100	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25 C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 165 BD 167 BD 169	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 165 BD 167 BD 169	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77-03

FIGURE 1 – P_D–T_C DERATING CURVE

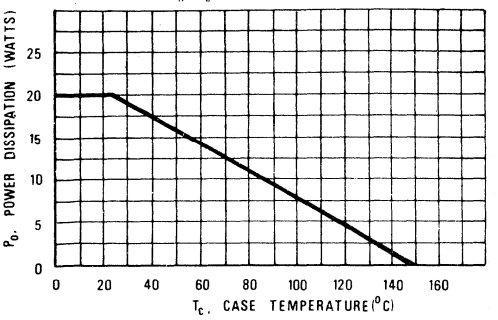
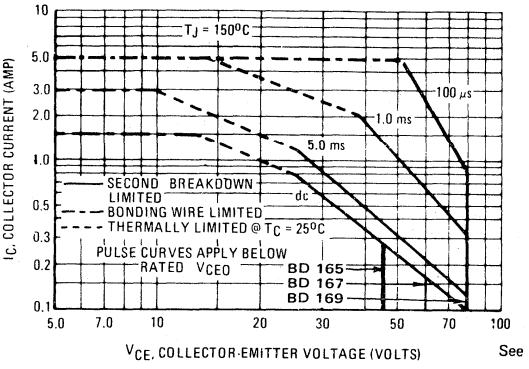


FIGURE 2 – SAFE OPERATING AREA



See Note 1

FIGURE 3 – COLLECTOR SATURATION REGION

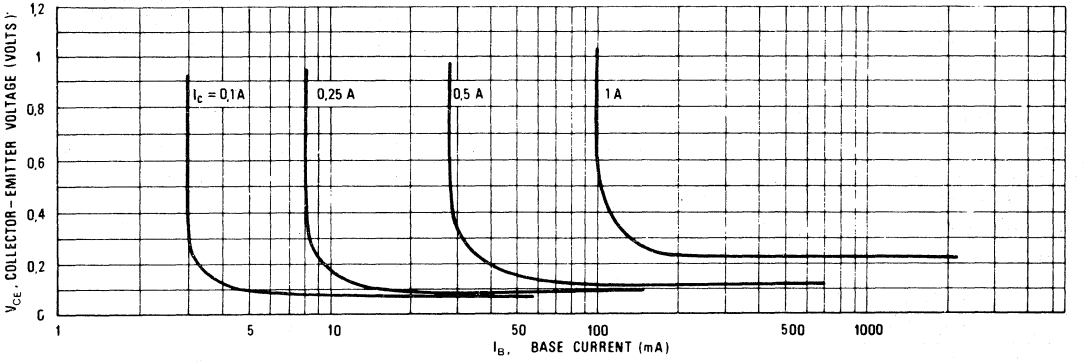


FIGURE 4 – CURRENT GAIN

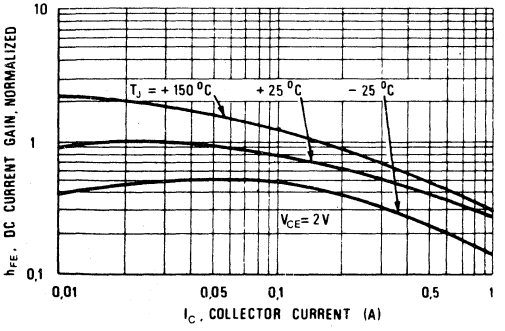
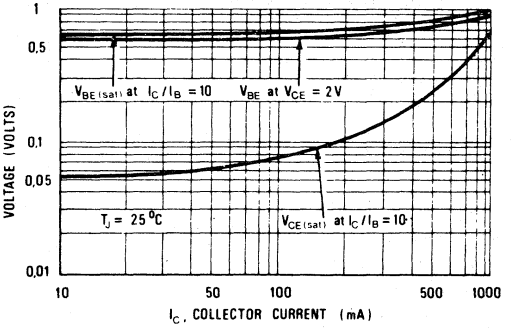


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD166
BD168 • BD170

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

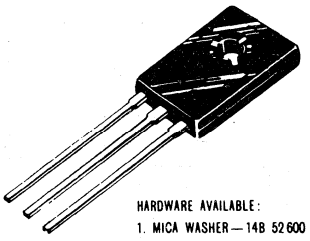
. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 166, 168, 170 are complementary with BD 165, 167, 169

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
20 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 166 BD 168 BD 170	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	°C

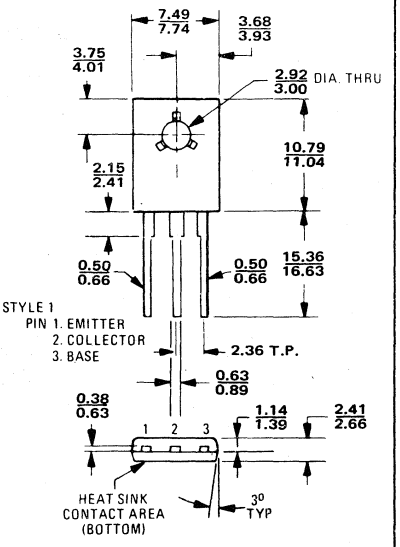
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 166 BD 168 BD 170	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 166 BD 168 BD 170	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base-Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	0.95	Vdc
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-03

FIGURE 1 – P_D–T_C DERATING CURVE

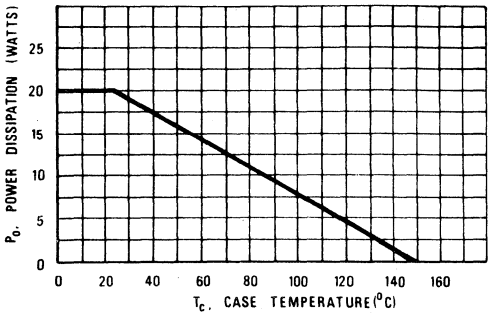
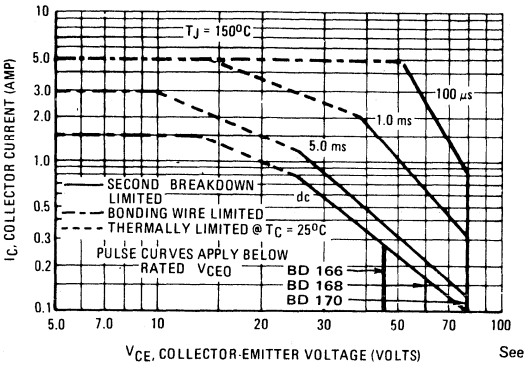


FIGURE 2 – SAFE OPERATING AREA



See Note 1

FIGURE 3 – COLLECTOR SATURATION REGION

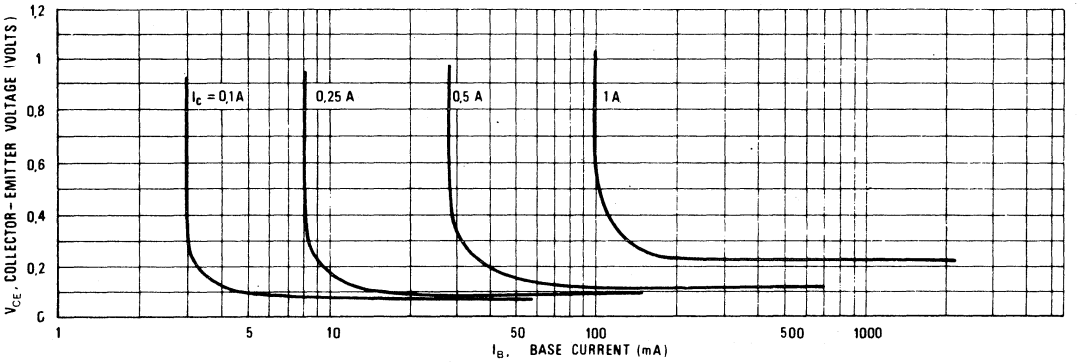


FIGURE 4 – CURRENT GAIN

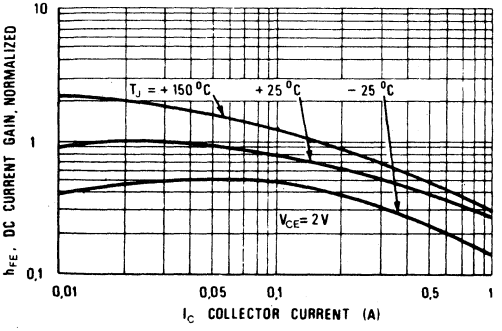
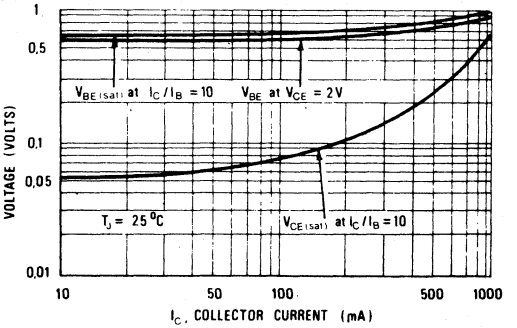


FIGURE 5 – "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD175, -6, -10, -16
BD177, -6, -10 • BD179, -6, -10

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 175, 177, 179 are complementary with BD 176, 178, 180
- Available in H_{FE} groups -6, -10, -16

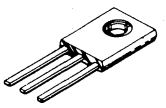
3 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
30 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

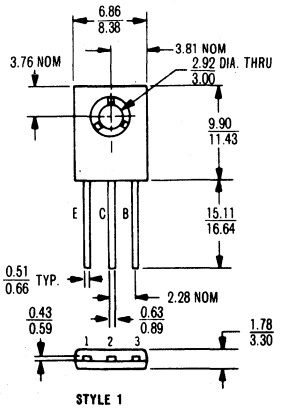
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 175 BD 177 BD 179	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 175 BD 177 BD 179	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) group -6 / -10 / -16 (I_C = 1 A, V_{CE} = 2 V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



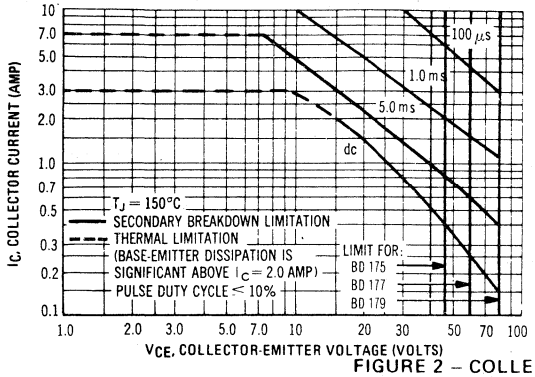
STYLE 1
Pin 1. Emitter
2. Collector
3. Base

When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

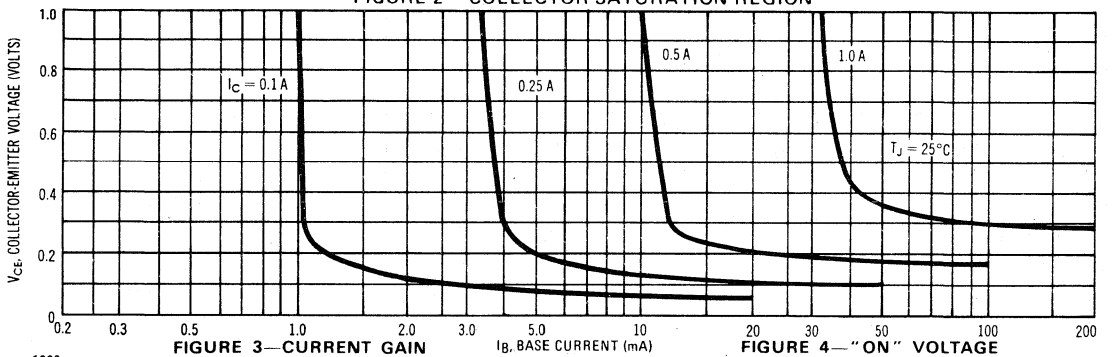


FIGURE 3—CURRENT GAIN

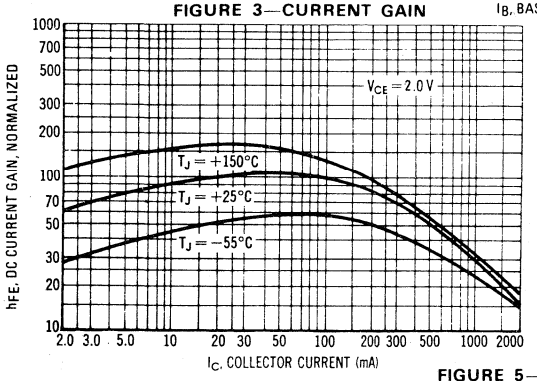


FIGURE 4—"ON" VOLTAGE

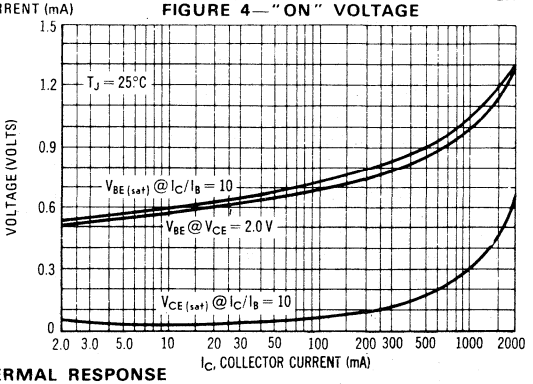
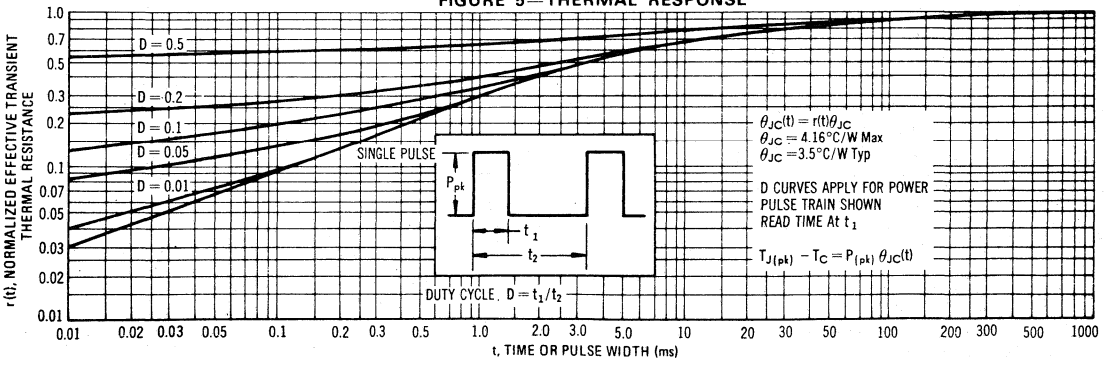


FIGURE 5—THERMAL RESPONSE



BD176, -6, -10, -16
BD178, -6, -10 • BD180, -6, -10

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 176, 178, 180 are complementary with BD 175, 177, 179
- Available in H_{FE} groups -6, -10, -16

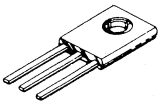
3 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
30 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 176 BD 178 BD 180	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

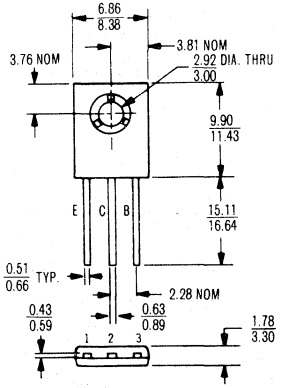
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		4.16	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 176 BD 178 BD 180	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 176 BD 178 BD 180	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2 V) group -6, -10, -16 (I_C = 1 A, V_{CE} = 2 V)	h_{FE}*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.8	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



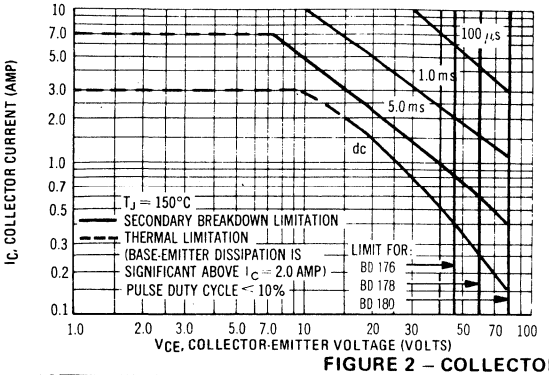
STYLE 1
Pin 1. Emitter
2. Collector
3. Base

When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 77

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

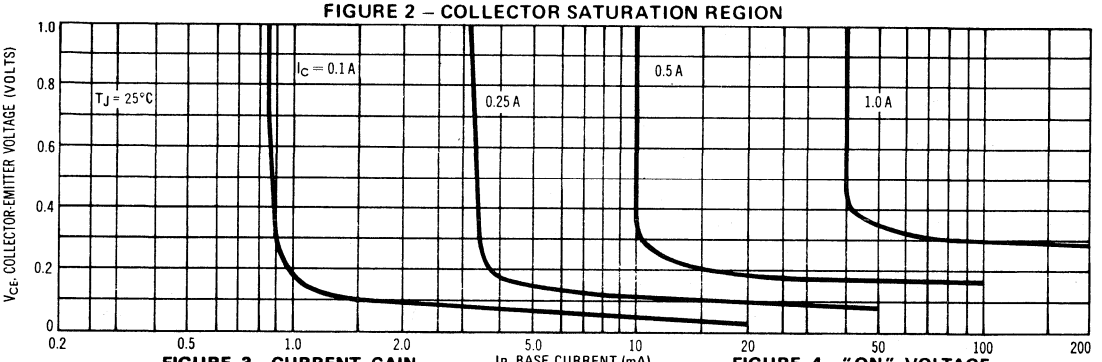


FIGURE 3—CURRENT GAIN

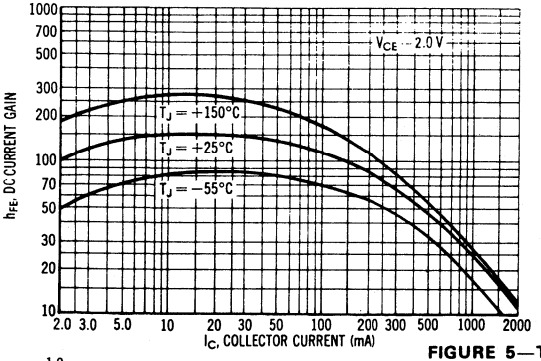


FIGURE 4—"ON" VOLTAGE

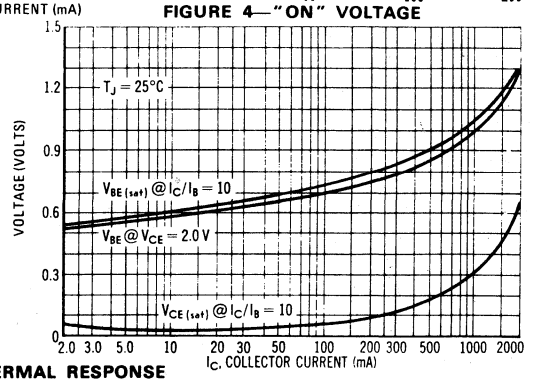
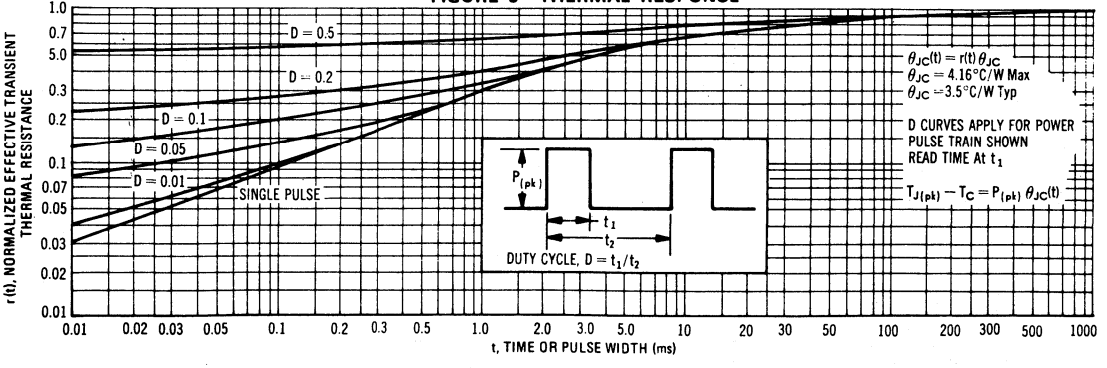


FIGURE 5—THERMAL RESPONSE



BD185
BD187 • BD189

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

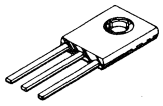
. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.5 Adc
- BD 185, 187, 189 are complementary with BD 186, 188, 190

4 AMPERE
POWER TRANSISTOR

NPN SILICON

30, 45, 60 VOLTS
40 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 185 BD 187 BD 189	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 185 BD 187 BD 189	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

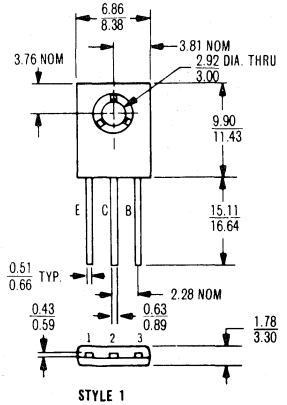
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 185 BD 187 BD 189	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 185 BD 187 BD 189	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 2Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 2Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1
Pin 1. Emitter
2. Collector
3. Base

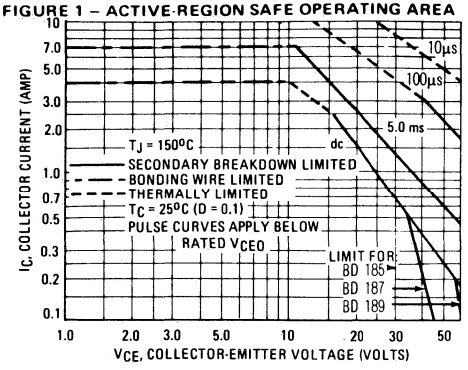
When mounting the device, torque not to exceed 0.01 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

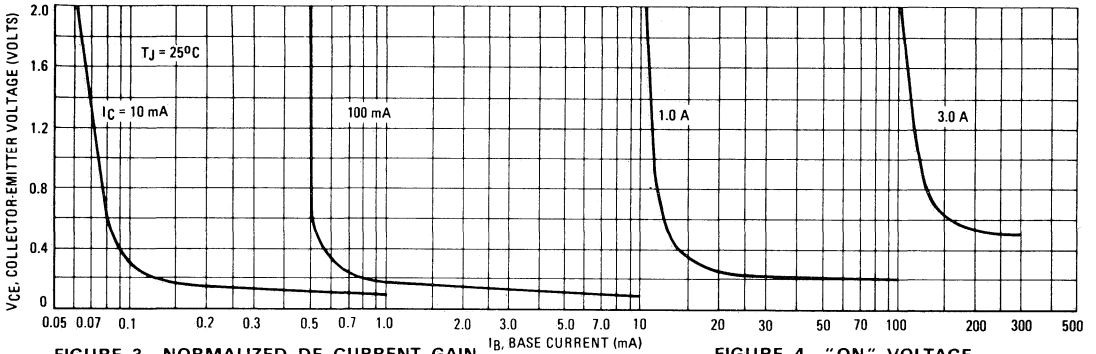


FIGURE 3—NORMALIZED DE CURRENT GAIN

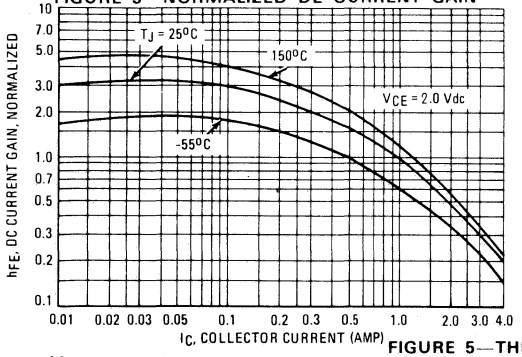


FIGURE 4—"ON" VOLTAGE

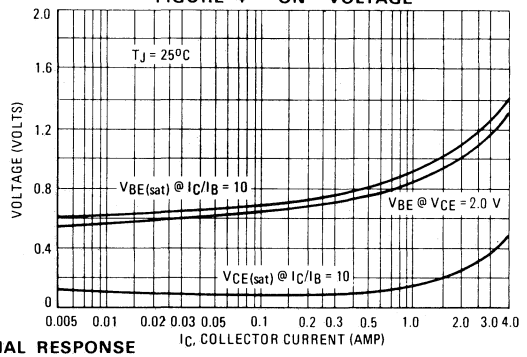
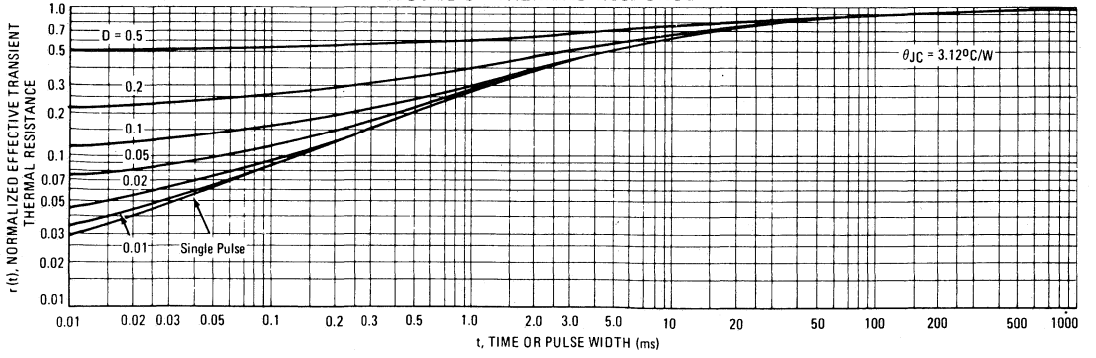


FIGURE 5—THERMAL RESPONSE



BD186
BD188 • BD190

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

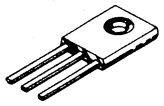
. . . designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 40 (Min) @ I_C = 0.5 Adc
- BD 186, 188, 190 are complementary with BD 185, 187, 189

4 AMPERE
POWER TRANSISTOR

PNP SILICON

30, 45, 60 VOLTS
40 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 186 BD 188 BD 190	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 186 BD 188 BD 190	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	°C

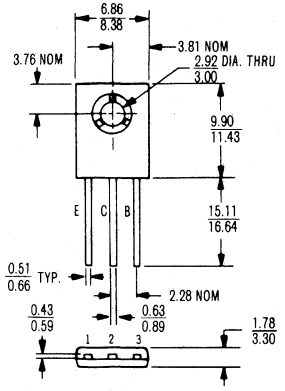
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 186 BD 188 BD 190	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 186 BD 188 BD 190	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2 A, V_{CE} = 2 V)	h_{FE}*		40 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.5	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs. Duty Cycle ≦ 2.0%.



STYLE 1
Pin 1. Emitter
2. Collector
3. Base

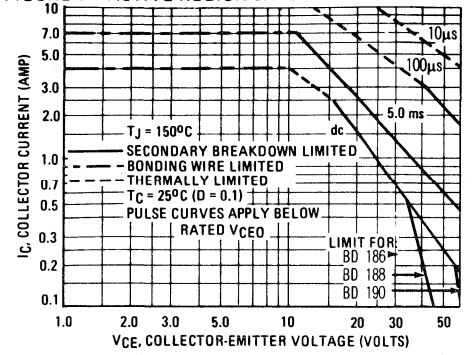
When mounting the device, torque not to exceed 0.01 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

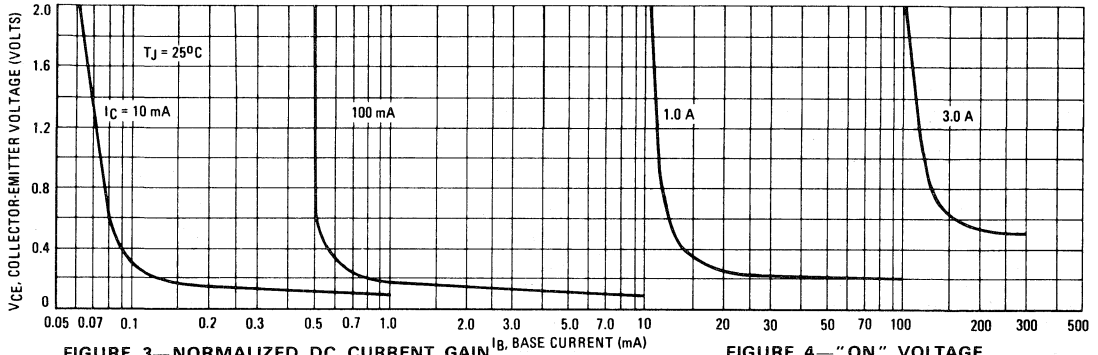


FIGURE 3—NORMALIZED DC CURRENT GAIN

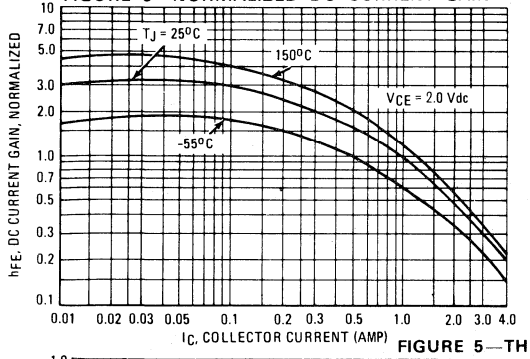


FIGURE 4—"ON" VOLTAGE

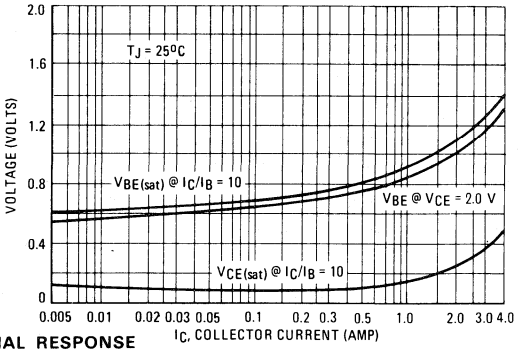
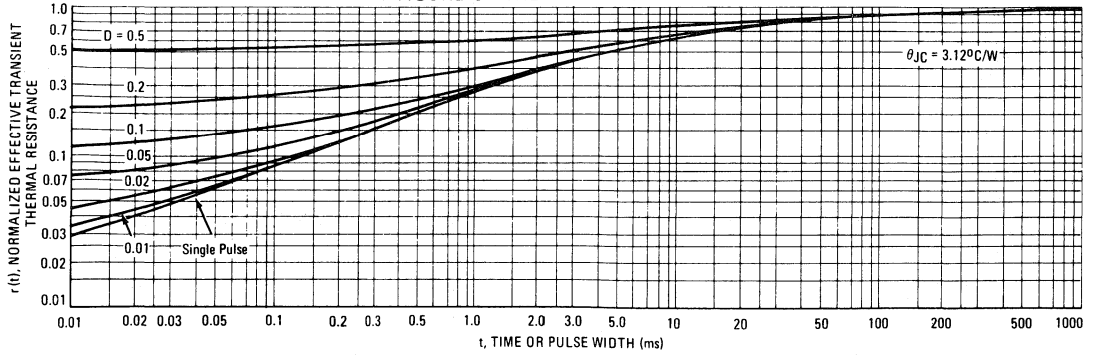


FIGURE 5—THERMAL RESPONSE



BD195
BD197 • BD199

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 30 (Min) @ I_C = 1.15 Adc
- BD 195, 197, 199 are complementary with BD 196, 198, 200

6 AMPERE
POWER TRANSISTOR

NPN SILICON

30, 45, 60 VOLTS
65 WATTS

HARDWARE AVAILABLE:
1. MICA WASHER—148 52600 F03
2. LOCK WASHER—04A 52200 F02

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 195 BD 197 BD 199	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 195 BD 197 BD 199	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		6.0	Adc
Base Current	I_B		2.5	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

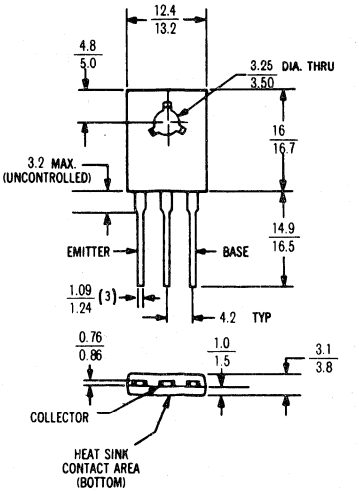
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 195 BD 197 BD 199	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 195 BD 197 BD 199	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs. Duty Cycle ≦ 2.0%.



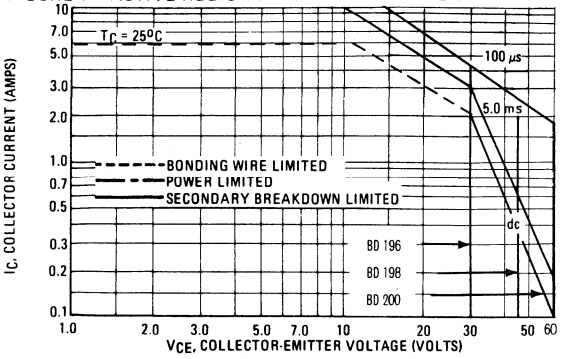
When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 90

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

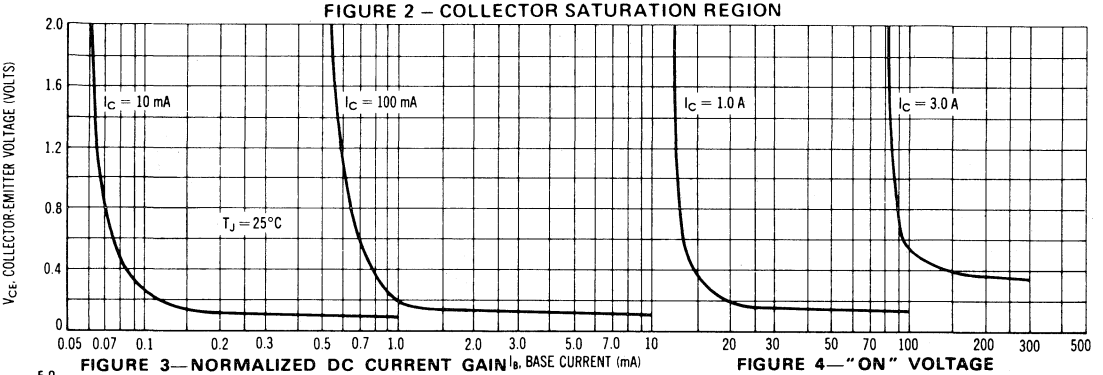


FIGURE 3—NORMALIZED DC CURRENT GAIN

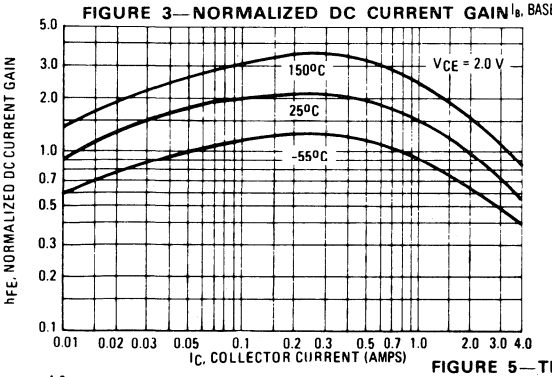


FIGURE 4—"ON" VOLTAGE

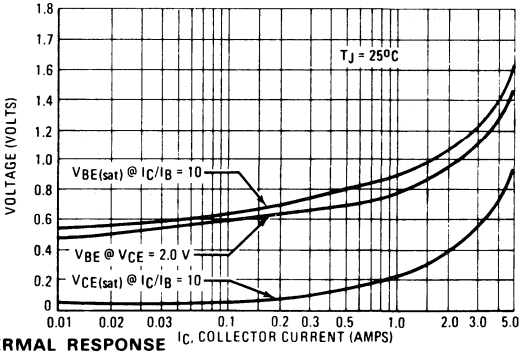
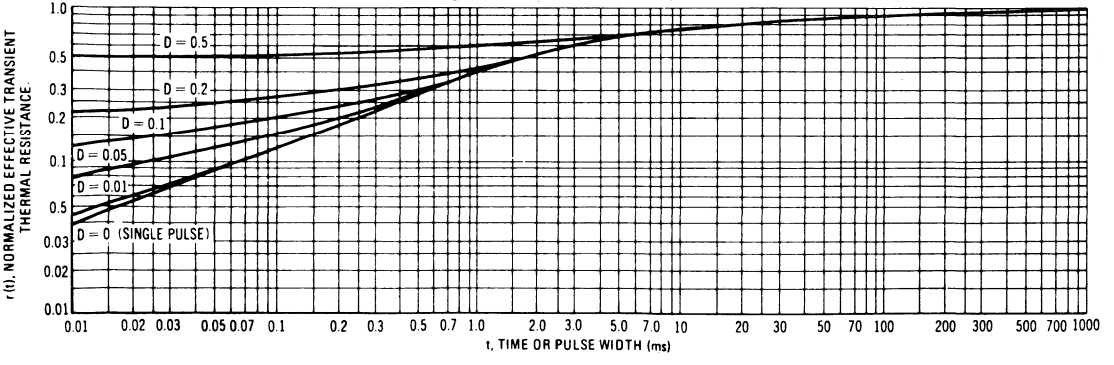


FIGURE 5—THERMAL RESPONSE



BD196
BD198 • BD200

PLASTIC HIGH POWER
SILICON PNP TRANSISTOR

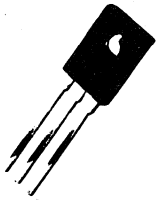
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 1 Adc
- BD 196, 198, 200 are complementary with BD 195, 197, 199

6 AMPERE
POWER TRANSISTOR

PNP SILICON

30, 45, 60 VOLTS
65 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F02

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 196 BD 198 BD 200	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 196 BD 198 BD 200	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		6.0	Adc
Base Current	I_B		2.5	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

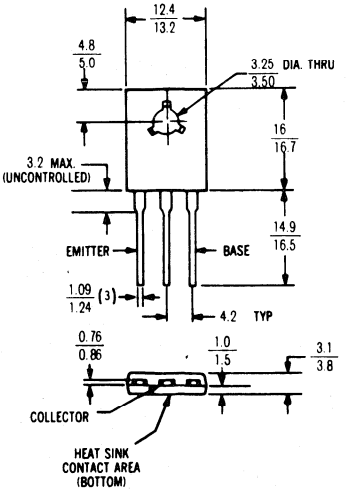
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 196 BD 198 BD 200	30 45 60	— — —	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 196 BD 198 BD 200	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.



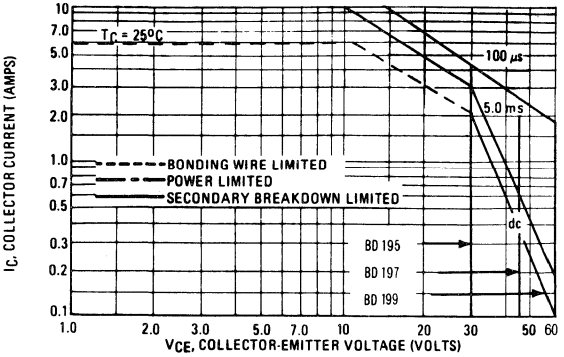
When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 90

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

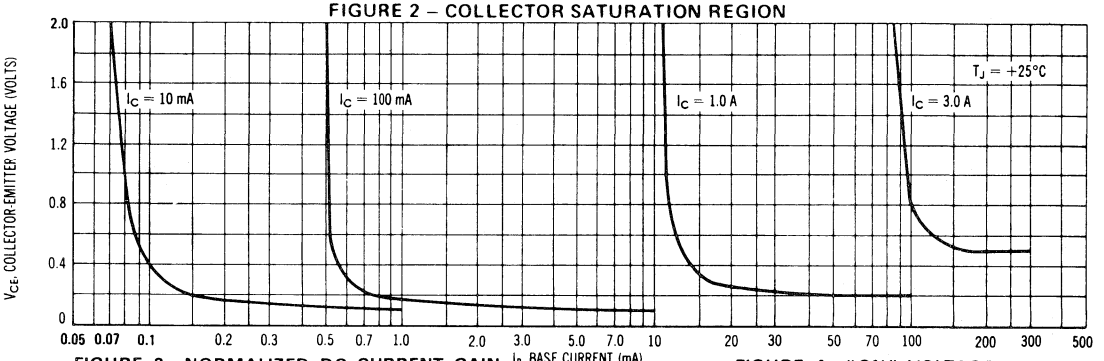


FIGURE 3—NORMALIZED DC CURRENT GAIN

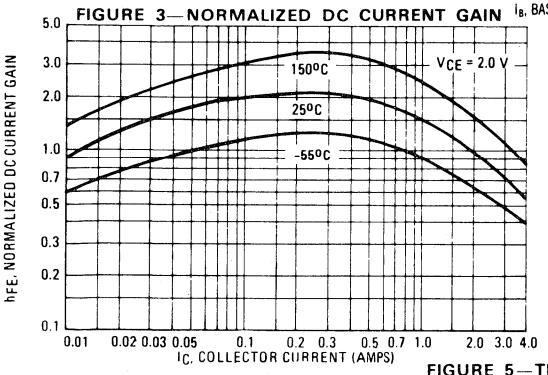


FIGURE 4—"ON" VOLTAGE

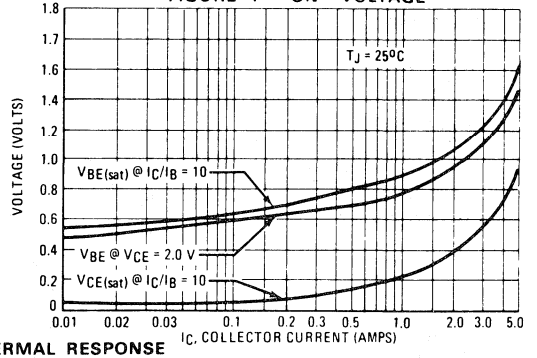
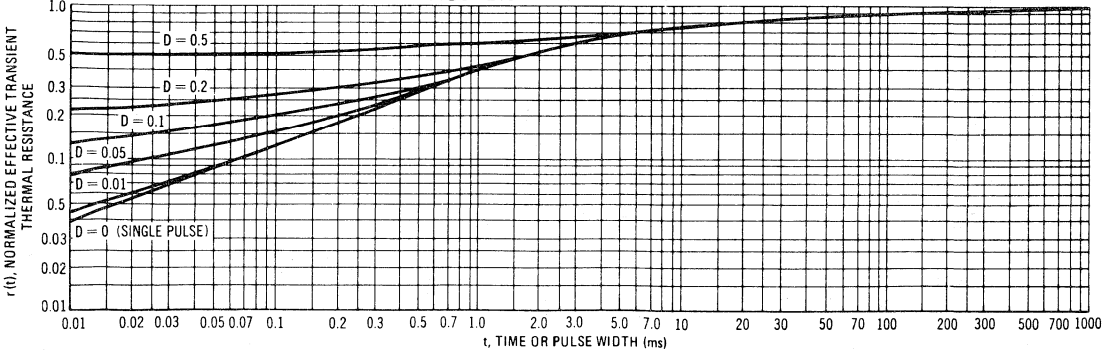


FIGURE 5—THERMAL RESPONSE



BD205
BD207

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 205, 207 are complementary with BD 206, 208

10 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60 VOLTS
90 WATTS

HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F02

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 205 BD 207	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 205 BD 207	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

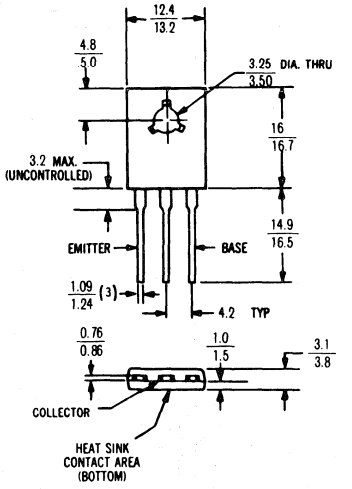
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD 205 BD 207	45 60	— —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 205 BD 207	— —	1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 90

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

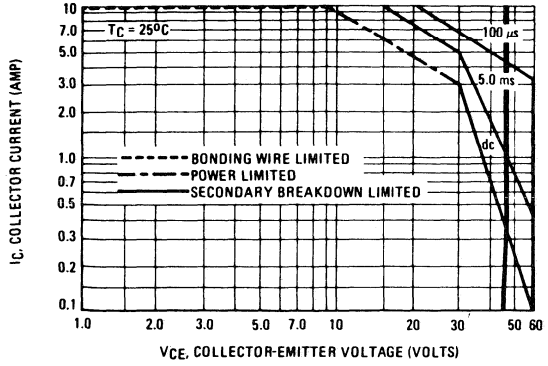


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

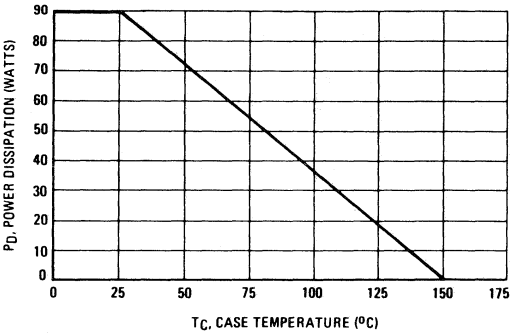


FIGURE 3 — "ON" VOLTAGES

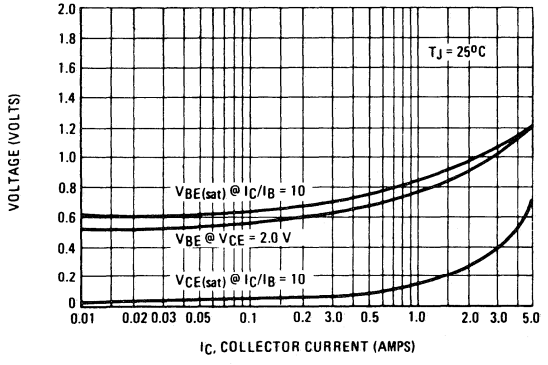


FIGURE 4 — CURRENT GAIN

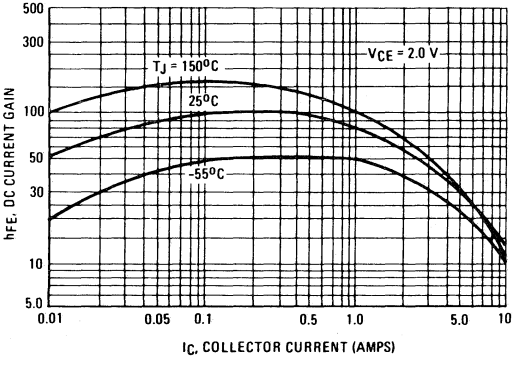
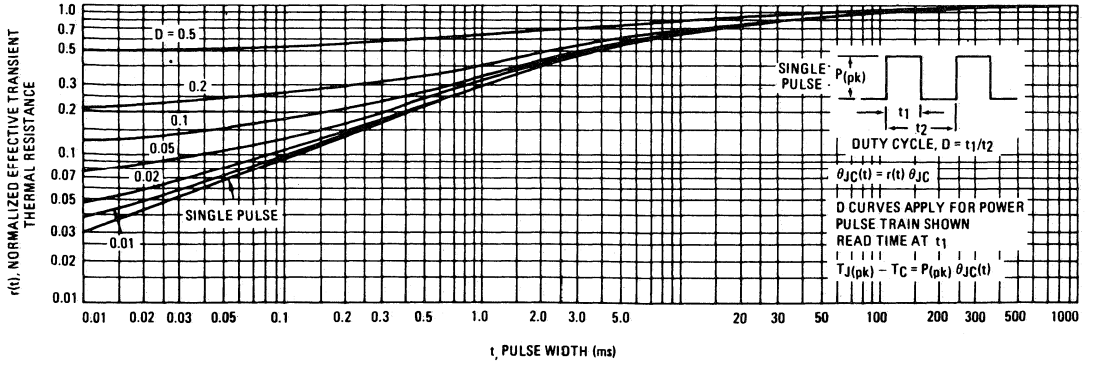


FIGURE 5 — THERMAL RESPONSE



BD206
BD208

PLASTIC HIGH POWER
SILICON PNP TRANSISTOR

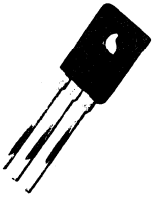
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 206, 208 are complementary with BD 205, 207

10 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60 VOLTS
90 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—148 52600 F03
2. LOCK WASHER—04A 52200 F02

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 206 BD 208	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 206 BD 208	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

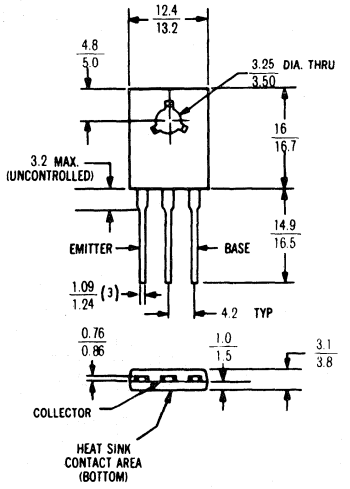
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD 206 BD 208	45 60	— —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	BD 206 BD 208	— —	1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 90

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

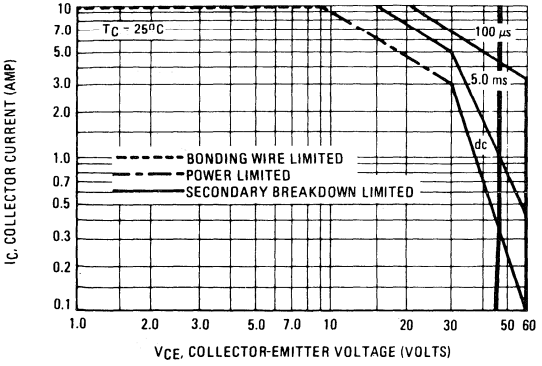


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

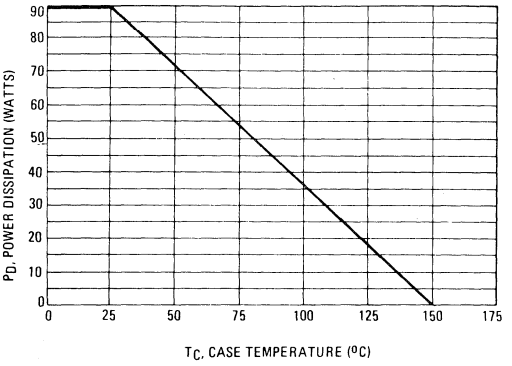


FIGURE 3 — "ON" VOLTAGES

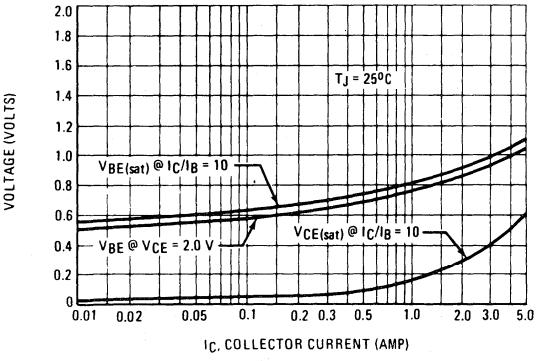


FIGURE 4 — CURRENT GAIN

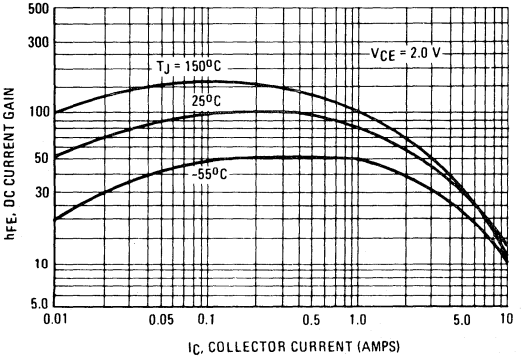
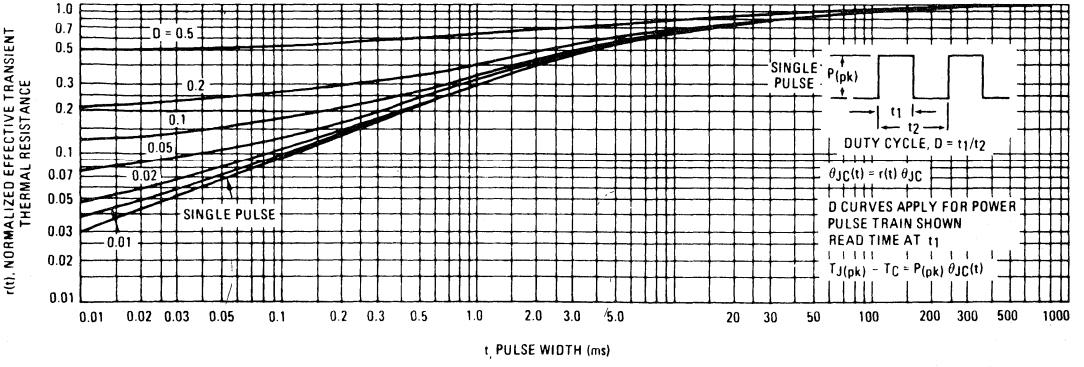


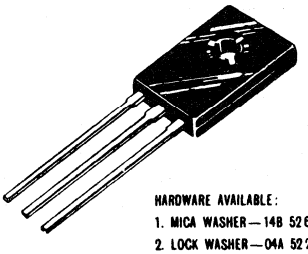
FIGURE 5 — THERMAL RESPONSE



NPN SILICON MEDIUM POWER TRANSISTORS

- For Power Ouput Stages and Line Driver in Television Receivers

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON



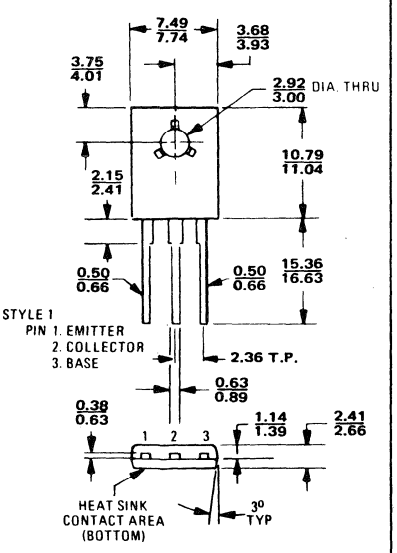
HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}		300	Vdc
Collector-Emitter Voltage	V_{CES}		500	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		0.5	Adc
Base Current	I_B		0.25	Adc
Total Device Dissipation $T_C = 25^o$ C Derate above 25° C	P_D		20 160	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{Stg}		−55 to +150	°C

THERMAL CHARACTERISTICS

	Symbol		Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}		6.25	°C/W



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-03

ELECTRICAL CHARACTERISTICS ($T_C = 25^o$ C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
Collector Emitter Sustaining Voltage ($I_C = 10$ mA, $I_B = 0$)	$V_{CEO\ (SUS)}$	300		Vdc
Collector Cuttof Current ($V_{CE} = 500$ v, $V_{BE} = 0$)	I_{CES}		0.1	mAdc
Base – Emitter Voltage ($V_{CE} = 5$ v, $I_C = 150$ mA)	V_{BE}		1.0	Vdc
DC Current Gain ($V_{CE} = 5$ v, $I_C = 50$ mA) ($V_{CE} = 5$ v, $I_C = 150$ mA)	h_{FE}	25 20	150	
Collector Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA)	$V_{CE\ (SAT)}$		1.0	Vdc

BD233
BD235 • BD237

PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR

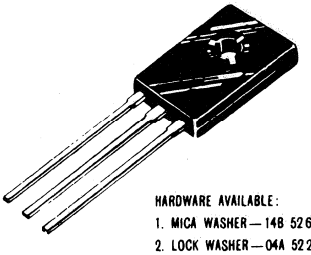
. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 233, 235, 237 are complementary with BD 234, 236, 238

2 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
25 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		55 to +150	°C

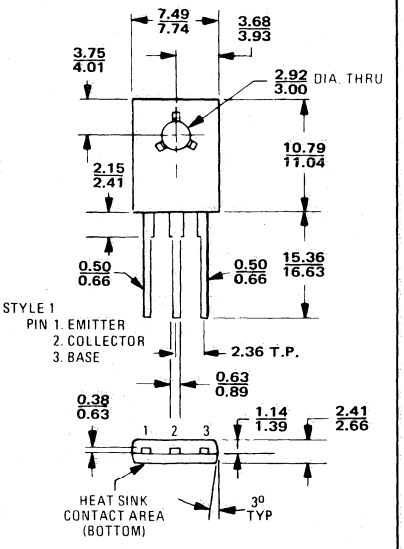
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5.0	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 233 BD 235 BD 237	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 233 BD 235 BD 237	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 1 A, V_{CE} = 2 V)	h_{FE1} h_{FE2}		40 25	— —	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



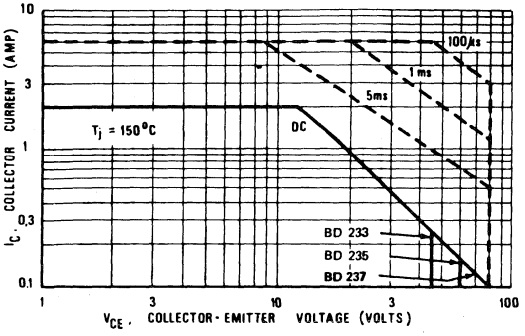
When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-03

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

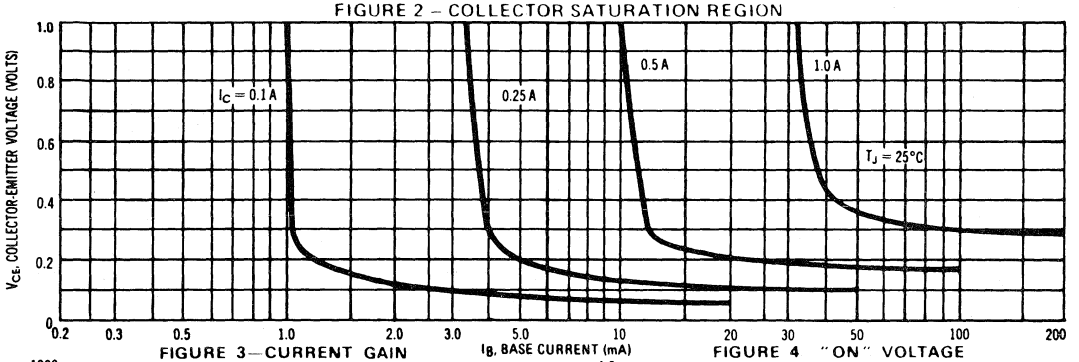


FIGURE 3—CURRENT GAIN

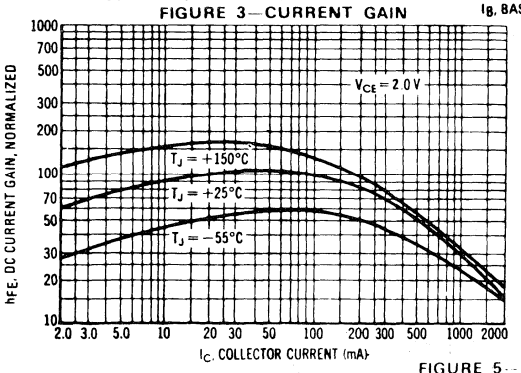


FIGURE 4 "ON" VOLTAGE

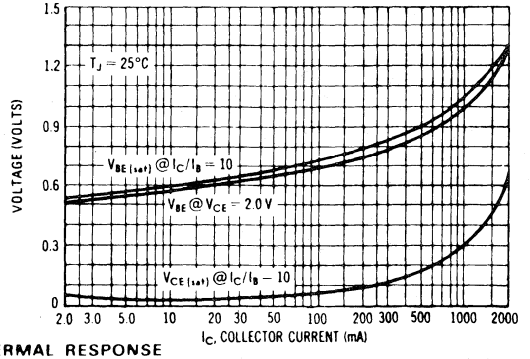
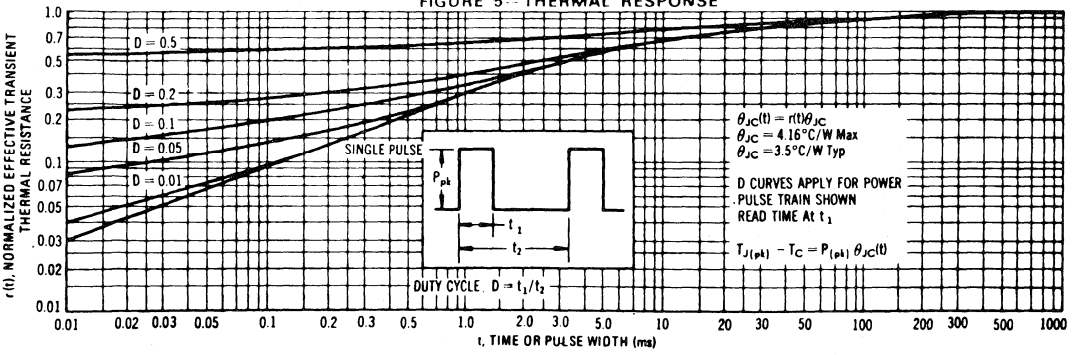


FIGURE 5 – THERMAL RESPONSE



BD234
BD236 • BD238

PLASTIC MEDIUM POWER
SILICON PNP TRANSISTOR

. . . designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 234, 236, 238 are complementary with BD 233, 235, 237

2 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
25 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation T_C=25°C	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

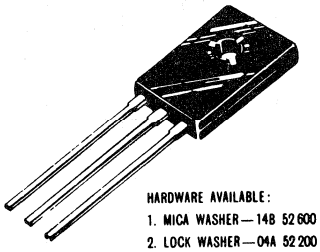
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		5.0	° C/W

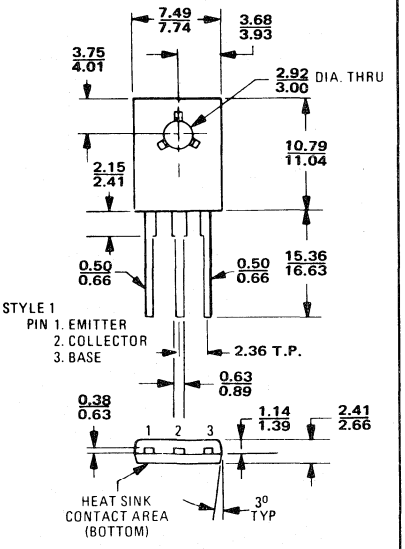
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}*	BD 234 BD 236 BD 238	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD 234 BD 236 BD 238	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 1 A, V_{CE} = 2 V)	h_{FE1} h_{FE2}		40 25	— —	
Collector-Emitter Saturation Voltage* (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$*		—	0.6	Vdc
Base-Emitter On Voltage* (I_C = 1 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.3	Vdc
Current-Gain-Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01



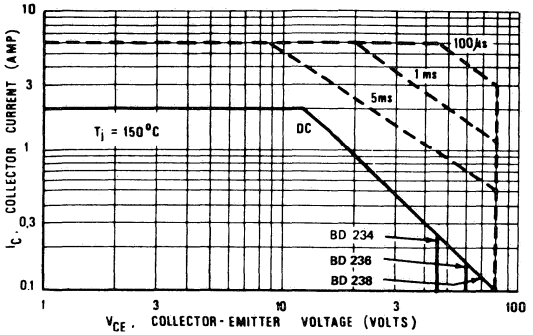
When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-03

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

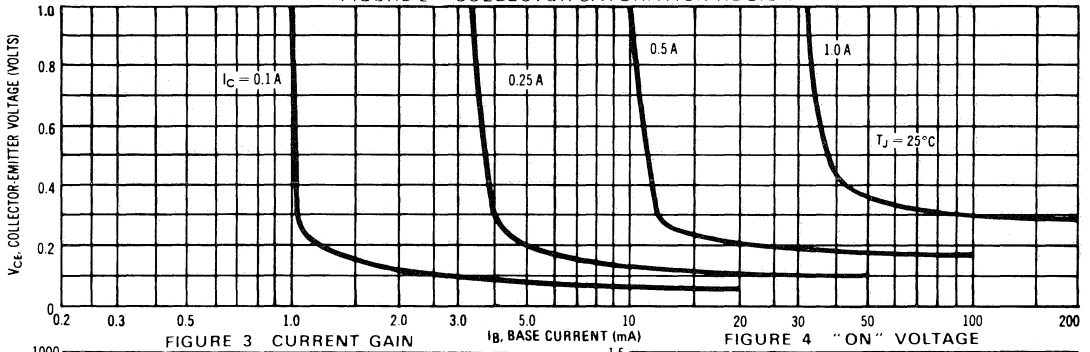


FIGURE 3 CURRENT GAIN

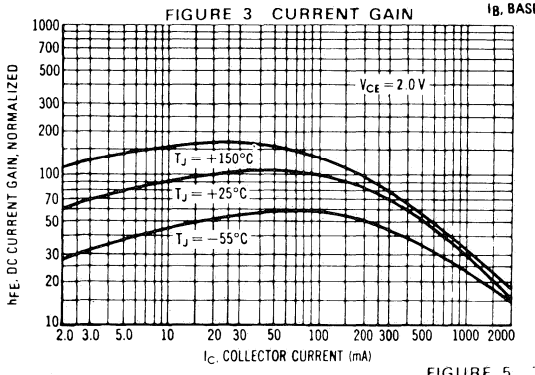


FIGURE 4 "ON" VOLTAGE

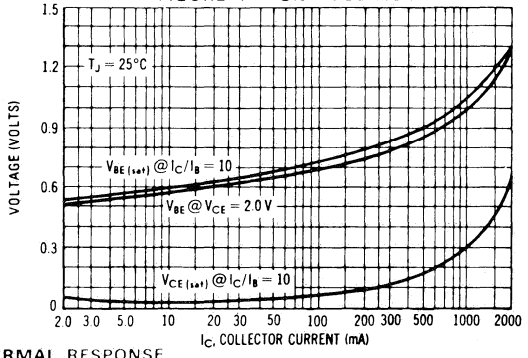
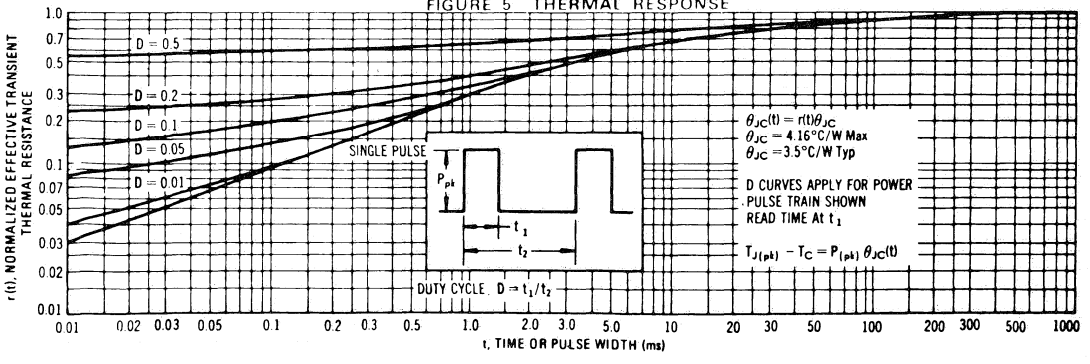


FIGURE 5 THERMAL RESPONSE



BD243, 243A, 243B, 243C
BD244, 244A, 244B, 244C

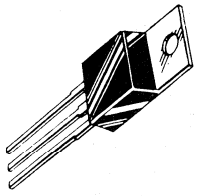
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BD243, BD244
  = 60 Vdc (Min) — BD243A, BD244A
  = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

45-60-80-100 VOLTS
65 WATTS



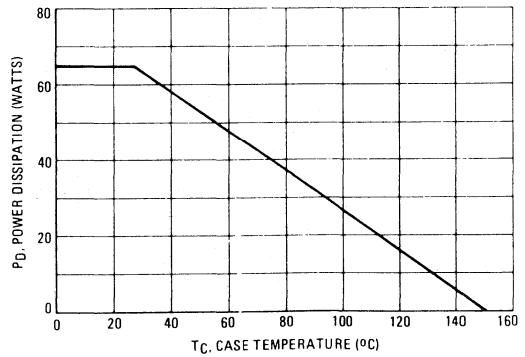
*MAXIMUM RATINGS

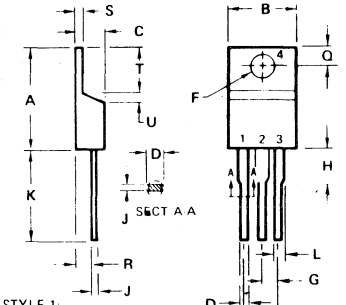
Rating	Symbol	BD243 BD244	BD243A BD244A	BD243B BD244B	BD243C BD244C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous	I_C	6				Adc
Peak		10				
Base Current	I_B	2.0				Adc
Total Device Dissipation @ T_C = 25°C	P_D	65				Watts
Derate above 25°C		0.52				W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

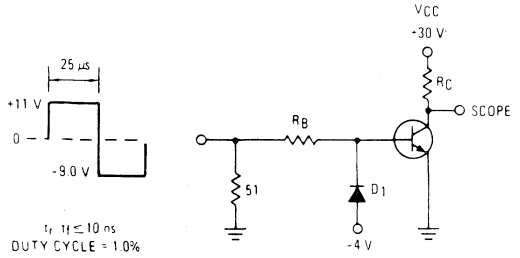
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243, BD244	$V_{CEO(sus)}$	45	–	Vdc
	BD243A, BD244A		60	–	
	BD243B, BD244B		80	–	
	BD243C, BD244C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	BD243, BD243A, BD244, BD244A		–	0.7	
(V_{CE} = 60 Vdc, I_B = 0)	BD243B, BD243C, BD244B, BD244C		–	0.7	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 45 Vdc, V_{EB} = 0)	BD243, BD244		–	400	
(V_{CE} = 60 Vdc, V_{EB} = 0)	BD243A, BD244A		–	400	
(V_{CE} = 80 Vdc, V_{EB} = 0)	BD243B, BD244B		–	400	
(V_{CE} = 100 Vdc, V_{EB} = 0)	BD243C, BD244C		–	400	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)			30	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			15	–	
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1 Adc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = h_{fe} \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5200 USED ABOVE IB = 100 mA
MSD6100 USED BELOW IB = 100 mA

FIGURE 3 – TURN-ON TIME

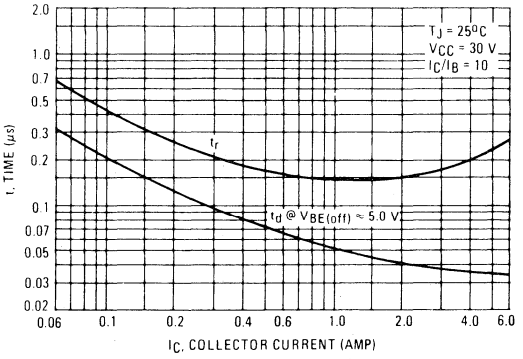


FIGURE 4 – THERMAL RESPONSE

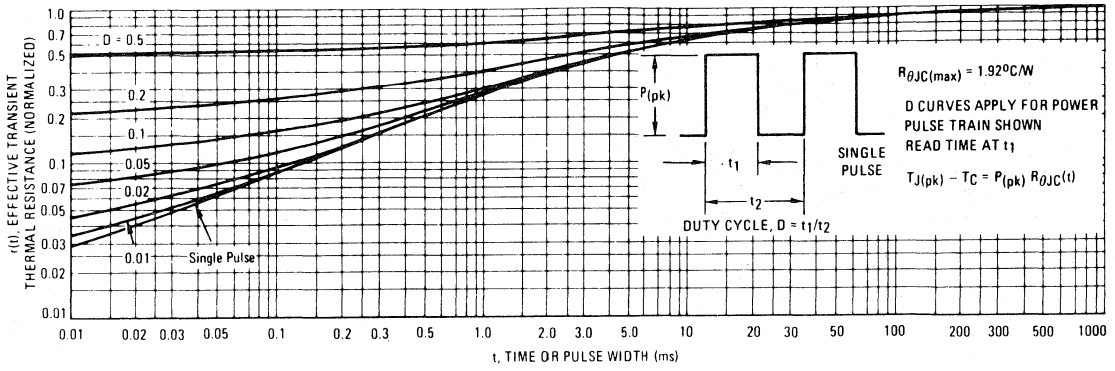
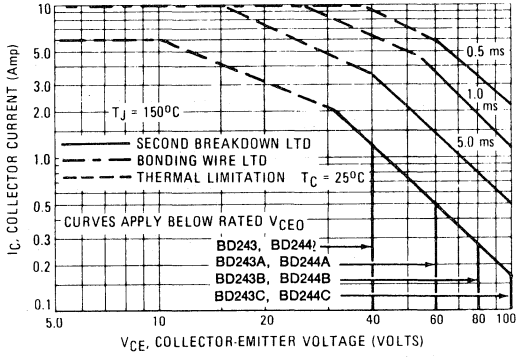


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

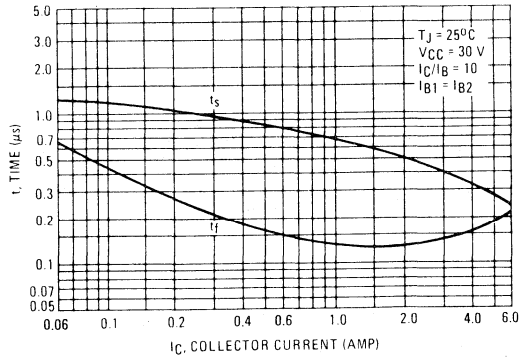


FIGURE 7 – CAPACITANCE

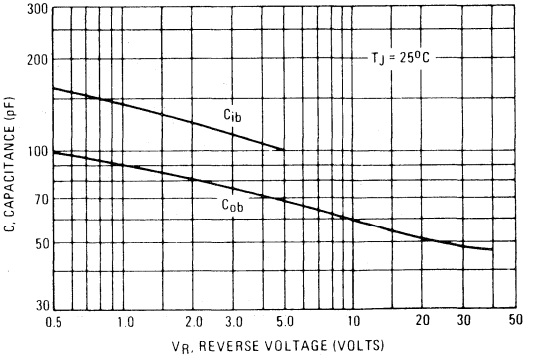


FIGURE 8 – DC CURRENT GAIN

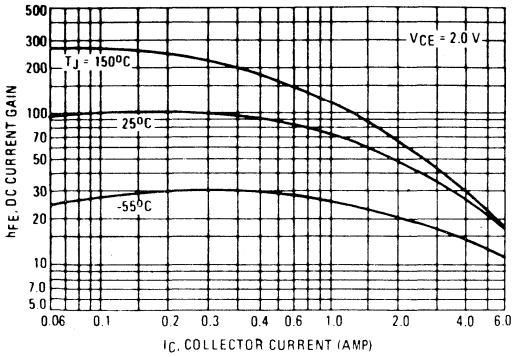


FIGURE 9 – COLLECTOR SATURATION REGION

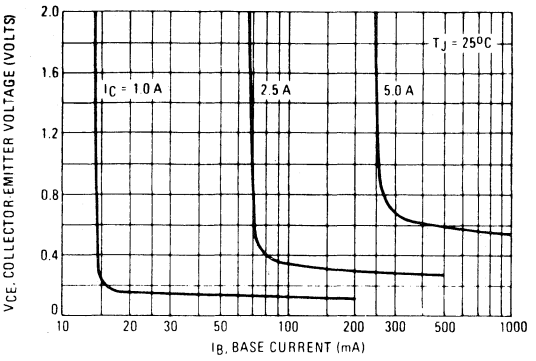


FIGURE 10 – "ON" VOLTAGES

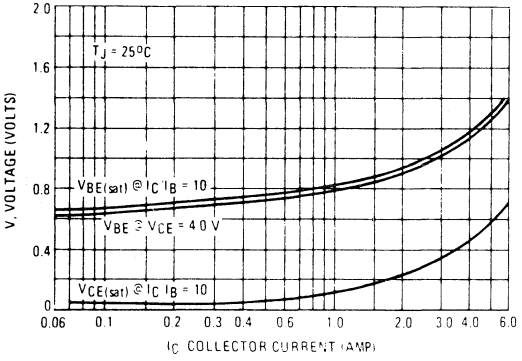


FIGURE 11 – TEMPERATURE COEFFICIENTS

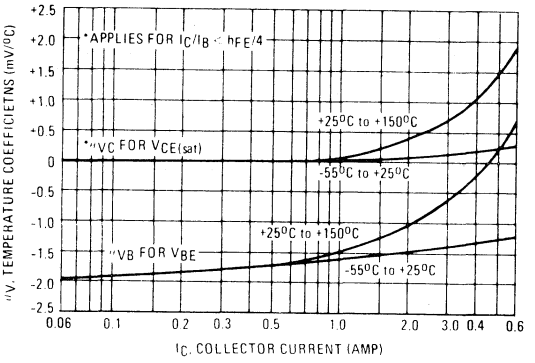


FIGURE 12 – COLLECTOR CUT-OFF REGION

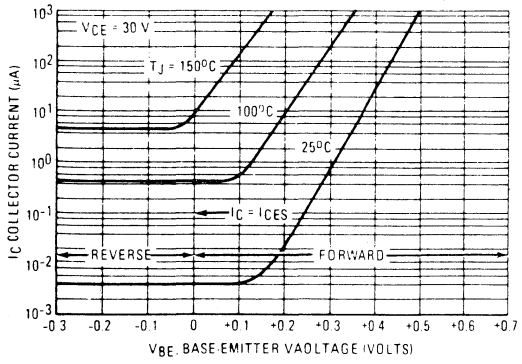
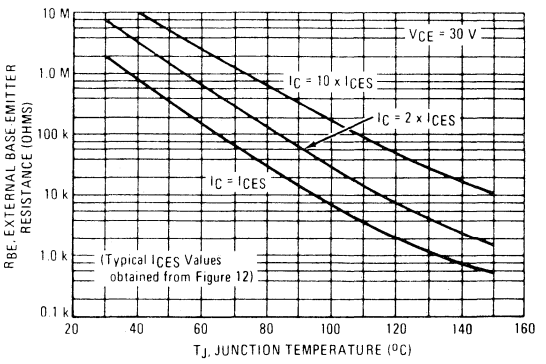


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



BD311 • BD312
BD313 • BD314

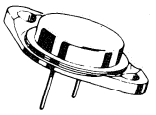
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... designed for high quality amplifiers operating up to 60 Watts into 4 ohm load with BD311, BD312 and into 8 ohm load with BD313, BD314.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical $f_T = 4.0$ MHz @ $I_C = 0.5$ A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
150 WATTS



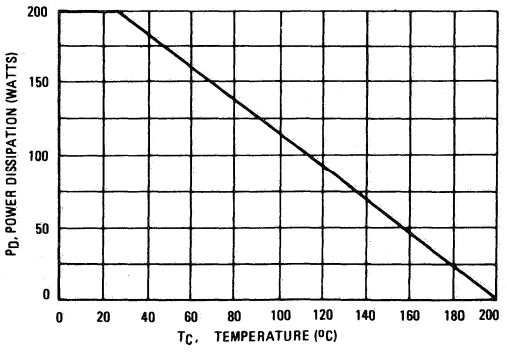
MAXIMUM RATINGS

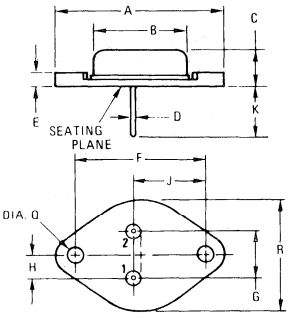
Rating	Symbol	BD311 BD312	BD313 BD314	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	150 0.857		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^oC/W$

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

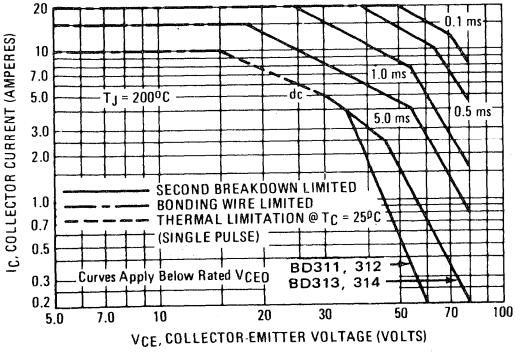
CASE 11 (TO-3)

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	BD311, BD312 BD313, BD314	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain I_C = 4.0 Adc, V_{CE} = 4.0 Vdc I_C = 5.0 Adc, V_{CE} = 4.0 Vdc I_C = 10 Adc, V_{CE} = 4.0 Vdc	 BD313, BD314 BD311, BD312 All Types	h_{FE}	 25 25 5		—
Collector-Emitter Saturation Voltage I_C = 5.0 Adc, I_B = 0.5 Adc		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage I_C = 5.0 Adc, I_B = 0.5 Adc		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage I_C = 5.0 Adc, V_{CE} = 4.0 Vdc		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	—	MHz

(1) Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\geq$ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ <200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP DEVICES
BD312 and BD314

NPN DEVICES
BD311 and BD313.

FIGURE 3 — DC CURRENT GAIN

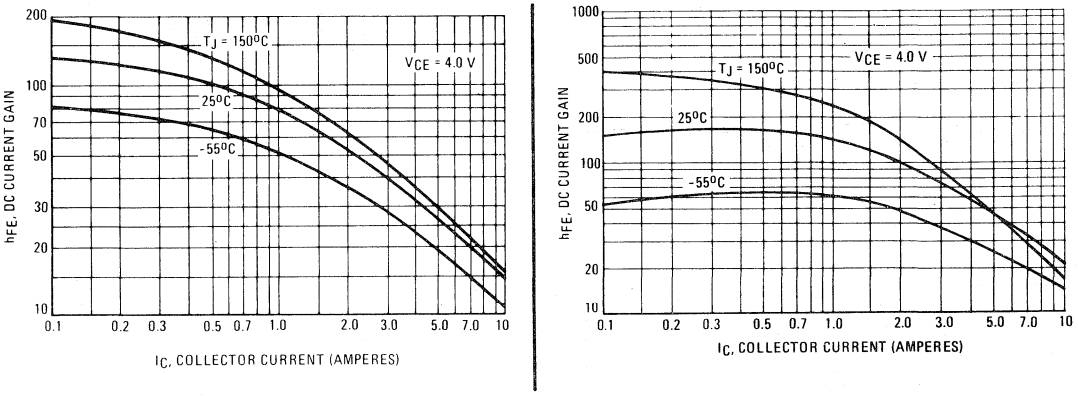
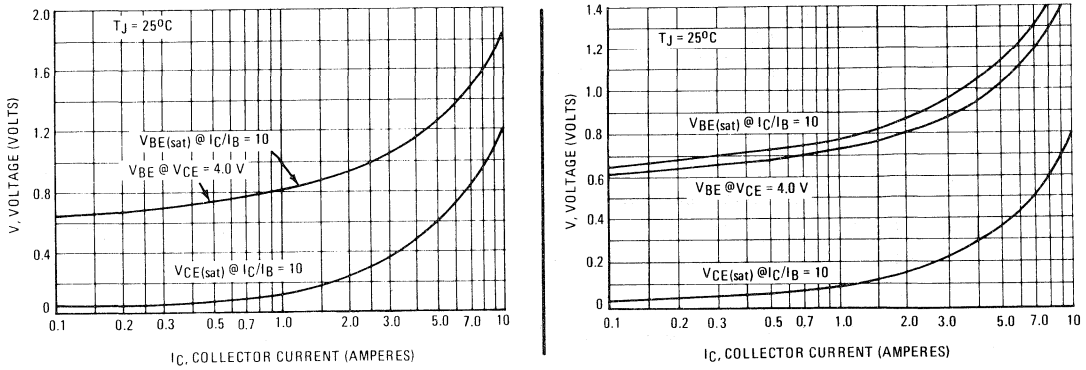


FIGURE 4 — "ON" VOLTAGES



BD315 • BD316
BD317 • BD318

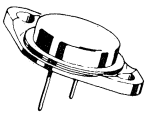
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... designed for high quality amplifiers operating up to 100 Watts into 4 ohm load with BD315, BD316 and into 8 ohm load with BD317, BD318.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical f_T = 2.0 MHz @ I_C = 1.0 A

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

80-100 VOLTS 200 WATTS



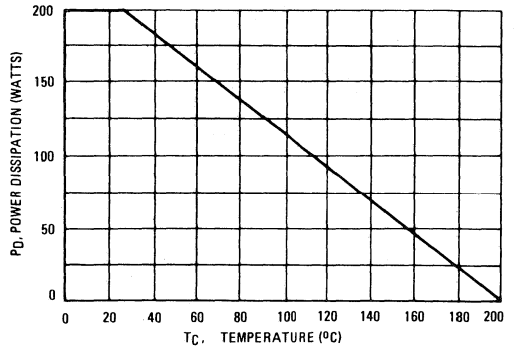
MAXIMUM RATINGS

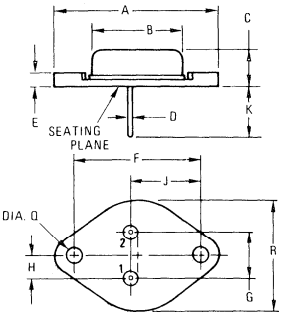
Rating	Symbol	BD315 BD316	BD317 BD318	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	200 1.14		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^oC/W$

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

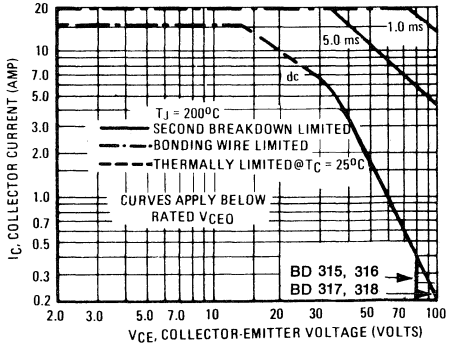
CASE 11 (TO-3)

*** ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	BD315, BD316 BD317, BD318	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain I_C = 5.0 Adc, V_{CE} = 4.0 Vdc I_C = 8.0 Adc, V_{CE} = 4.0 Vdc I_C = 10 Adc, V_{CE} = 4.0 Vdc	 BD317, BD318 BD315, BD316 All Types	h_{FE}	 25 25 15		—
Collector-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc		$V_{CE(sat)}$	—	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ <200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP DEVICES
BD316 and BD318

NPN DEVICES
BD315 and BD317

FIGURE 3 — DC CURRENT GAIN

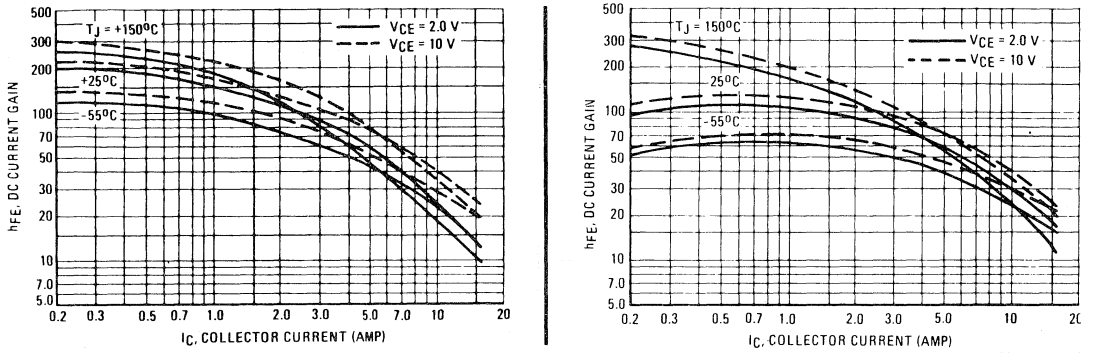
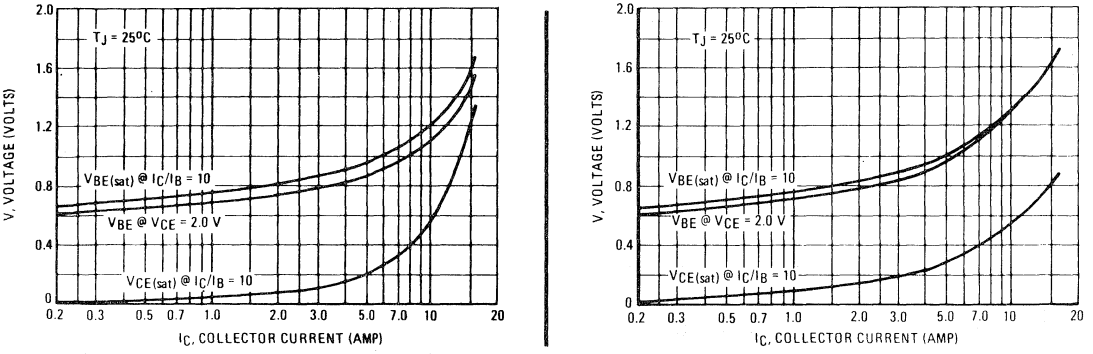


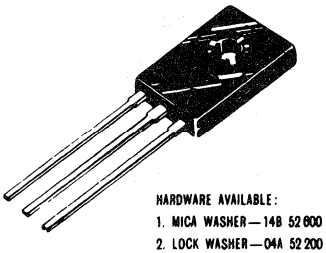
FIGURE 4 — "ON" VOLTAGES



NPN PLANAR SILICON MEDIUM-POWER TRANSISTORS

- Silicon replacement for Germanium AD161
- BD361, 361A are complementary to BD362, BD362A
- P_D of 15 W with T_j of 150 °C
- Case 77 package is Pin compatible with SOT-9
- F_T minimum 50 MHz

4 AMPERE
POWER TRANSISTOR
NPN SILICON
20 VOLTS
15 WATTS



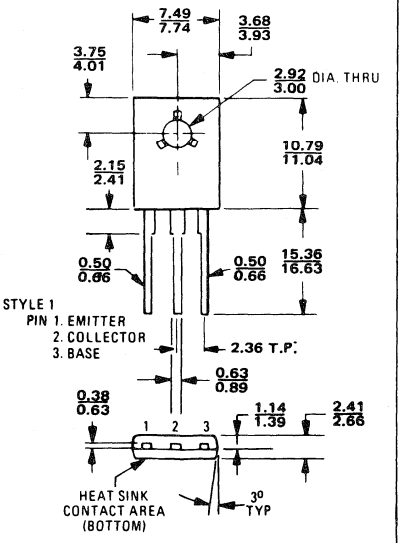
HARDWARE AVAILABLE:
1. MICA WASHER—14B 52 600 F03
2. LOCK WASHER—04A 52 200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD361 BD361A	20 20	Vdc
Collector-Base Voltage	V_{CBO}	BD361A BD361	32 32	Vdc
Emitter-Base Voltage	V_{EBO}		8	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25°$ C Derate above 25° C	P_D		15 120	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150	° C

THERMAL CHARACTERISTICS

	Symbol		Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}		8.35	° C/W



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

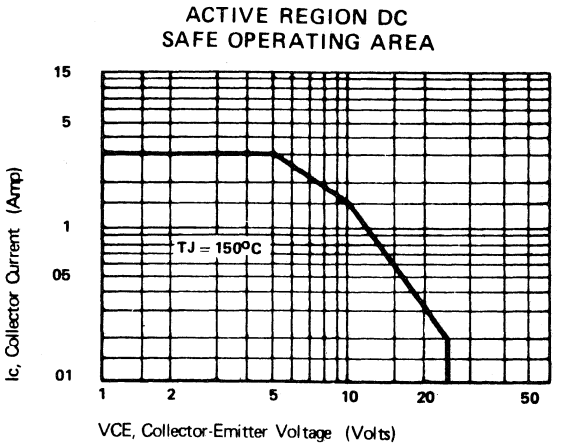
All dimensions in millimeters

CASE 77-03

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	20	—	Vdc
Collector Cutoff Current (V_{CB} = 32 V, I_E = 0) (V_{CB} = 32 V, I_E = 0, T_J = 150° C)	I_{CBO}	— —	0.2 1.0	μAdc mAdc
Emitter Cutoff Current (V_{EB} = 8 V, I_C = 0)	I_{EBO}	—	0.1	mAdc
DC Current Gain (I_C = 50 m A V_{CE} = 1 V)* BD361/A (I_C = 500 m A V_{CE} = 1 V)* BD361/A (I_C = 2.0 A V_{CE} = 1 V)* BD361 (I_C = 2.0 A V_{CE} = 1 V)* BD361A	h_{FE}	— 40 80 25 50	— 300 320 — —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 A, I_B = 20 m A)*	$V_{CE(sat)}$	—	0.8	Vdc
Base-Emitter On Voltage (I_C = 2.0 A V_{CE} = 1 V)*	$V_{BE(on)}$	—	1.5	Vdc
Current-Gain bandwidth product (I_C = 0.1 A, V_{CE} 10 V, f = 1MHz)	f_T	50		MHz

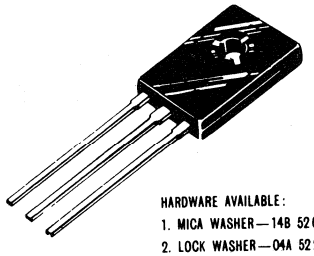
* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



PNP PLANAR SILICON MEDIUM-POWER TRANSISTORS

- Silicon replacement for Germanium AD162
- BD362, 362A are complementary to BD361, BD361A
- P_D of 15W T_j of 150 °C
- Case 77 package is Pin compatible with SOT-9
- F_T minimum 50 MHz

4 AMPERE
POWER TRANSISTOR
PNP SILICON
20 VOLTS
15 WATTS



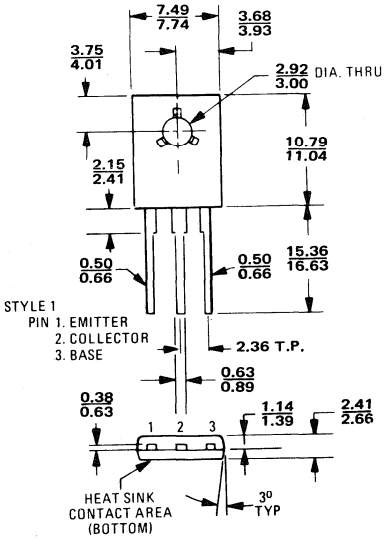
HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD362 BD362A	20 20	Vdc
Collector-Base Voltage	V_{CBO}	BD362 BD362A	32 32	Vdc
Emitter-Base Voltage	V_{EBO}		10	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25°$ C Derate above 25° C	P_D		15 120	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—65 to +150	° C

THERMAL CHARACTERISTICS

	Symbol		Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}		8.35	° C/W



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

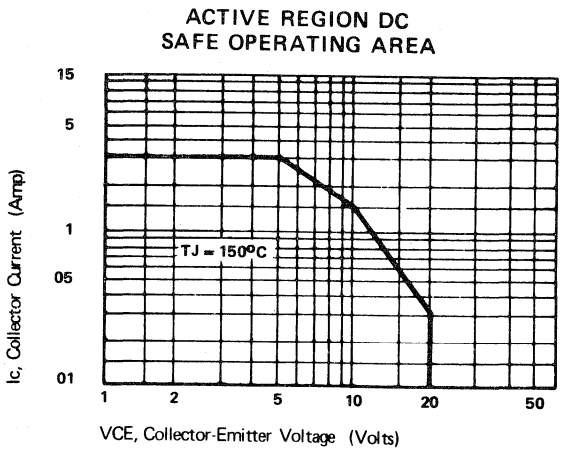
All dimensions in millimeters

CASE 77-03

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	20	—	Vdc
Collector Cutoff Current (V_{CB} = 32 V, I_E = 0) (V_{CB} = 32 V, I_E = 0, T_J = 150° C)	I_{CBO}	— —	0.2 1.0	μAdc mAdc
Emitter Cutoff Current (V_{EB} = 10 V, I_C = 0)	I_{EBO}	—	0.1	mAdc
DC Current Gain (I_C = 5 mA V_{CE} = 10 V) BD362/A (I_C = 50 mA V_{CE} = 1 V)* BD362/A (I_C = 500 mA V_{CE} = 1 V)* BD362/A (I_C = 2.0 A V_{CE} = 1 V)* BD362 (I_C = 2.0 A V_{CE} = 1 V)* BD362A	h_{FE}	 55 70 80 25 50	 — 300 320 — —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 A, I_B = 20 mA)*	$V_{CE(sat)}$	—	0.6	Vdc
Base-Emitter On Voltage (I_C = 2.0 A V_{CE} = 1 V)*	$V_{BE(on)}$	—	1.2	Vdc
Current-Gain Bandwidth Product (I_C = 0.1 A, V_{CE} 10 V, f = 1 MHz)	f_T	50		MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



BD364, BD366, BD368 (NPN)
BD365, BD367, BD369 (PNP)

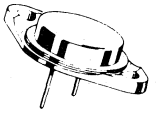
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for high quality amplifiers operating up to 100 Watts into 4 ohm load in regular complementary operation or up to several hundred watts in 4 or 8 ohms in series connected mode

- High DC Current Gain $h_{FE\ min.}$ = 20 @ I_C = 10 A
- Excellent Safe Operating Area
- High Current Gain – Bandwidth Product:
  f_T = 4.0 MHz @ I_C = 1.0 A
- Low Collector-Emitter Saturation Voltage:
  $V_{CE\ sat}$ = 1 Vdc (max.) @ 10 A

20 AMPERES
COMPLEMENTARY SILICON
POWER TRANSISTORS

50, 60, 80 VOLTS
200 WATTS



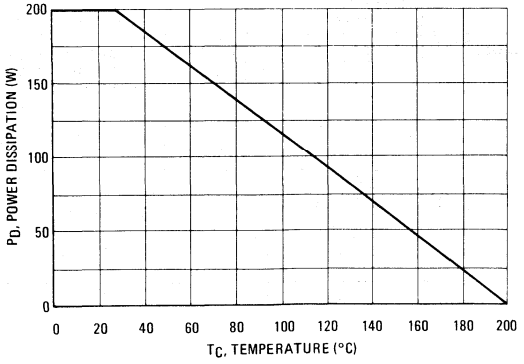
MAXIMUM RATINGS

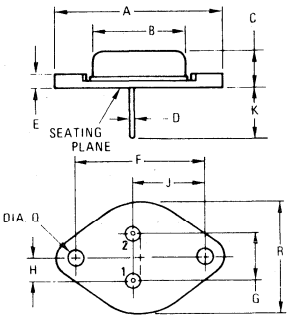
Rating	Symbol	BD364 BD365	BD366 BD367	BD368 BD369	Unit
Collector-Emitter Voltage	V_{CEO}	50	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	20 30			Adc
Base Current – Continuous	I_B	7.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

Collector connected to case

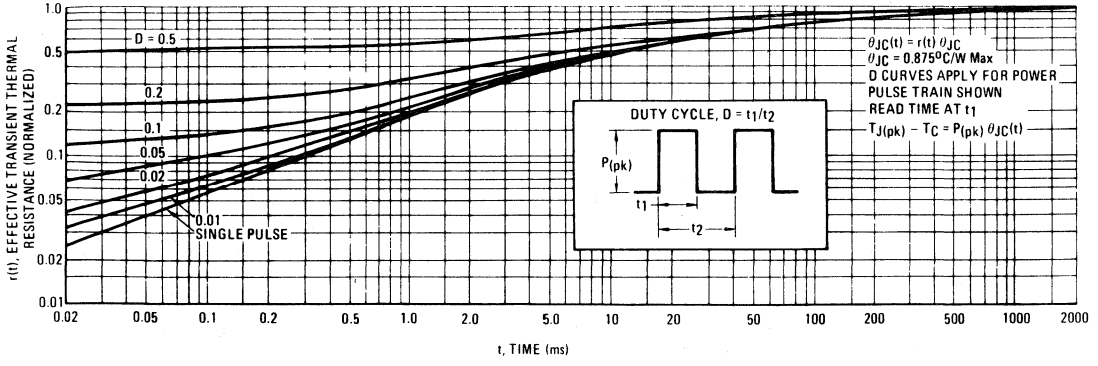
CASE 11 (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	BD364, BD365 BD366, BD367 BD368, BD369	V_{CEO} (sus)	50 60 80		Vdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTIC (1)					
DC Current Gain I_C = 5.0 Adc, V_{CE} = 4.0 Vdc I_C = 8.0 Adc, V_{CE} = 4.0 Vdc I_C = 10 Adc, V_{CE} = 4.0 Vdc	All types	H_{FE}	25 25 20		–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)		V_{CE} (sat)	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)		V_{BE} (sat)		1.8	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		V_{BE} (on)	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 1 Vdc, f_{test} = 1 MHz)		f_T	4.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$.

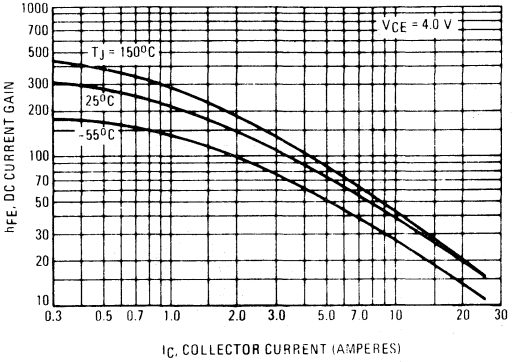
FIGURE 2 – THERMAL RESPONSE



PNP DEVICES
BD365, BD367, BD369

NPN DEVICES
BD364, BD366, BD368

FIGURE 3 – DC CURRENT GAIN



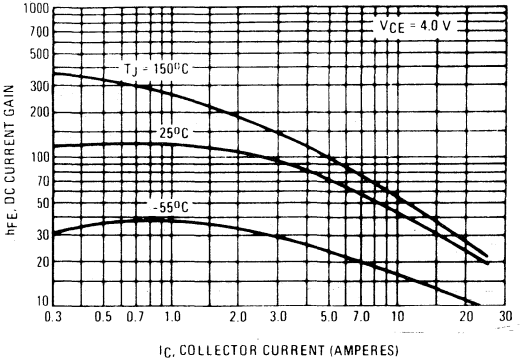
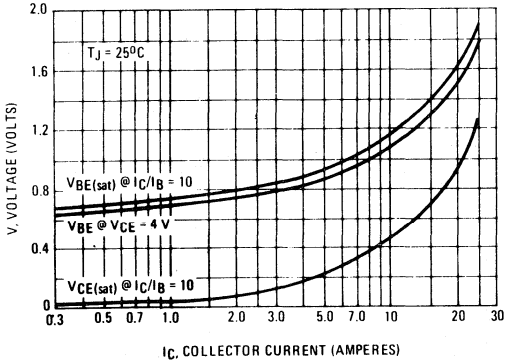


FIGURE 4 – "ON" VOLTAGES



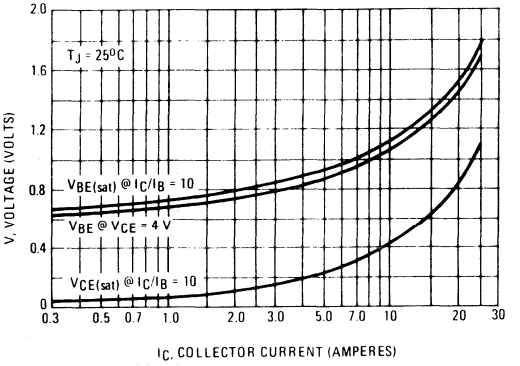
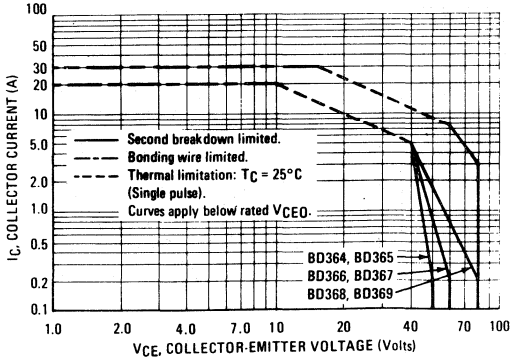


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown . Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calcualted from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Motorola Application Note AN-415).

BD385
BD387 • BD389

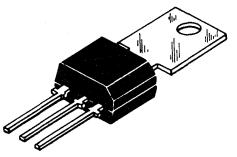
NPN SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min.) @ I_C = 1.0 mAdc – BD389
- Duowatt Package – 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to PNP BD386, BD388, BD390

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

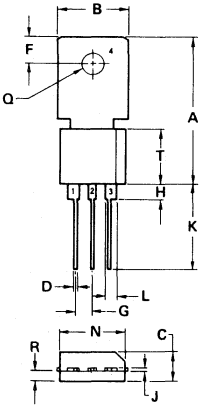
Rating	Symbol	BD385	BD387	BD389	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current – Continuous – Peak (1)	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.
(1) ≤10 ms, ≤ 50% Duty Cycle

♦Annular Semiconductors Patented by Motorola Inc.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD385	BV_{CEO}	60	–	Vdc
	BD387		80	–	
	BD389		100	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc; I_E = 0)	BD385	BV_{CBO}	60	–	Vdc
	BD387		80	–	
	BD389		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD385		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD387		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD389		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	75	250	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	18	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

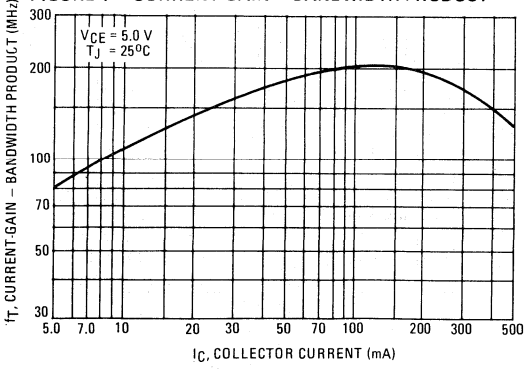
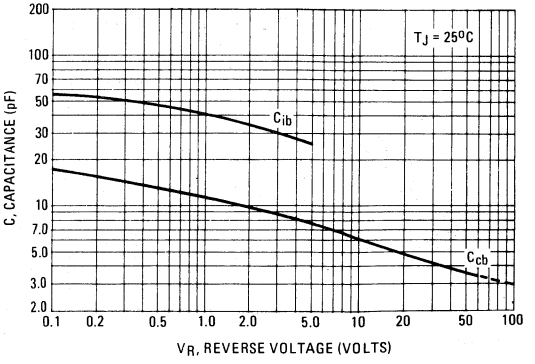


FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

FIGURE 3 – DC CURRENT GAIN

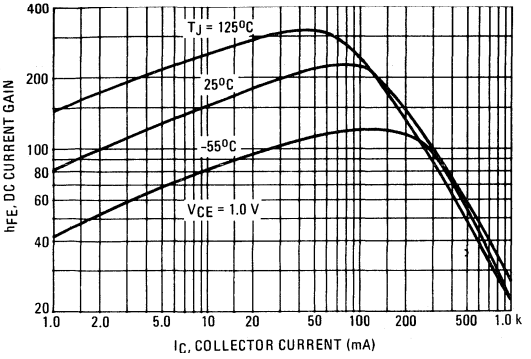


FIGURE 4 – "ON" VOLTAGE

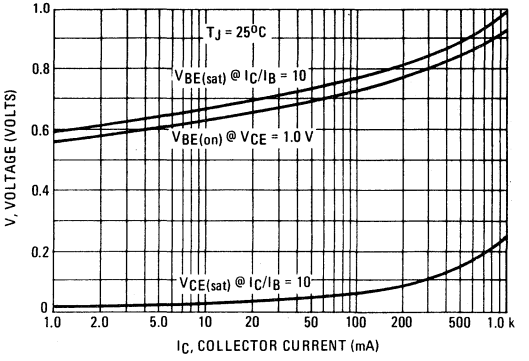


FIGURE 5 – COLLECTOR SATURATION REGION

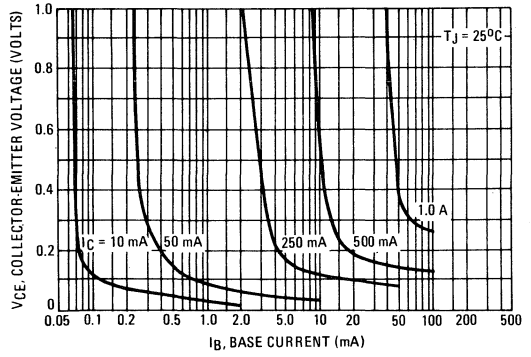


FIGURE 6 – TEMPERATURE COEFFICIENTS

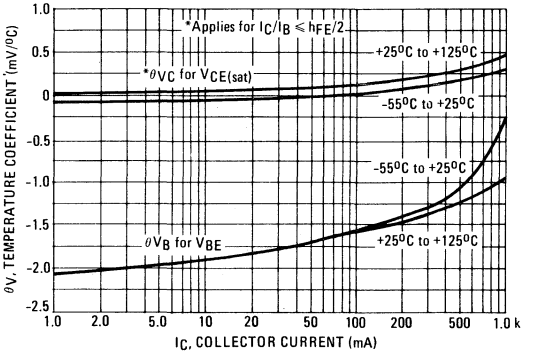


FIGURE 7 – COLLECTOR CHARACTERISTICS

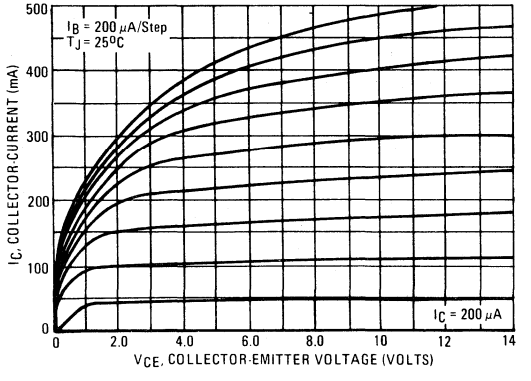
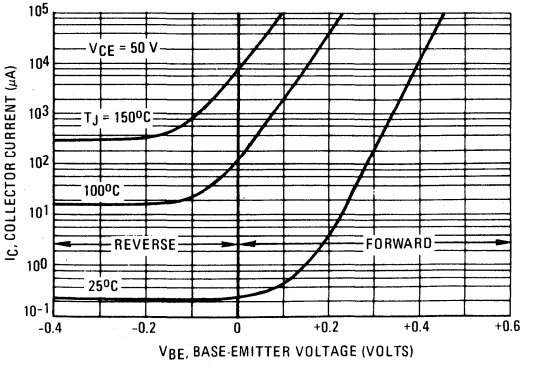


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – THERMAL RESPONSE

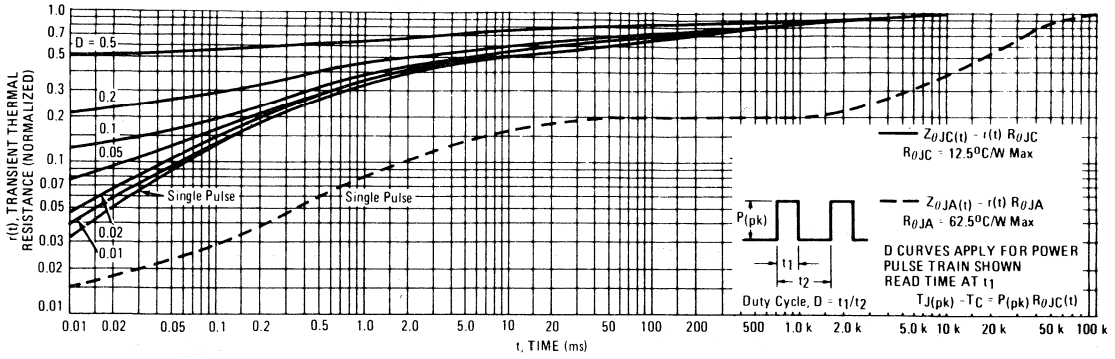
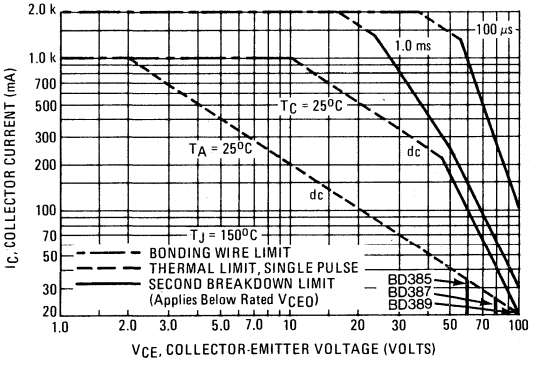


FIGURE 10 – ACTIVE-REGION SAFE-OPERATING AREA

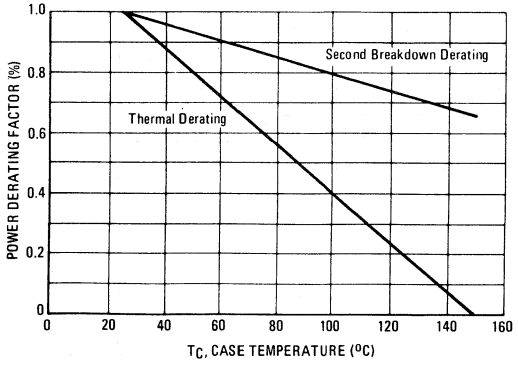


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



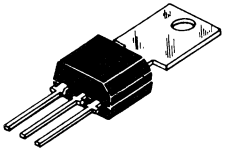
BD386
BD388 • BD390

PNP SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc — BD390
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BD385/BD387/BD389

PNP SILICON AMPLIFIER TRANSISTORS



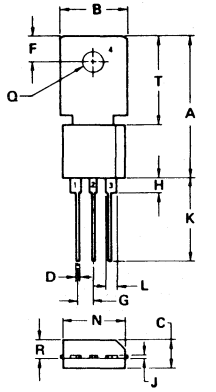
MAXIMUM RATINGS

Rating	Symbol	BD386	BD388	BD390	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current — Continuous Peak	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

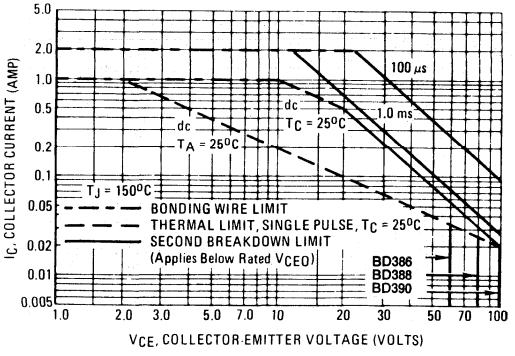
♦Annular Semiconductors Patented by Motorola Inc.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS •					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD386	BV_{CEO}	60	–	Vdc
	BD388		80	–	
	BD390		100	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BD386	BV_{CBO}	60	–	Vdc
	BD388		80	–	
	BD390		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD386		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD388		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD390		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	75	250	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	18	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

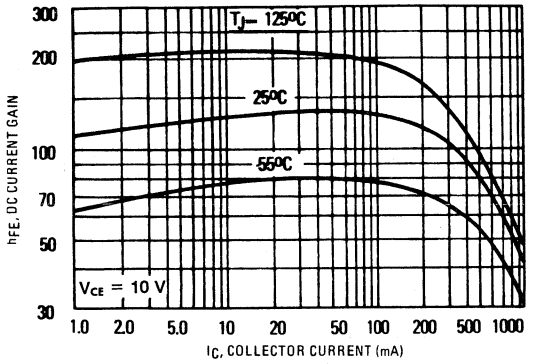


FIGURE 2 – DC CURRENT GAIN

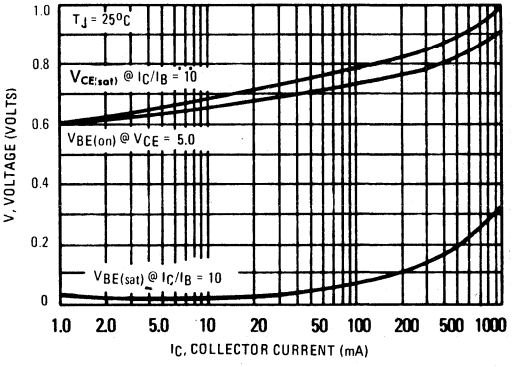


FIGURE 3 – "ON" VOLTAGES

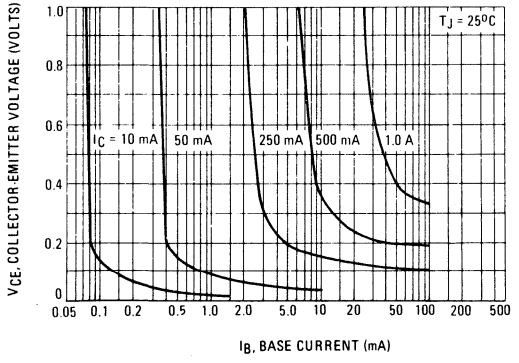


FIGURE 4 – COLLECTOR SATURATION REGION

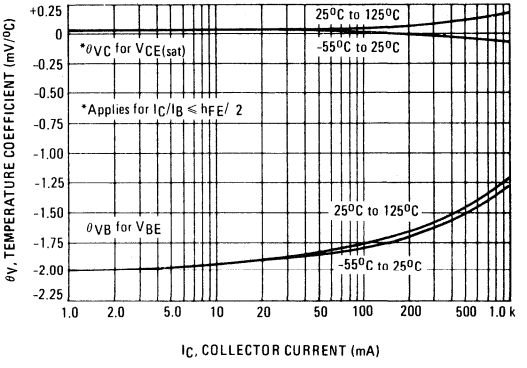


FIGURE 5 – TEMPERATURE COEFFICIENTS

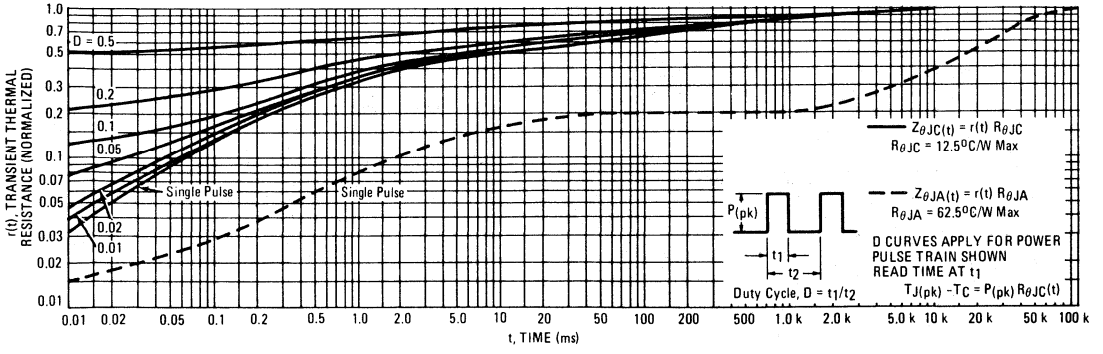


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

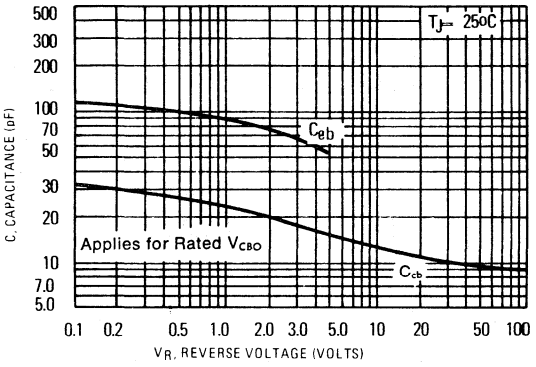


FIGURE 7 – CAPACITANCE

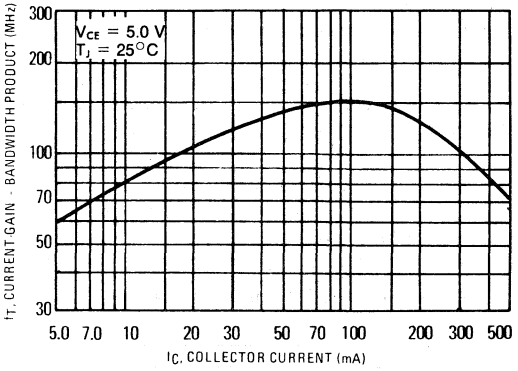


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

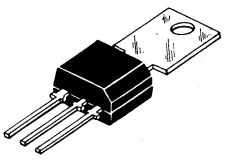
BD411
BD412

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc – BD 411
  = 15,000 (Min) @ I_C = 500 mAdc – BD 411
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- **Complements to PNP BD 413/414**

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS



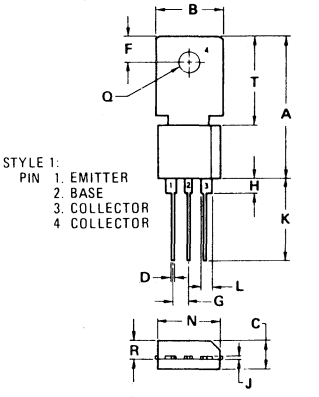
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current – Continuous	I_C	2.0	Adc
*Base Current – Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

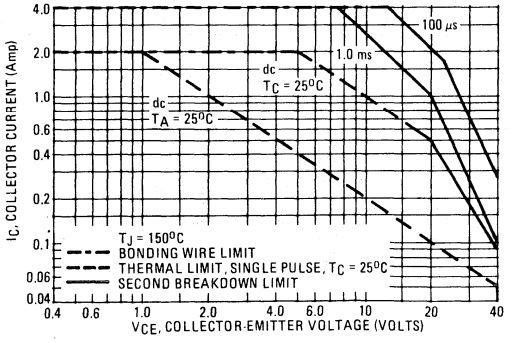
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	12	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS(1)				
DC Current Gain	h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc) BD411		25,000	150,000	
BD412		15,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc) BD411		15,000	–	
BD412		10,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) BD411		5,000	–	
BD412		3,000	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 2.0 mAdc)		–	1.5	
(I_C = 2.0 Adc, I_B = 4.0 mAdc)		–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
High Frequency Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	1.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	7.0	pF
Small-Signal Current Gain	h_{fe}			–
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz) BD411		20,000	–	
BD412		15,000	–	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

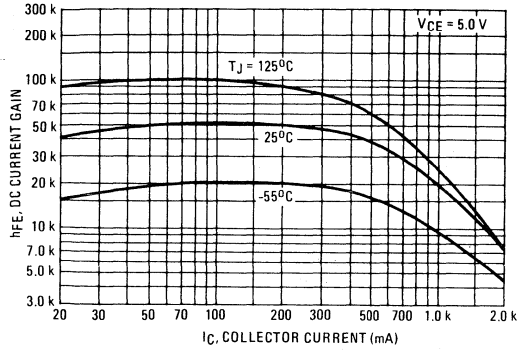


FIGURE 3 – "ON" VOLTAGES

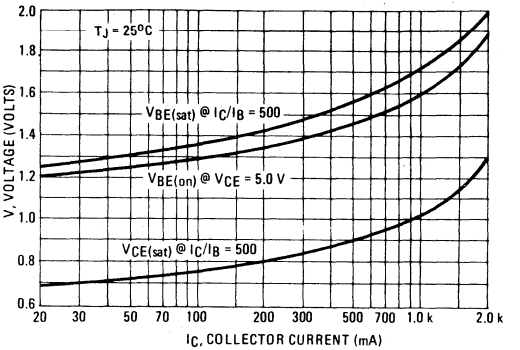


FIGURE 4 – COLLECTOR SATURATION REGION

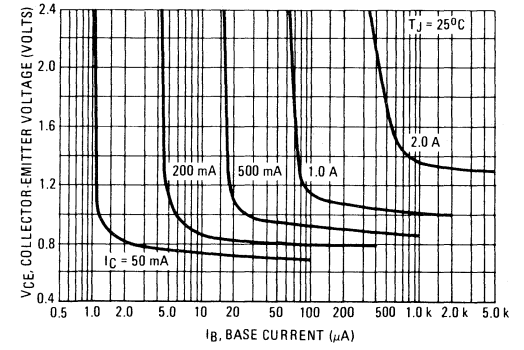


FIGURE 5 – TEMPERATURE COEFFICIENT

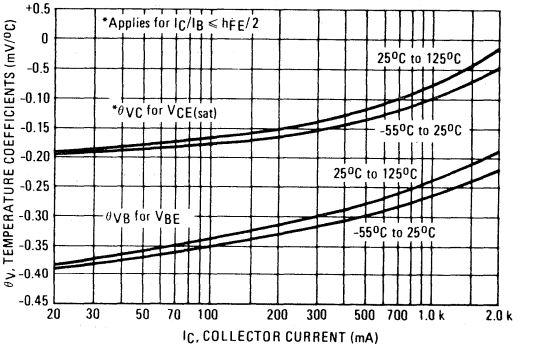
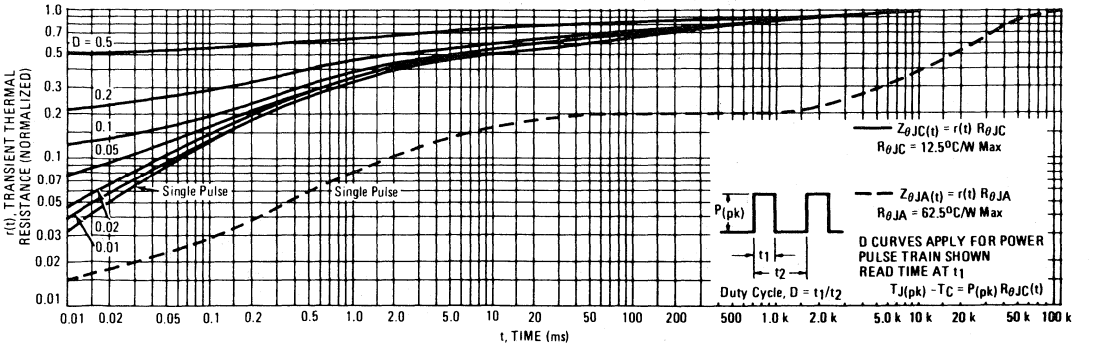


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

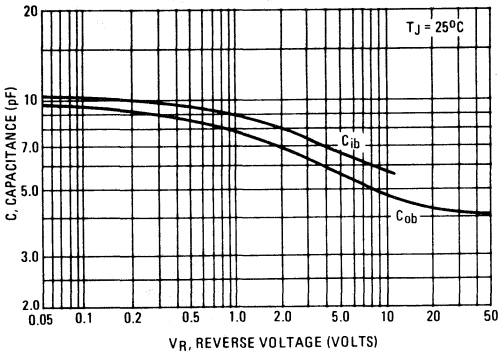
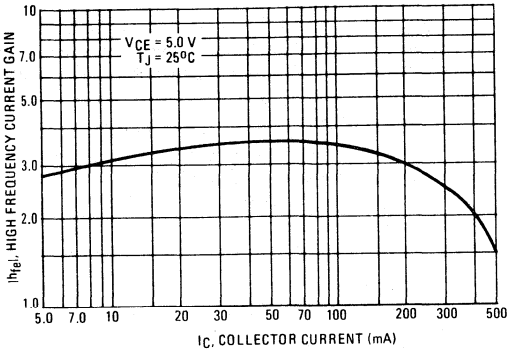


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN



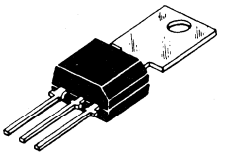
BD413
BD414

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain –
  h_{FE} = 20,000 (Min) @ I_C = 200 mAdc – BD413
  = 15,000 (Min) @ I_C = 500 mAdc – BD414
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BD411/412

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS



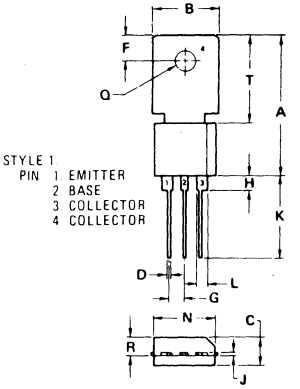
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current – Continuous	I_C	2.0	Adc
*Base Current – Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

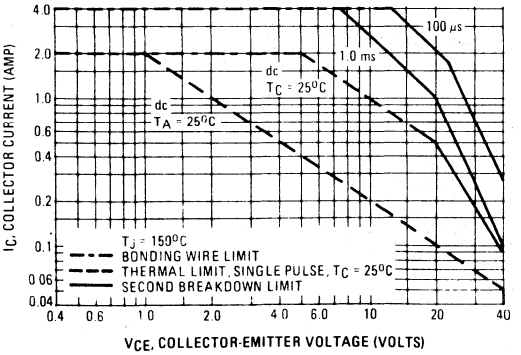
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 μAdc, V_{BE} = 0)		BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	12	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	BD413		20,000	150,000	
	BD414		15,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	BD413		15,000	–	
	BD414		10,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	BD413		5,000	–	
	BD414		3,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 2.0 mAdc)			–	1.5	
(I_C = 2.0 Adc, I_B = 4.0 mAdc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
High Frequency Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		$\lvert h_{fe} \rvert$	0.5	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	12	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BD413	h_{fe}	20,000	–	
	BD414		15,000	–	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

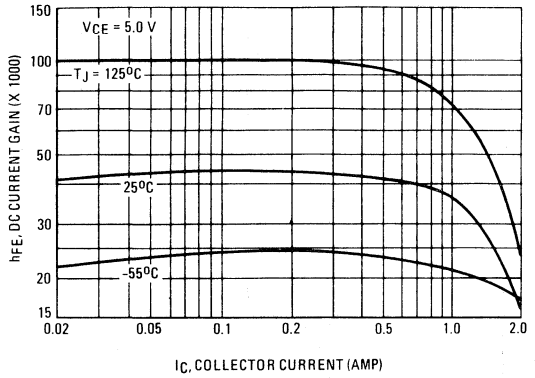


FIGURE 3 – "ON" VOLTAGES

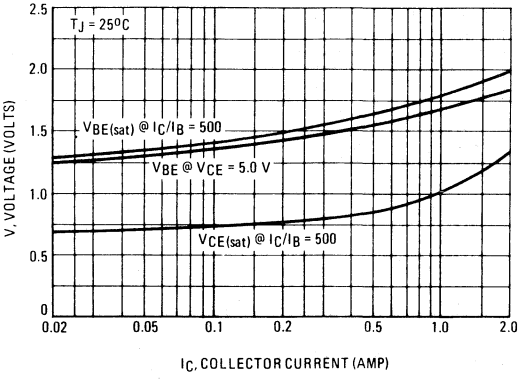


FIGURE 4 – COLLECTOR SATURATION REGION

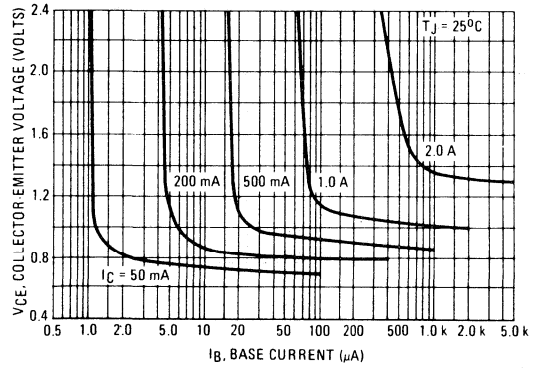


FIGURE 5 – TEMPERATURE COEFFICIENT

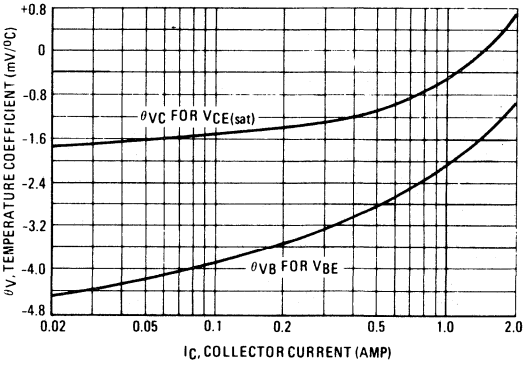
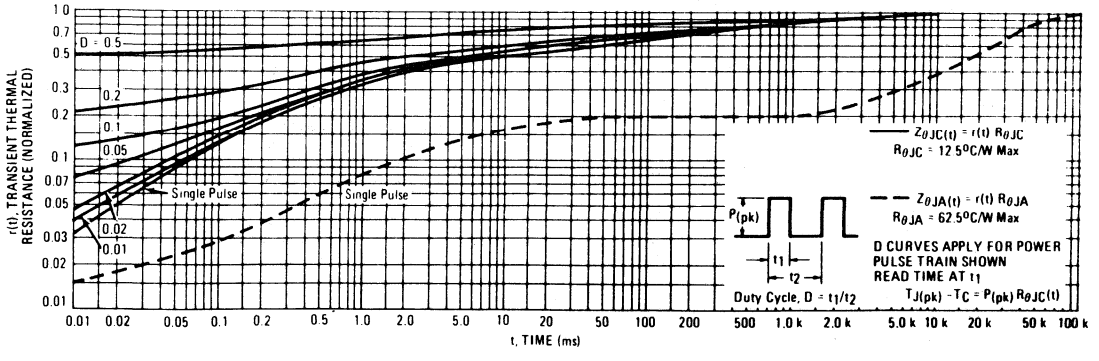


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

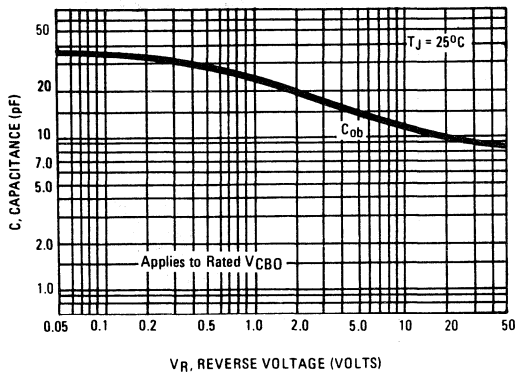
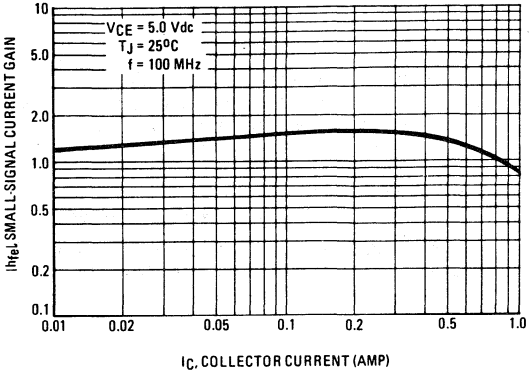


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN



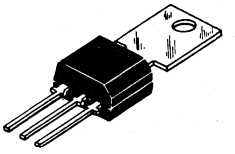
BD415
BD417 • BD419

NPN SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc – BD419
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^oC$
- Complements to PNP BD416/BD418/BD420

NPN SILICON AMPLIFIER TRANSISTORS



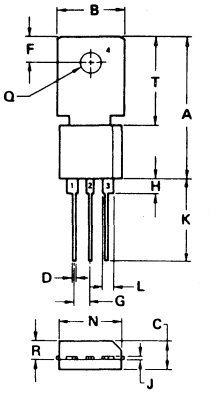
MAXIMUM RATINGS

Rating	Symbol	BD415	BD417	BD419	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current – Continuous Peak	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	2.0 16			Watts $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80			Watts $mW/^oC$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			^oC
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	62.5	$^oC/W$
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	$^oC/W$

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

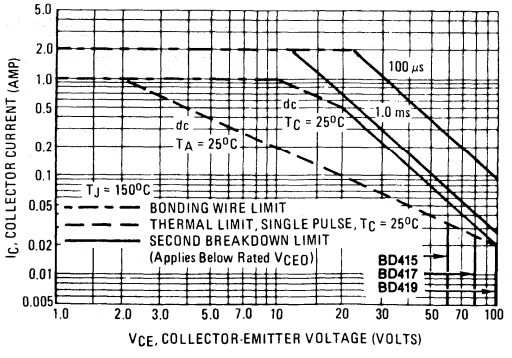
♦Annular Semiconductors Patented by Motorola Inc.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD415	BV_{CEO}	60	–	Vdc
	BD417		80	–	
	BD419		100	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BD415	BV_{CBO}	60	–	Vdc
	BD417		80	–	
	BD419		100	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD415		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD417		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD419		–	100	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		f_T	75	250	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

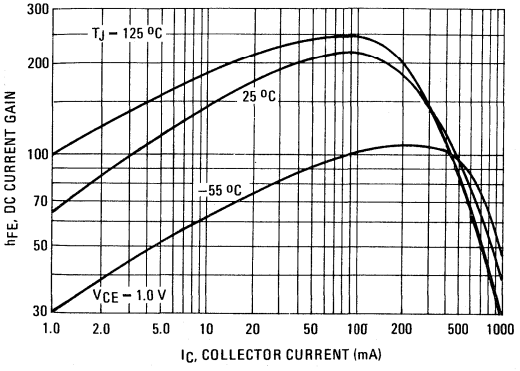


FIGURE 2 – DC CURRENT GAIN

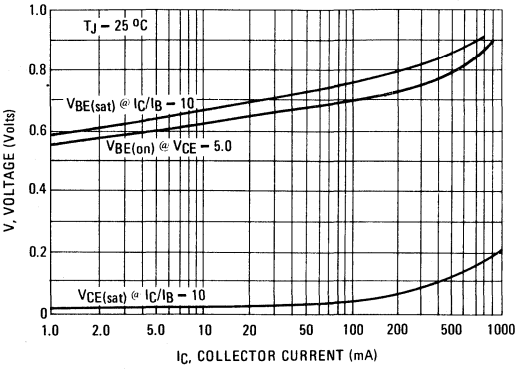


FIGURE 3 – "ON" VOLTAGES

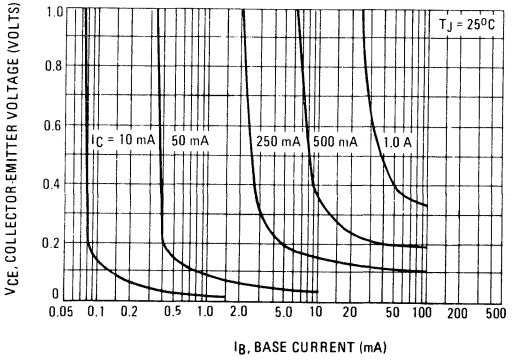


FIGURE 4 – COLLECTOR SATURATION REGION

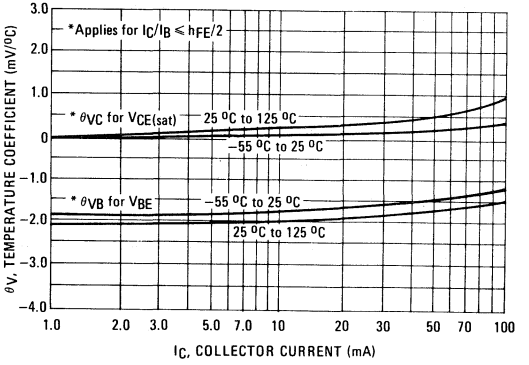


FIGURE 5 – TEMPERATURE COEFFICIENTS

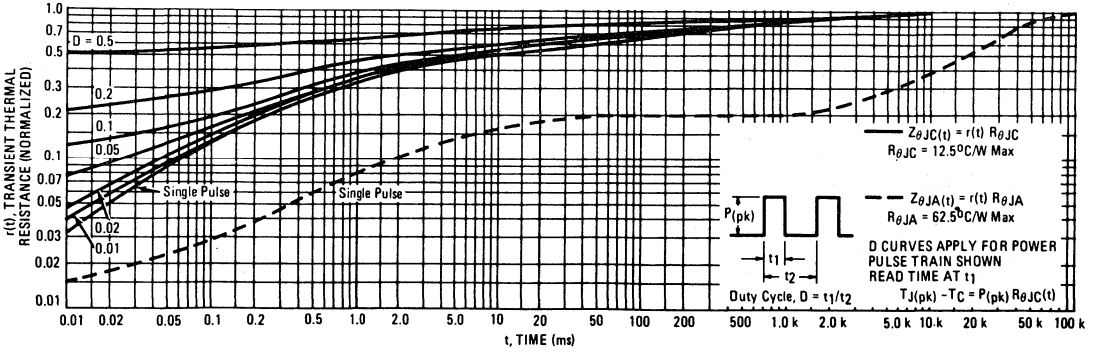


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

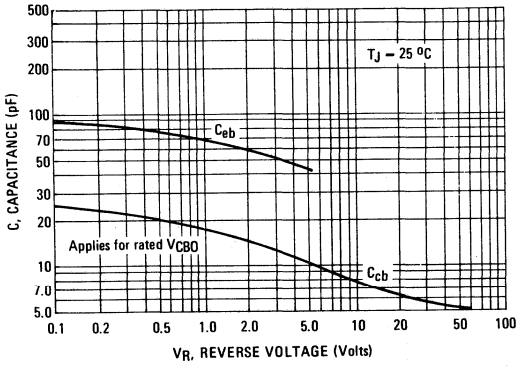


FIGURE 7 – CAPACITANCE

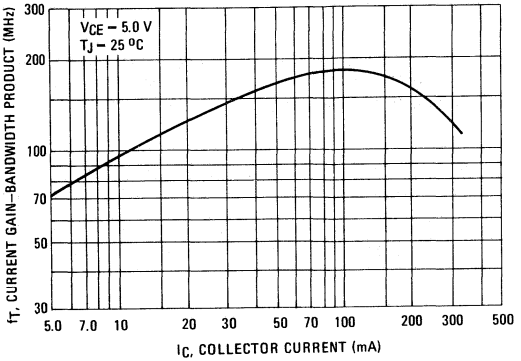


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

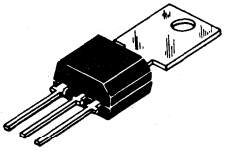
BD416
BD418 • BD420

PNP SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc - **BD420**
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^oC$
- Complements to NPN BD415/BD417/BD419

PNP SILICON AMPLIFIER TRANSISTORS



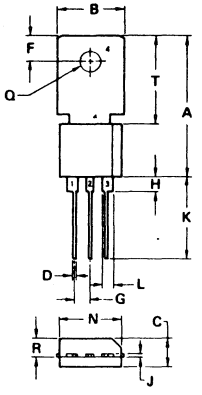
MAXIMUM RATINGS

Rating	Symbol	BD416	BD418	BD420	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current – Continuous Peak	I_C	1.0 2.0			Adc
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	2.0 16			Watts mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80			Watts mW/^oC
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			^oC
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	62.5	$^oC/W$
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	$^oC/W$

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

♦Annular Semiconductors Patented by Motorola Inc.

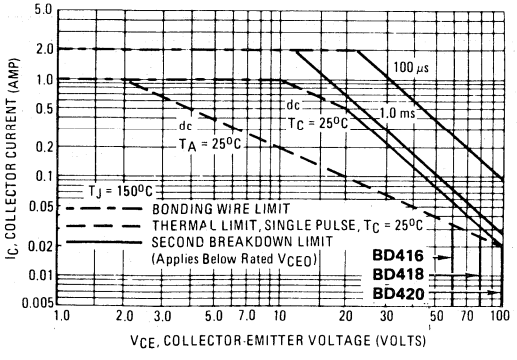
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	BD416		60	–	
	BD418		80	–	
	BD420		100	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BD416		60	–	
	BD418		80	–	
	BD420		100	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD416		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD418		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD420		–	100	
Emitter Cutoff Current		I_{EBO}	–	100	nAdc
(V_{EB} = 4.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	75	250	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	18	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

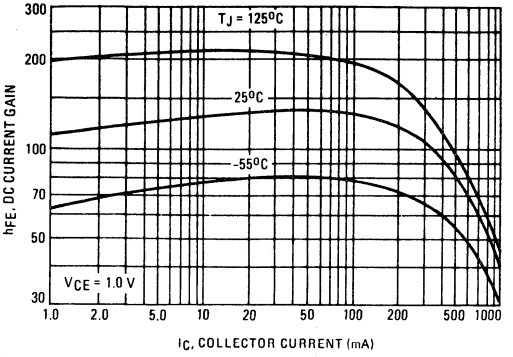


FIGURE 3 – "ON" VOLTAGE

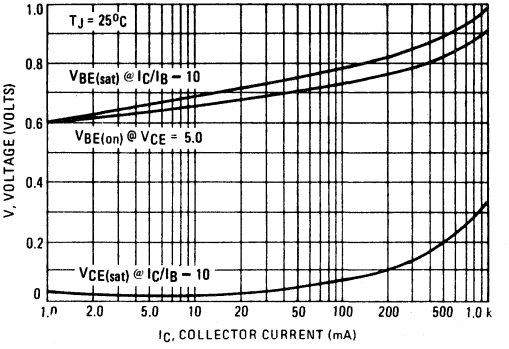


FIGURE 4 – COLLECTOR SATURATION REGION

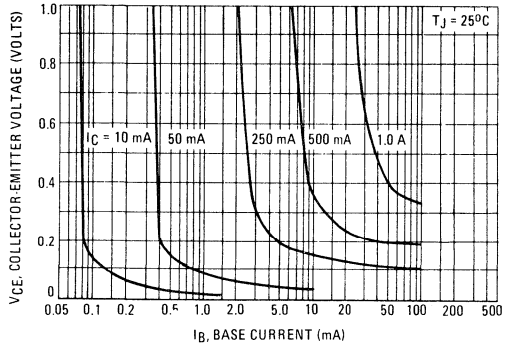


FIGURE 5 – TEMPERATURE COEFFICIENT

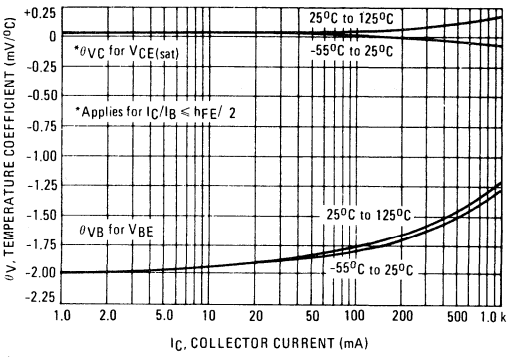
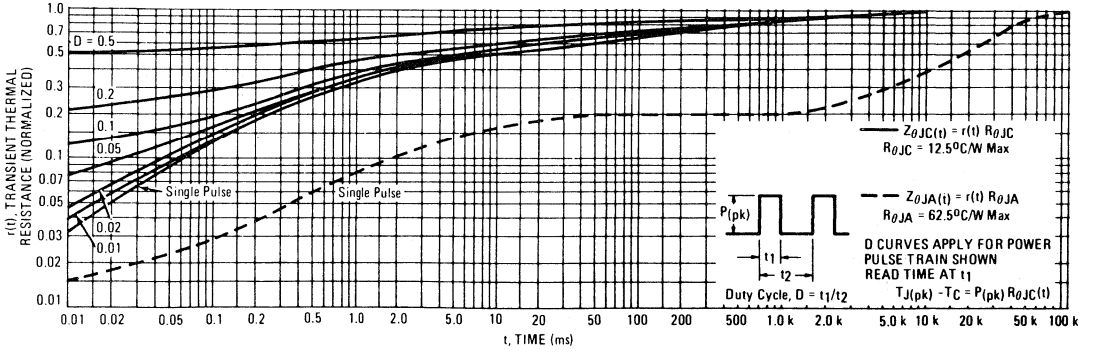


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

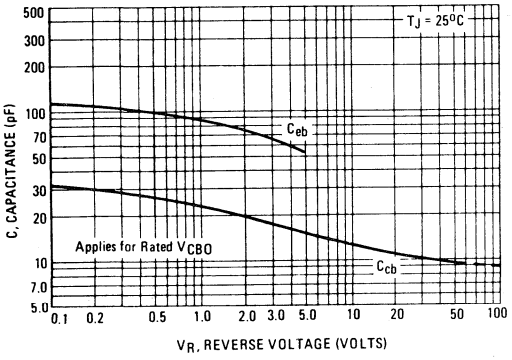
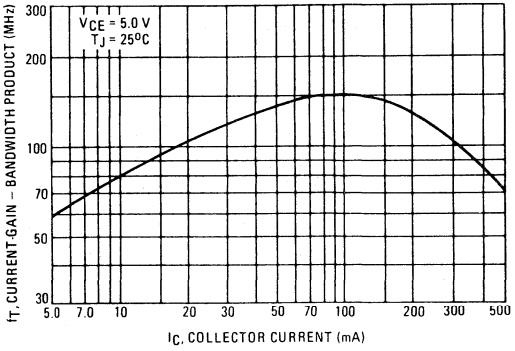


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT



BD505
BD507 • BD509

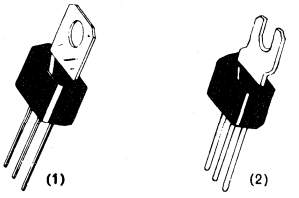
NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to PNP BD506, BD508, BD510
- Uniwatt▲ Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C, 10.0 Watts @ T_C = 25°C

NPN SILICON AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
10 WATTS



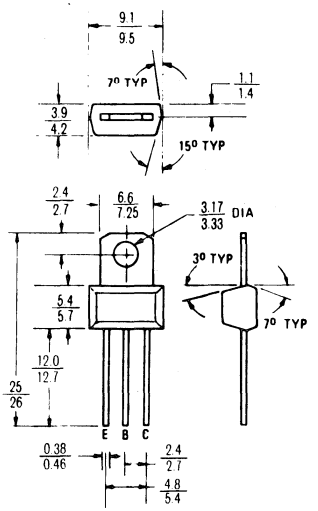
(1) Standard package: BD505, 507, 509
(2) Tab formed for flat mounting: BD505-1, 507-1, 509-1
Also available with leads formed to TO-5 configuration: BD505-5, 507-5, 509-5

MAXIMUM RATINGS

Rating	Symbol	BD505	BD507	BD509	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}	—	5.0	—	Vdc
Collector Current - Continuous	I_C	—	2.0	—	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0			Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

♦Annular Semiconductors Patented by Motorola Inc.
▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD505 BD507 BD509	BV_{CEO}	20 30 40	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	—	—	Vdc
Collector Cutoff Current (VCB = 20, 30, 40 Vdc, I_E = 0)	BD505 BD507 BD509	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 250 mAdc, V_{CE} = 2 Vdc) (I_C = 1.0 Adc, V_{CE} = 2 Vdc)		h_{FE}	60 40	160 90	— —	—
Collector-Emitter Saturation Voltage(1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.30	0.7	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	0.91	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

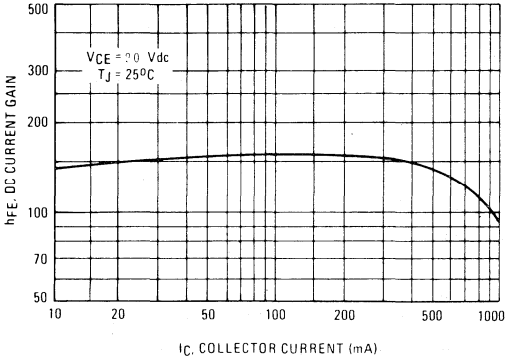


FIGURE 2 — "ON" VOLTAGES

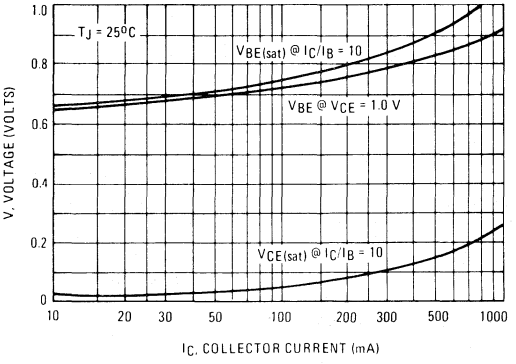
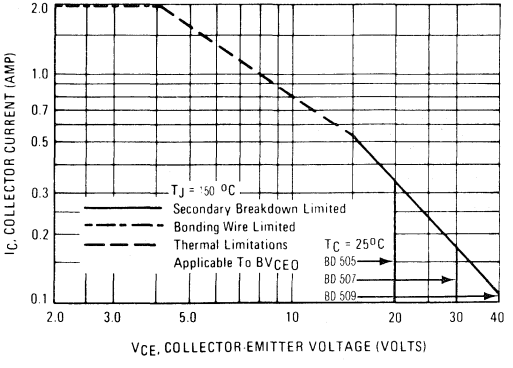


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD506
BD508 • BD510

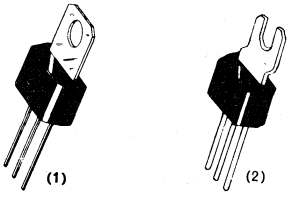
PNP SILICON ANNULAR♦ TRANSISTORS

. . . designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to NPN BD505, BD507, BD509
- Uniwatt▲ Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C, 10.0 Watts @ T_C = 25°C

PNP SILICON AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
10 WATTS



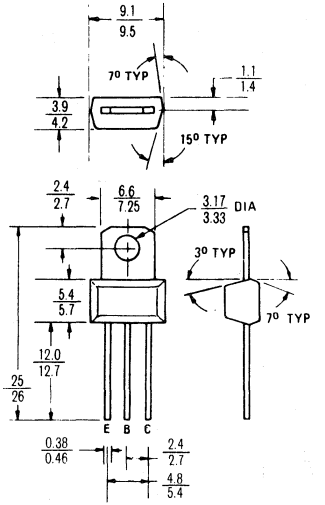
(1) Standard package: BD506, 508, 510
(2) Tab formed for flat mounting: BD506-1, 508-1, 510-1
Also available with leads formed to TO-5 configuration: BD506-5, 508-5, 510-5

MAXIMUM RATINGS

Rating	Symbol	BD506	BD508	BD510	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}	——	5.0	——	Vdc
Collector Current – Continuous	I_C	——	2.0	——	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

♦Annular Semiconductors Patented by Motorola Inc.
▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD506	BV_{CEO}	20	—	—	Vdc
	BD508		30	—	—	
	BD510		40	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 20, 30, 40 Vdc, I_E = 0)	BD506	I_{CBO}	—	—	100	nAdc
	BD508		—	—	100	
	BD510		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 250 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	60	135	—	—
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			40	90	—	
Collector-Emitter Saturation Voltage(1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.40	0.7	Vdc
Base-Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	0.92	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	180	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

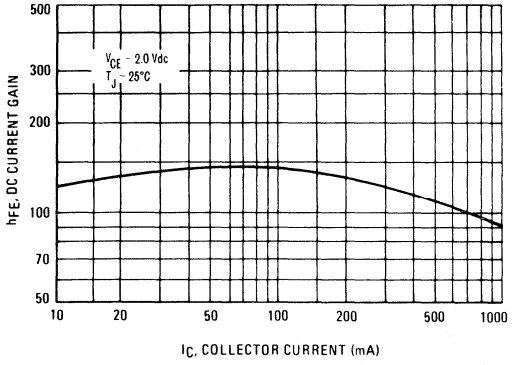


FIGURE 2 — "ON" VOLTAGES

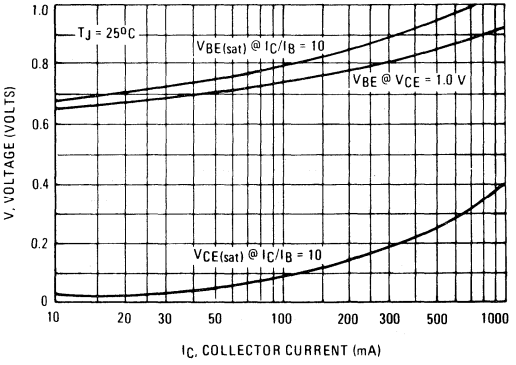
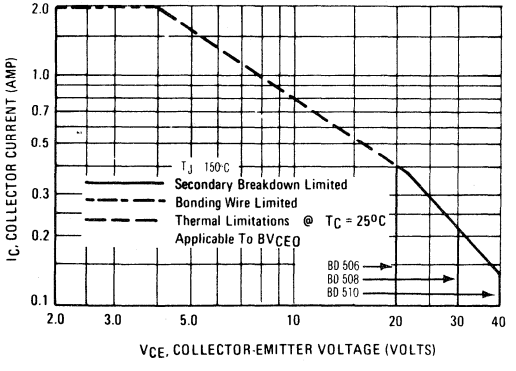


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_J (pk) = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD515
BD517 • BD519

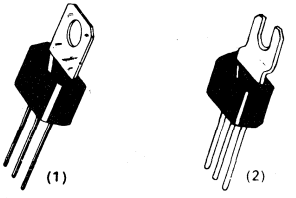
NPN SILICON ANNULAR* AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) @ I_C = 1 mAdc — BD515
  60 Vdc (Min) @ I_C = 1 mAdc — BD517
  80 Vdc (Min) @ I_C = 1 mAdc — BD519
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to BD516, BD518, BD520

NPN SILICON AMPLIFIER TRANSISTORS

45 - 60 - 80 VOLTS
10 WATTS



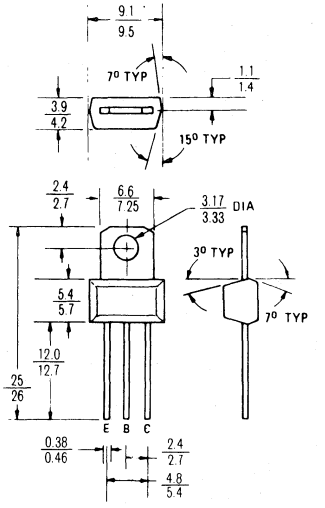
(1) Standard package: BD515, 517, 519
(2) Tab formed for flat mounting: BD515-1, 517-1, 519-1
Also available with leads formed to TO-5 configuration: BD515-5, 517-5, 519-5

MAXIMUM RATINGS

Rating	Symbol	BD515	BD517	BD519	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	——	4.0	——	Vdc
Collector Current — Continuous	I_C	——	2.0	——	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}		-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

*Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD515	BV_{CEO}	45	—	—	Vdc
	BD517		60	—	—	
	BD519		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current						nAdc
(V_{CB} = 30 Vdc, I_E = 0)	BD515	I_{CBO}	—	—	100	
(V_{CB} = 40 Vdc, I_E = 0)	BD517		—	—	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD519		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				—
(I_C = 10 mAdc, V_{CE} = 2.0 Vdc)			—	115	—	
(I_C = 150 mAdc, V_{CE} = 2.0 Vdc)			60	125	350	
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)			25	55	—	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$				Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.18	0.5	
(I_C = 500 mAdc, I_B = 25 mAdc)			—	0.24	—	
Base-Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	0.74	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	160	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — TYPICAL DC CURRENT GAIN

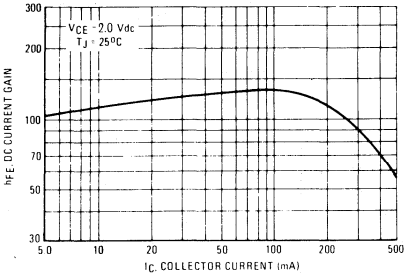


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

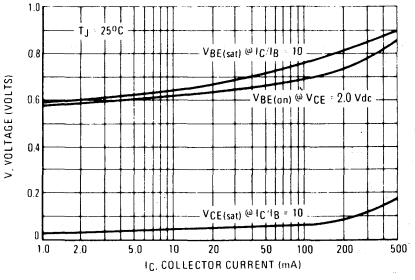


FIGURE 3 — DC SAFE OPERATING AREA

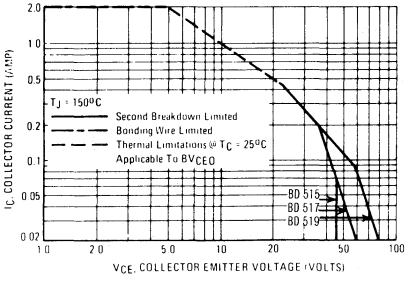
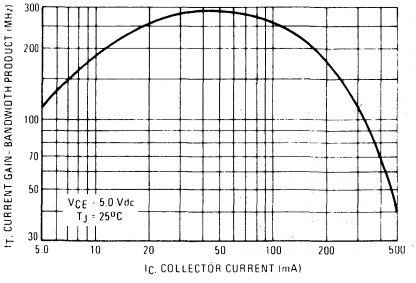


FIGURE 4 — CURRENT-GAIN — BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD516
BD518 • BD520

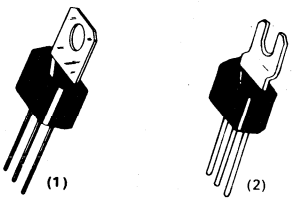
PNP SILICON ANNULAR * AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) @ I_C = 1 mAdc — BD516
  60 Vdc (Min) @ I_C = 1 mAdc — BD518
  80 Vdc (Min) @ I_C = 1 mAdc — BD520
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to BD515, BD517, BD519

PNP SILICON ANNULAR * AMPLIFIER TRANSISTORS

45 - 60 - 80 VOLTS
10 WATTS



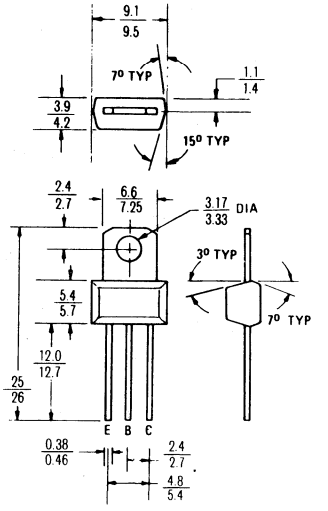
(1) Standard package: BD516, 518, 520
(2) Tab formed for flat mounting: BD516-1, 518-1, 520-1
Also available with leads formed to TO-5 configuration: BD516-5, 518-5, 520-5

MAXIMUM RATINGS

Rating	Symbol	BD516	BD518	BD520	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	—— 4.0 ——			Vdc
Collector Current — Continuous	I_C	—— 2.0 ——			Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0			Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

*Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD516	BV_{CEO}	45	—	—	Vdc
	BD518		60	—	—	
	BD520		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current						nAdc
(V_{CB} = 30 Vdc, I_E = 0)	BD516	I_{CBO}	—	—	100	
(V_{CB} = 40 Vdc, I_E = 0)	BD518		—	—	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD520		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				—
(I_C = 10 mAdc, V_{CE} = 2.0 Vdc)			—	150	—	
(I_C = 150 mAdc, V_{CE} = 2.0 Vdc)			60	130	350	
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)			25	80	—	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$				Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.24	0.5	
(I_C = 500 mAdc, I_B = 25 mAdc)			—	0.32	—	
Base-Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	0.78	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	125	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

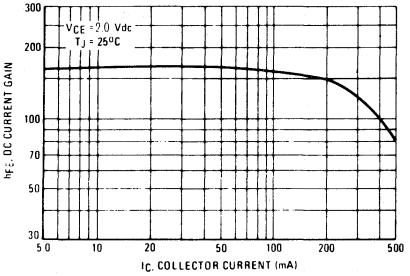


FIGURE 2 — "ON" VOLTAGES

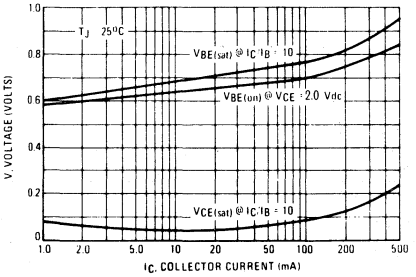


FIGURE 3 — DC SAFE OPERATING AREA

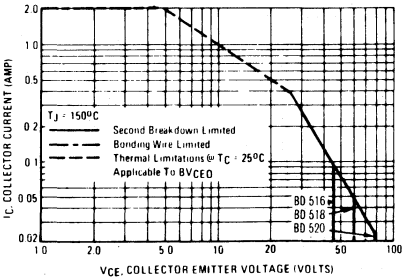
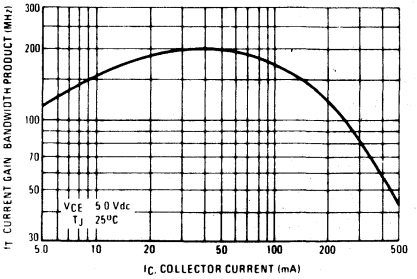


FIGURE 4 — CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150 °C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD525
BD527 • BD529

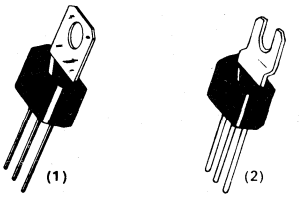
NPN SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — BD525
  80 Vdc (Min) @ I_C = 1.0 mAdc — BD527
  100 Vdc (Min) @ I_C = 1.0 mAdc — BD529
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to PNP BD526, BD528, BD530

NPN SILICON AMPLIFIER TRANSISTORS

60 - 80 - 100 VOLTS
10 WATTS



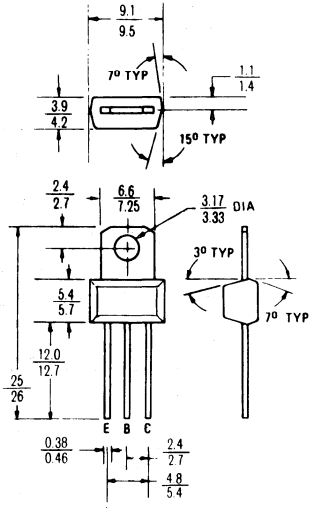
(1) **Standard package: BD525, 527, 529**
(2) Tab formed for flat mounting: BD525-1, 527-1, 529-1
Also available with leads formed to TO-5 configuration: BD525-5, 527-5, 529-5

MAXIMUM RATINGS

Rating	Symbol	BD525	BD527	BD529	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	—— 4.0 ——			Vdc
Collector Current — Continuous	I_C	—— 2.0 ——			Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0			Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

♦Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD525	BV_{CEO}	60	—	—	Vdc
	BD527		80	—	—	
	BD529		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current						nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD525	I_{CBO}	—	—	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD527		—	—	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD529		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				—
(I_C = 50 mAdc, V_{CE} = 2.0 Vdc)			60	115	—	
(I_C = 250 mAdc, V_{CE} = 2.0 Vdc)			30	95	—	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			—	0.18	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)			—	0.1	—	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	0.74	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	150	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — TYPICAL DC CURRENT GAIN

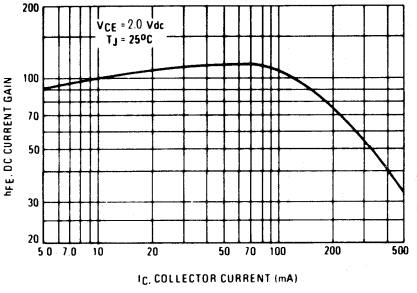


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

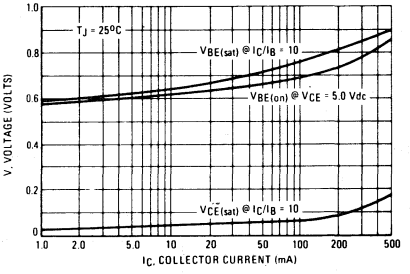


FIGURE 3 — SAFE OPERATING AREA

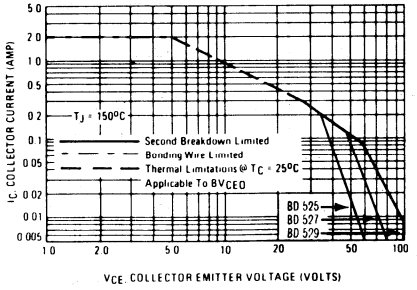
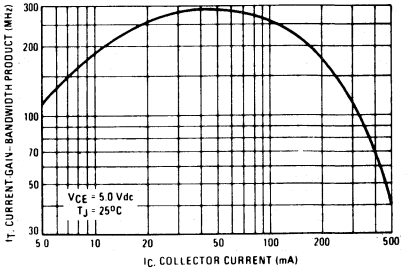


FIGURE 4 — CURRENT-GAIN BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on TJ(pk) = 150 °C; TC is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD526
BD528 • BD530

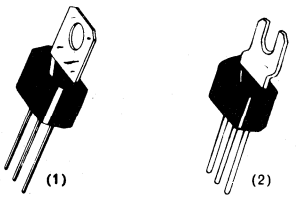
PNP SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc — BD526
  80 Vdc (Min) @ I_C = 1.0 mAdc — BD528
  100 Vdc (Min) @ I_C = 1.0 mAdc — BD530
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complements to NPN BD525, BD527, BD529

PNP SILICON AMPLIFIER TRANSISTORS

60 - 80 - 100 VOLTS
10 WATTS



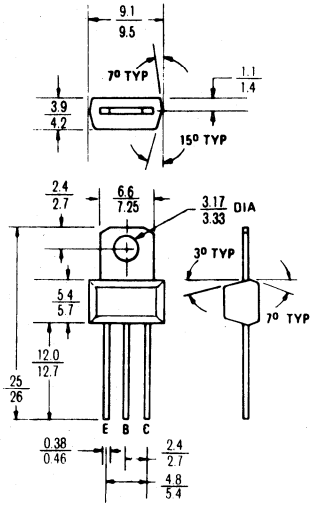
(1) Standard package: BD526, 528, 530
(2) Tab formed for flat mounting: BD526-1, 528-1, 530-1
Also available with leads formed to TO-5 configuration: BD526-5, 528-5, 530-5

MAXIMUM RATINGS

Rating	Symbol	BD526	BD528	BD530	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	—— 4.0 ——			Vdc
Collector Current - Continuous	I_C	—— 2.0 ——			Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0			Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

♦Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BD526	BV_{CEO}	60	—	—	Vdc
	BD528		80	—	—	
	BD530		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current						nAdc
(V_{CB} = 40 Vdc, I_E = 0)	BD526	I_{CBO}	—	—	100	
(V_{CB} = 60 Vdc, I_E = 0)	BD528		—	—	100	
(V_{CB} = 80 Vdc, I_E = 0)	BD530		—	—	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				—
(I_C = 50 mAdc, V_{CE} = 2.0 Vdc)			60	153	—	
(I_C = 250 mAdc, V_{CE} = 2.0 Vdc)			30	98	—	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			—	0.22	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)			—	0.15	—	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	0.78	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain--Bandwidth Product (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	100	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

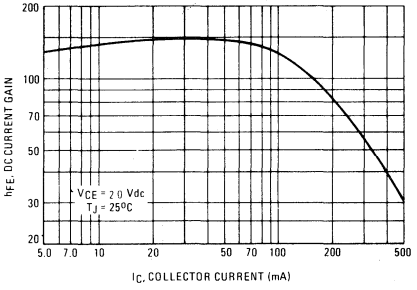


FIGURE 2 — "ON" VOLTAGES

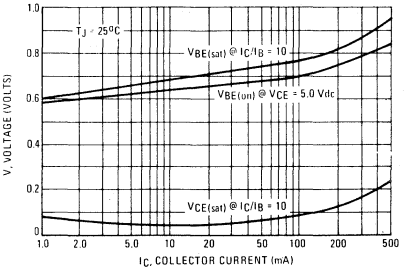


FIGURE 3 — DC SAFE OPERATING AREA

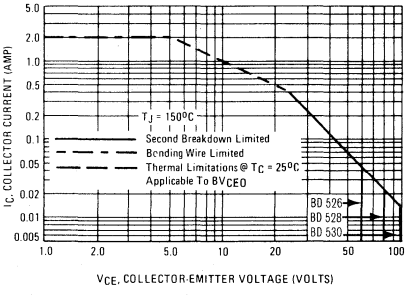
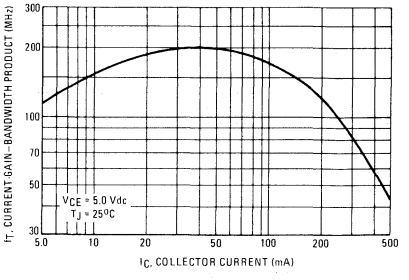


FIGURE 4 — CURRENT-GAIN--BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

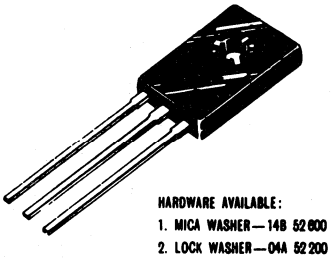
The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD561

NPN SILICON MEDIUM-POWER TRANSISTOR

- Designed for 5 to 10W Audio Amplifiers
- BD561 is complementary to BD562
- P_D of 40W with T_j of 150° C
- Case 77 package is Pin compatible with SOT-9

4 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
40 WATTS



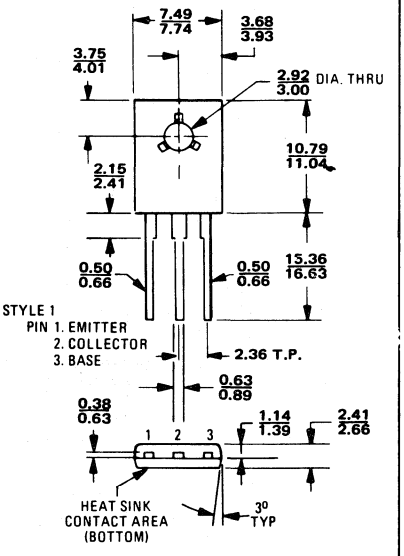
HARDWARE AVAILABLE:
1. MICA WASHER—14B 52 000 F03
2. LOCK WASHER—04A 52 200 F01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current	I_C	4	Adc
Base Current	I_B	2	Adc
Total Device Dissipation $T_C = 25°$ C Derate above 25° C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—65 to +150	° C

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	° C/W



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

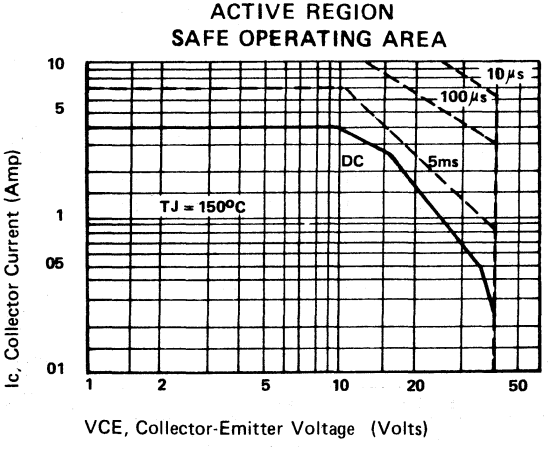
All dimensions in millimeters

CASE 77-03

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector Cutoff Current (V_{CB} = 45 V, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 V, I_C = 0)	I_{EBO}	—	0.1	mAdc
DC Current Gain (I_C = 50 mA V_{CE} = 1.0 V) * (I_C = 500 mA V_{CE} = 1.0 V) * (I_C = 2.0 A V_{CE} = 1.0 V) *	h_{FE}	 40 60 40	 — — —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 A I_B = 0.1 A) *	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage (I_C = 2.0 A V_{CE} = 1.0 V) *	$V_{BE(on)}$	—	1.2	Vdc

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %

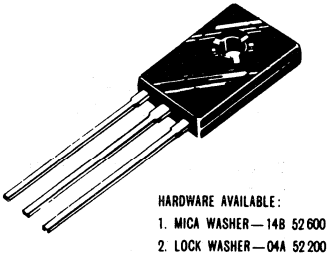


BD562

PNP SILICON MEDIUM-POWER TRANSISTOR

- Designed for 5 to 10W Audio Amplifiers
- BD562 is complementary to BD561
- P_D of 40W with T_j of 150° C
- Case 77 package is Pin compatible with SOT-9

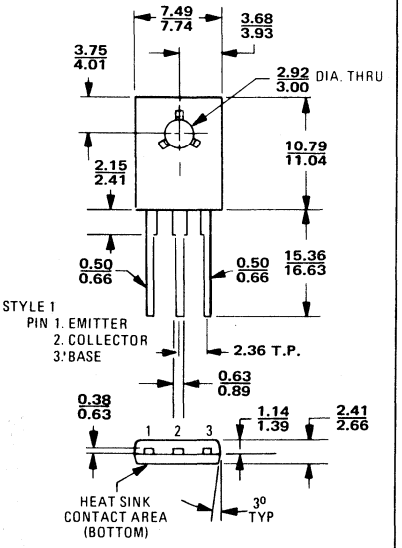
4 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
40 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current	I_C	4	Adc
Base Current	I_B	2	Adc
Total Device Dissipation $T_C = 25°$ C Derate above 25° C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—65 to +150	° C



When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

All dimensions in millimeters

CASE 77-03

E - 075 R1

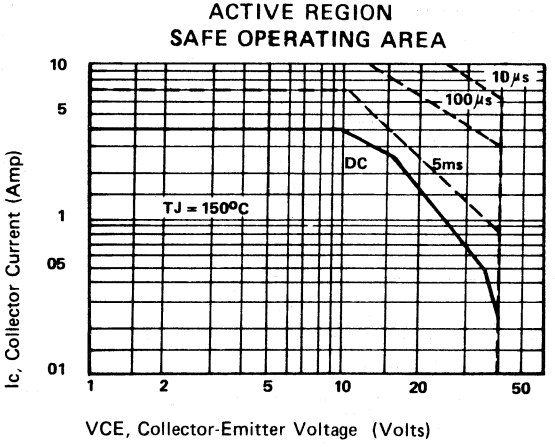
THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Characteristics	Symbol	Min.	Max.	Unit
Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector Cutoff Current (V_{CB} = 45 V, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 V, I_C = 0)	I_{EBO}	—	0.1	mAdc
DC Current Gain (I_C = 50 mA V_{CE} = 1.0 V) * (I_C = 500 mA V_{CE} = 1.0 V) * (I_C = 2.0 A V_{CE} = 1.0 V) *	h_{FE}	 40 60 40	 — — —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 A I_B = 0.1 A) *	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage (I_C = 2.0 A V_{CE} = 1.0 V) *	$V_{BE(on)}$	—	1.2	Vdc

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0 %



BD675, 675A • BD677, 677A
BD679, 679A • 681

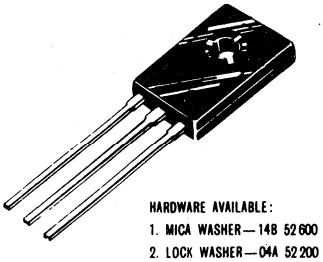
PLASTIC MEDIUM-POWER SILICON NPN DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

4.0 AMPERE
DARLINGTON POWER TRANSISTORS NPN SILICON

45, 60, 80, 100 VOLTS
40 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

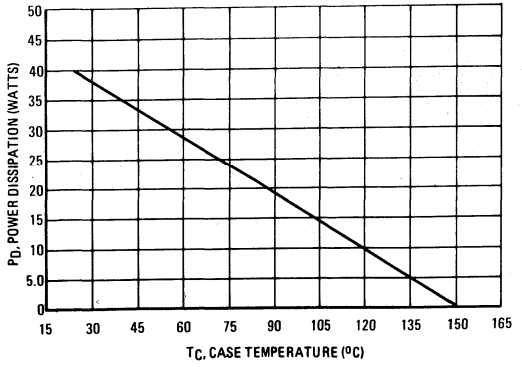
MAXIMUM RATINGS

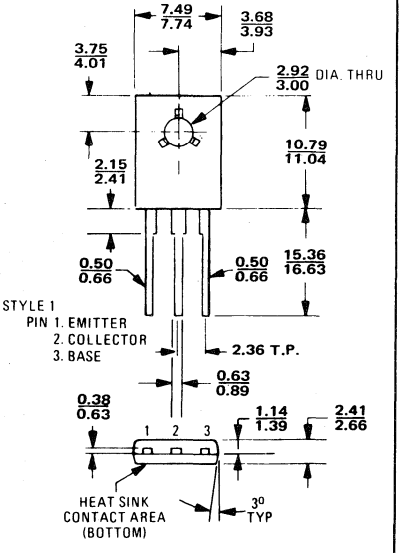
Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	–55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING





When mounting the device, torque not to exceed 0.07 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

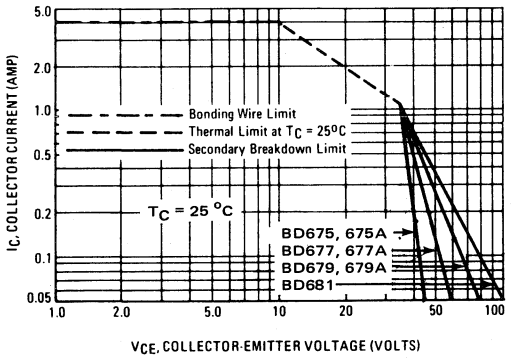
CASE 77-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD675, 677, 679, 681 BD 675A, 677A, 679A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	BD 677, 679 BD 675A, 677A, 679A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD 677, 679 BD 675A, 677A, 679A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

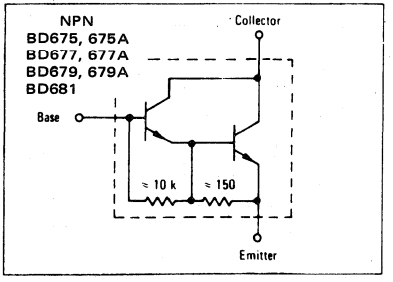
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 DARLINGTON CIRCUIT SCHEMATIC



BD676, 676A • BD678, 678A
BD680, 680A • BD682

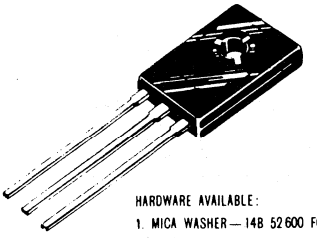
PLASTIC MEDIUM-POWER SILICON PNP DARLINGTONS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

4.0 AMPERE
DARLINGTON POWER TRANSISTORS PNP SILICON

45, 60, 80, 100 VOLTS
40 WATTS



HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

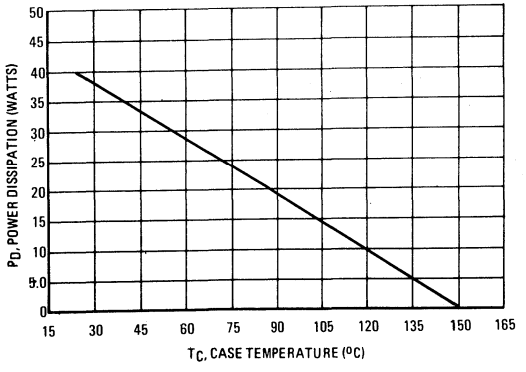
MAXIMUM RATING

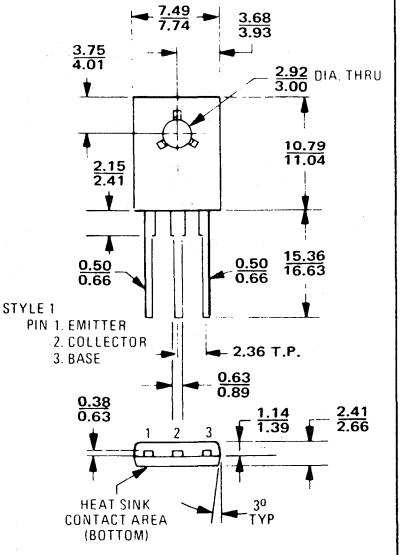
Rating	Symbol	BD676 BD676A	BD678 BD678A	BD680 BD680A	BD682	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING





When mounting the device torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

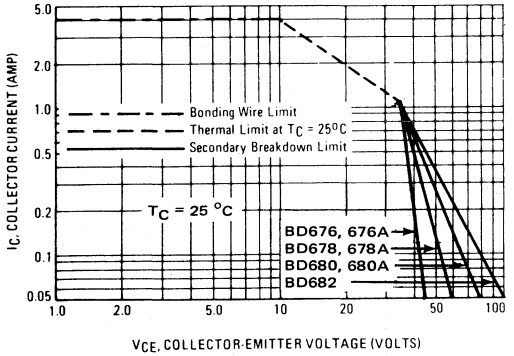
CASE 77-03

ELECTRICAL CHARACTERISTICS (T_C 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD676, 678, 680, 682 BD 676A, 678A, 680A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	BD 678, 680 BD 676A, 678A, 680A	$V_{CE(sat)}$	–	2.5 2.8	Vdc
Base-Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	BD 678, 680 BD 676A, 678A, 680A	$V_{BE(on)}$	–	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

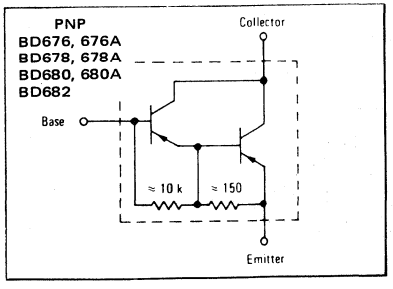
FIGURE 2 - DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 DARLINGTON CIRCUIT SCHEMATIC



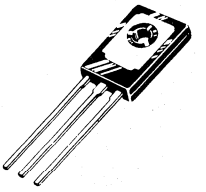
BD775, BD777, BD779 (NPN)
BD776, BD778, BD780 (PNP)

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR◇ POWER TRANSISTORS

. . . designed for general purpose amplifier and high-speed switching applications such as hammer drivers for desk calculators.

- High DC Current Gain
  h_{FE} = 1400 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage – @ 10 mAdc
  V_{CEO} (sus) = 45 Vdc (Min) – BD775, 776
  = 60 Vdc (Min) – BD777, 778
  = 80 Vdc (Min) – BD779, 780
- Reverse Voltage Protection Diode
- Monolithic Construction with Built-in Base-Emitter output Resistor
- Thermopad II△ Construction with Hard Solder for High Reliability.

DARLINGTON
4-AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
45, 60, 80 VOLTS
15 WATTS



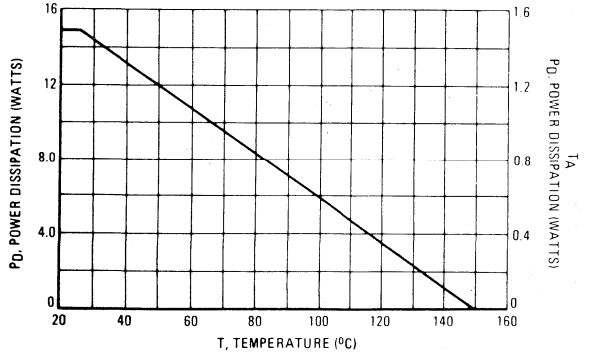
MAXIMUM RATINGS

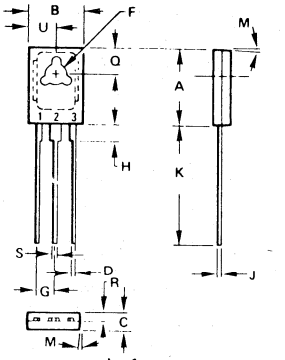
Rating	Symbol	BD775 BD776	BD777 BD778	BD779 BD780	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	4.0 6.0			Adc
Base Current	I_B	100			mAdc
Total Device Dissipation T_C = 25°C – Derate above 25°C	P_D	15 0.12			Watts W/°C
Operating and Storage junction Temperature Range	T_J, T_{stg} T_J, T_{stg}	– 65 to + 150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	RθJC	8.34	°C/W
Thermal Resistance, junction to Ambient	RθJA	83.3	°C/W

FIGURE 1 – POWER DERATING





style 1
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

CASE 77-03

◇ Annular Semiconductors Patented by Motorola Inc.
△ Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
OFF CHARACTERISTICS				
Collector-Emitter Collector-Emitter Sustaining Voltage (1) (I_O = 10 mAdc, I_B = 0) BD775, BD776 BD777, BD778 BD779, BD780	V_{CEO} (sus)	 45 60 80		Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) BD775, BD776 (V_{CE} = 30 Vdc, I_B = 0) BD777, BD778 (V_{CE} = 40 Vdc, I_B = 0) BD779, BD780	I_{CEO}		 100 100 100	μAdc
Collector Cutoff Current (V_{CB} = Rated, V_{CEO} (sus), I_E = 0) (V_{CB} = Rated, V_{CEO} (sus), I_E = 0, I_C = 100 °C)	I_{CBO}		 1.0 100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	H_{FE}	750		
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6 mAdc)	V_{CE} (Sat)		1.5	Vdc
Base Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6 mAdc)	V_{BE} (Sat)		2.5	Vdc
Base-Emitter On Voltage (I_C = 1.5 Adc, V_{CE} = 3 Vdc)	V_{BE} (On)		2.3	Vdc
Output Diode Voltage Drop (I_{EC} = 2.0 Adc)	V_{EC}		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	f_T	20		MHz
	SYMBOL		**TYP.**	**UNIT**
Turn-On Time (I_C = 250 mA/V_{CE} = 2 V) BD775-777-779 BD776-778-780	t_{on}	25	 250 150	ns
Turn Off Time (I_C = 250 mA, V_{CE} = 2 V) BD775-777-779 BD776-778-780	t_{off}		 600 400	ns

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

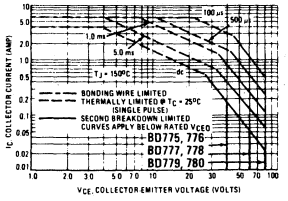


FIGURE 3 – TYPICAL DC CURRENT GAIN

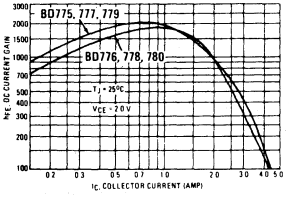
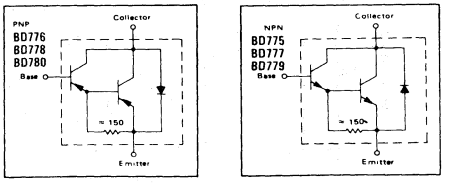


FIGURE 4 – DARLINGTON CIRCUIT SCHEMATIC



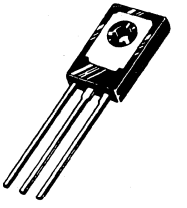
BD785, BD787 (NPN)
BD786, BD788 (PNP)

COMPLEMENTARY PLASTIC SILICON ANNULAR♦ POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
  V_{CEO} (sus) 45 Vdc (Min) – BD785, BD787
  60 Vdc (Min) – BD786, BD788
- High Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45, 60VOLTS
15 WATTS



*MAXIMUM RATINGS

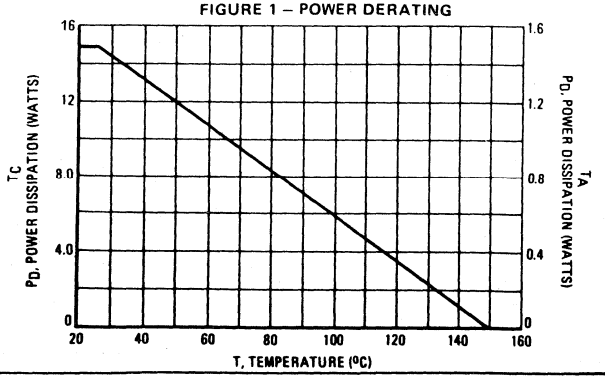
Rating	Symbol	BD785 BD786	BD787 BD788	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

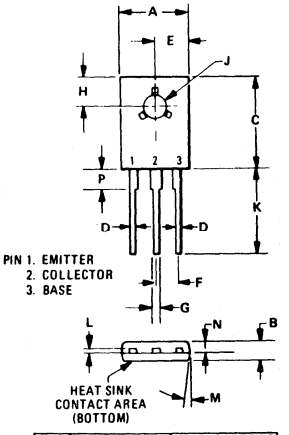
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.295	0.305	7.490	7.750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3.940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.170	16.380
L	0.015	0.025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0.095	2.160	2.410

CASE 77-03

♦Annular Semiconductors Patented by Motorola Inc.

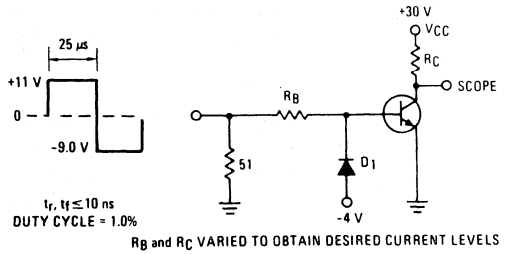
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	BD785, BD786	$V_{CEO(sus)}$	45	–	Vdc
	BD787, BD788		60	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	BD785, BD786		–	100	
(V_{CE} = 30 Vdc, I_B = 0)	BD787, BD788		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD785, BD786		–	1.0	μAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD787, BD788		–	1.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD785, BD786		–	0.1	mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C	BD787, BD788		–	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.4	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	0.8	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter on Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0) f = 0.1 MHz)	BD785, BD787		–	50	
	BD786, BD788		–	70	
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

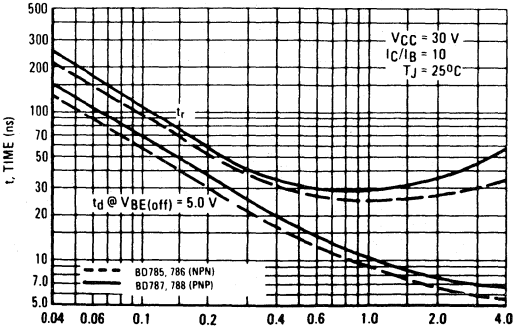


FIGURE 4 – THERMAL RESPONSE

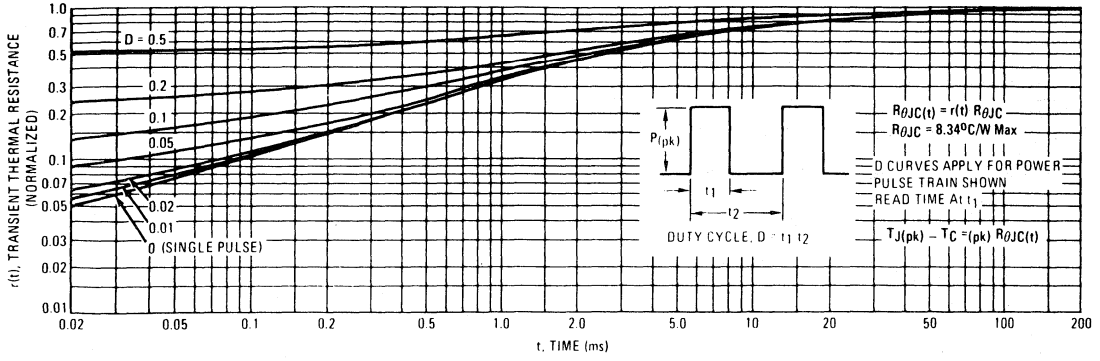
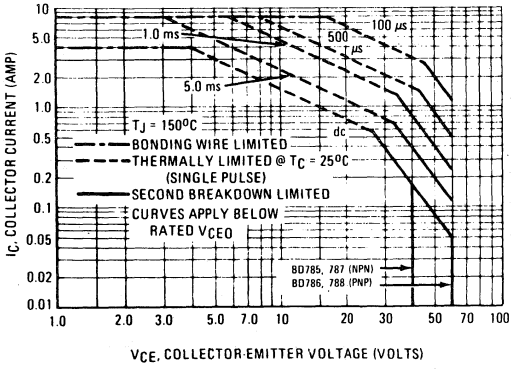


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

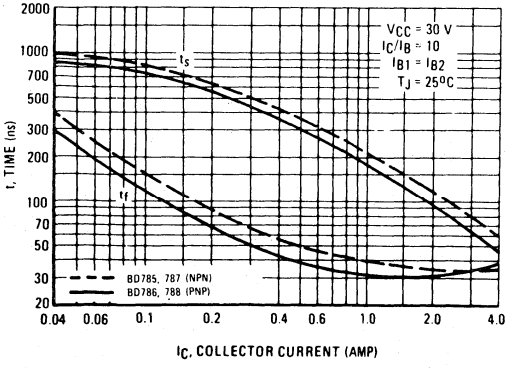
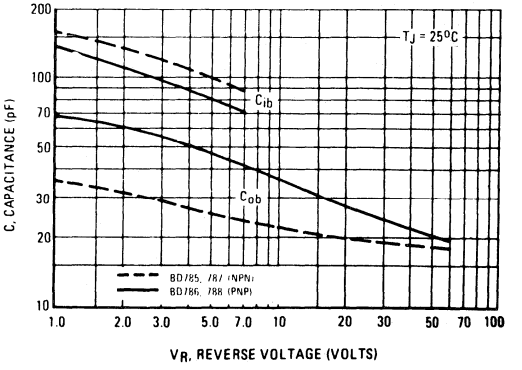


FIGURE 7 – CAPACITANCE



NPN
BD785, BD787

PNP
BD786, BD788

FIGURE 8 – DC CURRENT GAIN

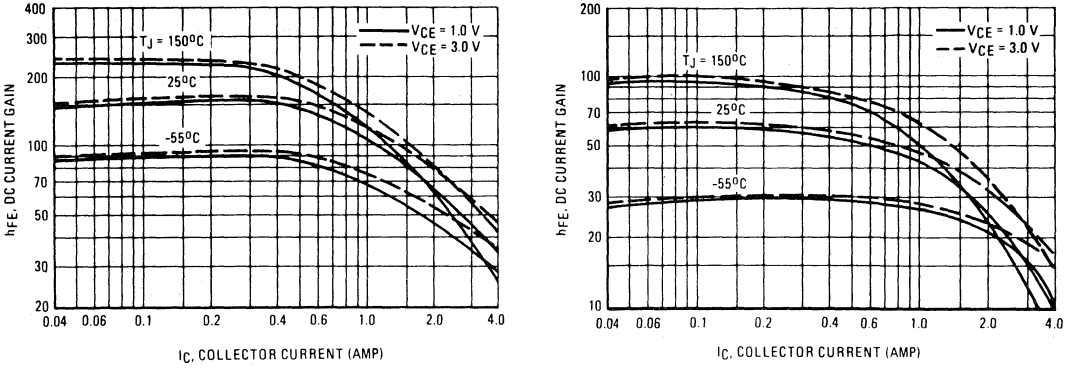


FIGURE 9 – "ON" VOLTAGES

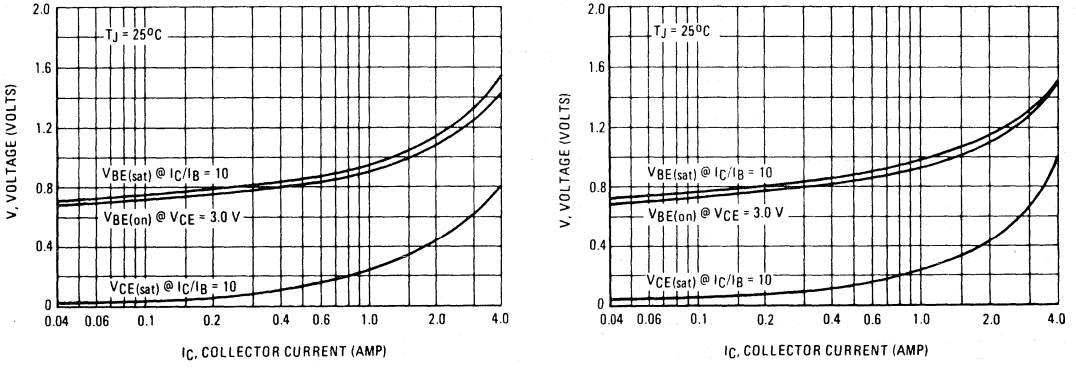
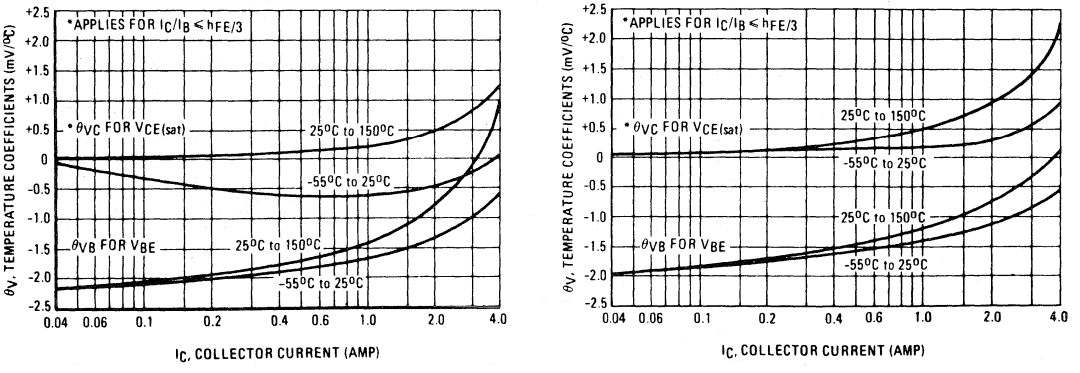


FIGURE 10 – TEMPERATURE COEFFICIENTS



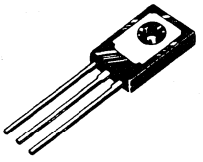
BD789, BD791 (NPN)
BD790, BD792 (PNP)

COMPLEMENTARY PLASTIC SILICON ANNULAR♦ POWER TRANSISTORS

. . . designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 80 Vdc (Min) – BD789, BD790
  = 100 Vdc (Min) –BD791, BD792
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-250
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain – Bandwidth Product –
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)

4 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



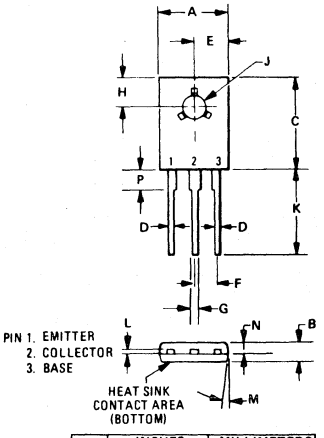
*MAXIMUM RATINGS

Rating	Symbol	BD789 BD790	BD791 BD792	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

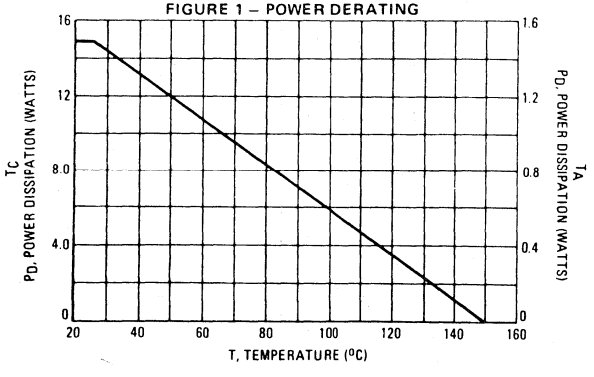
*Indicates JEDEC Registered Data.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.295	0.305	7.490	7.750
B	0.095	0.105	2.410	2.670
C	0.425	0.435	10.800	11.050
D	0.020	0.026	0.508	0.660
E	0.145	0.155	3.680	3.940
F	0.093 TP		2.360 TP	
G	0.025	0.035	0.635	0.889
H	0.148	0.158	3.760	4.010
J	0.115	0.118	2.920	3.000
K	0.595	0.645	15.110	16.380
L	0.015	0.025	0.381	0.635
M	3° TYP		3° TYP	
N	0.045	0.055	1.140	1.400
P	0.085	0.095	2.160	2.410

CASE 77-03

FIGURE 1 – POWER DERATING



♦Annular Semiconductors Patented by Motorola Inc.

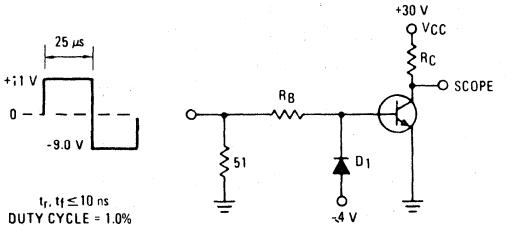
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	BD789, BD790		80	–	
	BD791, BD792		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	BD789, BD790		–	100	
(V_{CE} = 50 Vdc, I_B = 0)	BD791, BD792		–	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD789, BD790		–	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD791, BD792		–	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD789, BD791		–	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD790, BD792		–	0.1	
Emitter Cutoff Current		I_{EBO}	–	1.0	μAdc
(V_{EB} = 6.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			20	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			10	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)			–	2.5	
(I_C = 4.0 Adc, I_B = 800 mAdc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	1.8	Vdc
(I_C = 2.0 Adc, I_B = 200 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 200 mAdc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	40	–	MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz	BD789, BD790		–	50	
	BD791, BD792		–	70	
Small-Signal Current Gain		h_{fe}	10	–	–
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

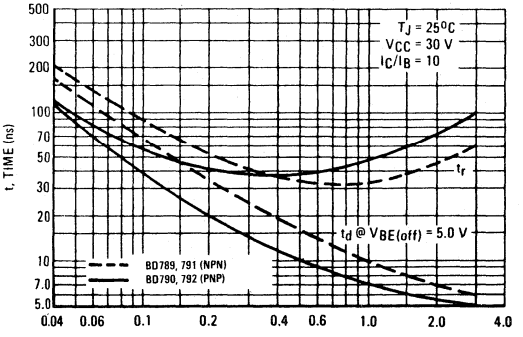


FIGURE 4 – THERMAL RESPONSE

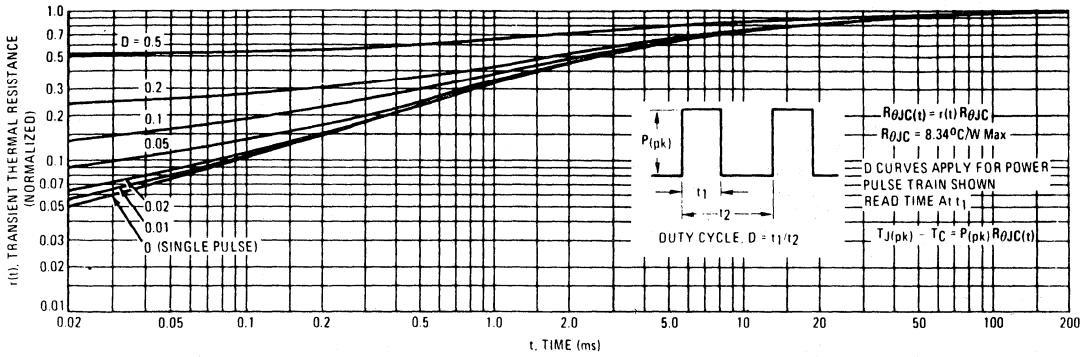
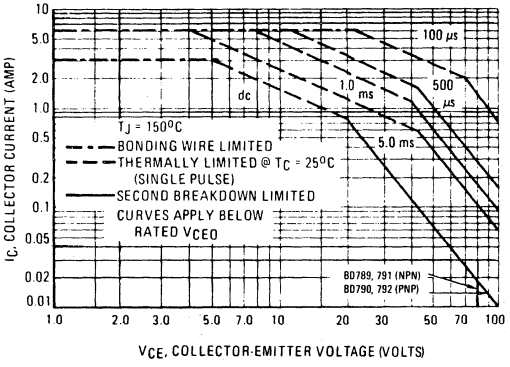


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



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The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

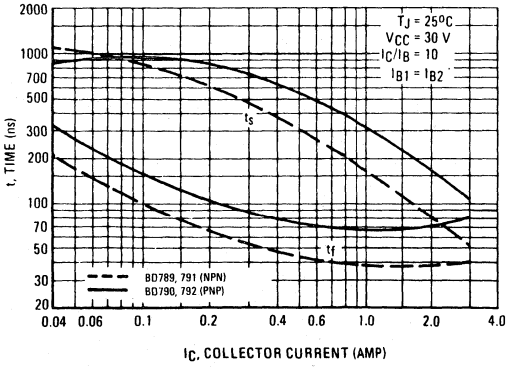
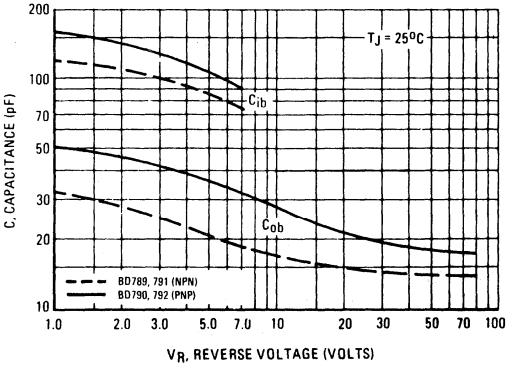


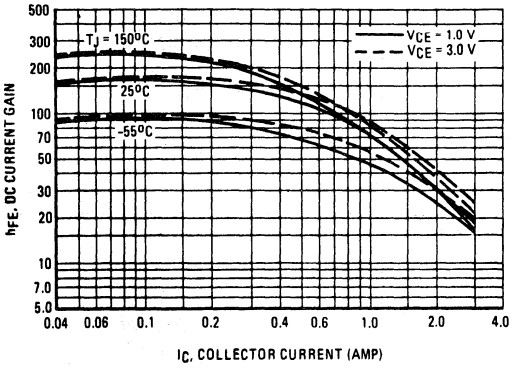
FIGURE 7 – CAPACITANCE



NPN
BD789, BD791

PNP
BD790, BD792

FIGURE 8 – DC CURRENT GAIN



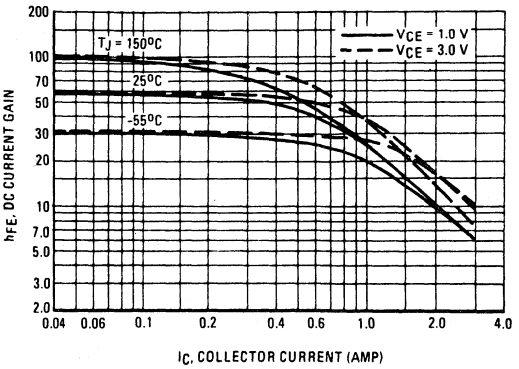
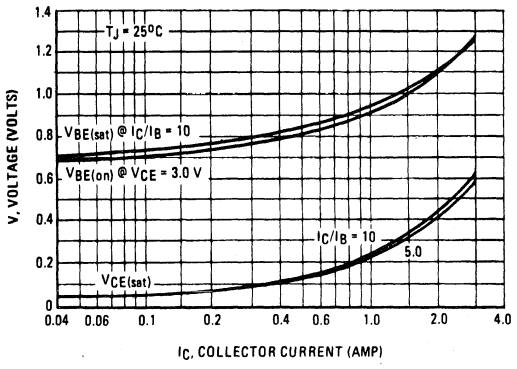


FIGURE 9 – "ON" VOLTAGES



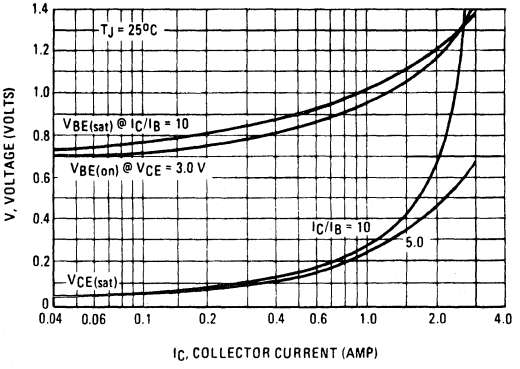
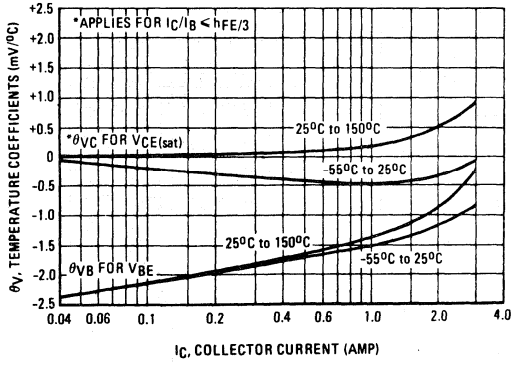
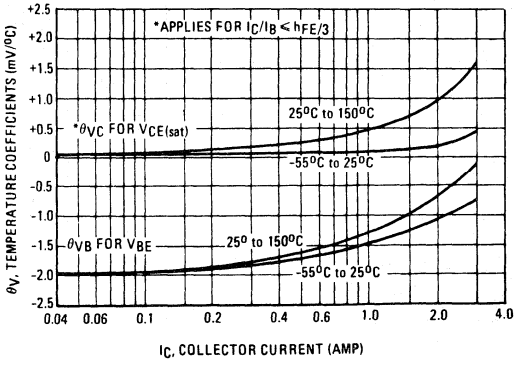


FIGURE 10 – TEMPERATURE COEFFICIENTS





BD795 • BD797
BD799 • BD801

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

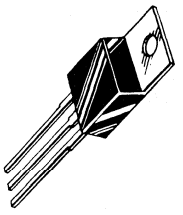
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD 795, 797, 799, 801 are complementary with BD 796, 798, 800, 802

8 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80, 100 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C=25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

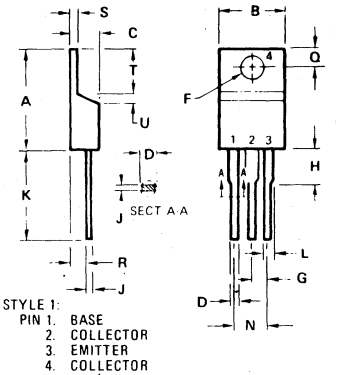
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD795 BD797 BD799 BD801	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	BD795 BD797 BD799 BD801	— — — —	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	BD 795/797 BD 799/801 BD 795/797 BD 799/801	40 30 25 15	— — — —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C =0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.

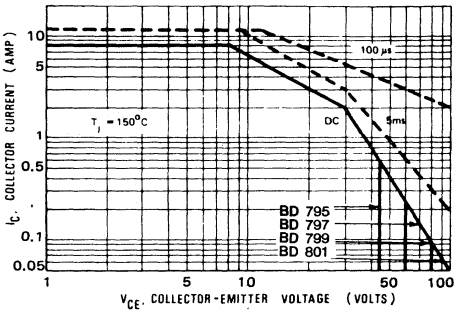


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – COLLECTOR SATURATION REGION

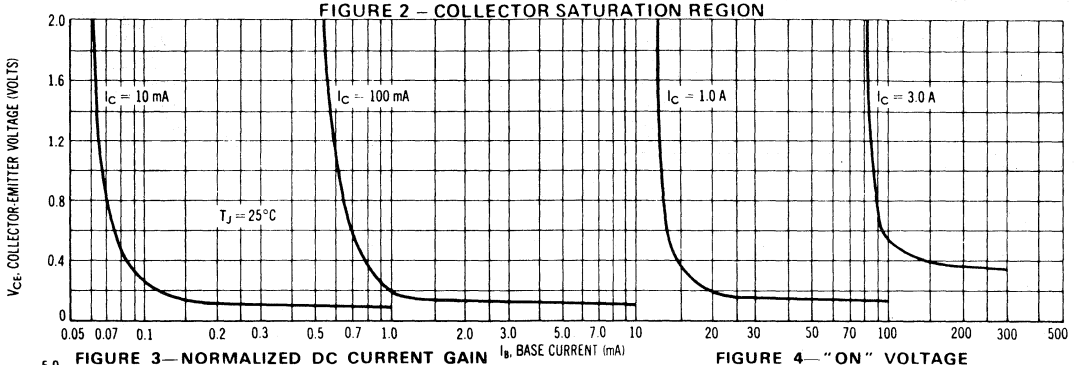


FIGURE 3—NORMALIZED DC CURRENT GAIN

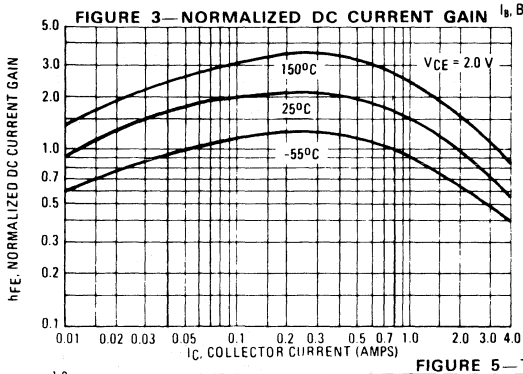


FIGURE 4—"ON" VOLTAGE

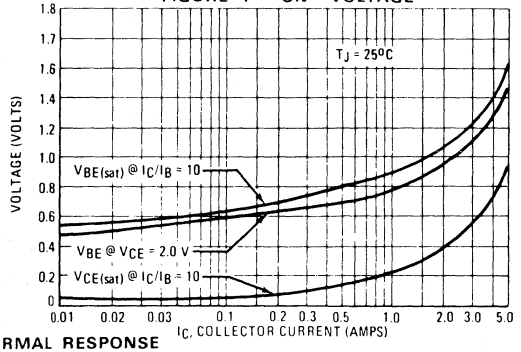
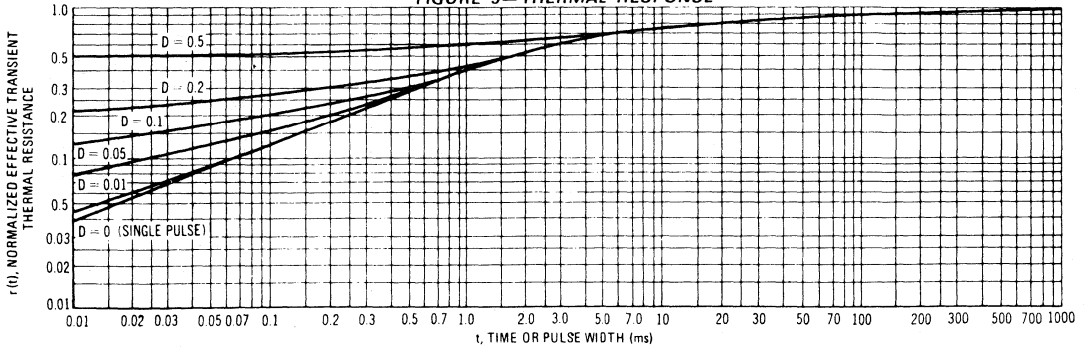


FIGURE 5—THERMAL RESPONSE



BD796 • BD798
BD800 • BD802

PLASTIC HIGH POWER
SILICON PNP TRANSISTOR

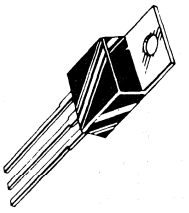
. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain—h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD 796, 798, 800, 802 are complementary with BD 795, 797, 799, 801

8 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80, 100 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation T_C=25°C Derate avove 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

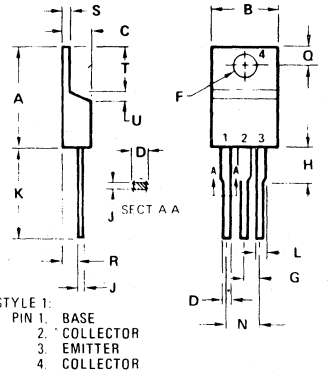
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.92	° C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}*	BD796 BD798 BD800 BD802	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	 BD796 BD798 BD800 BD802	 — — — —	 0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 1 A, V_{CE} = 2 V) (I_C = 3 A, V_{CE} = 2 V)	h_{FE}*	 BD 796/798 BD 800/802 BD 796/788 BD 800/802	 40 30 25 15	 — — — —	
Collector-Emitter Saturation Voltage* (I_C = 3 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$*		—	1.0	Vdc
Base-Emitter On Voltage* (I_C = 3 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C =0.25Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.



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U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

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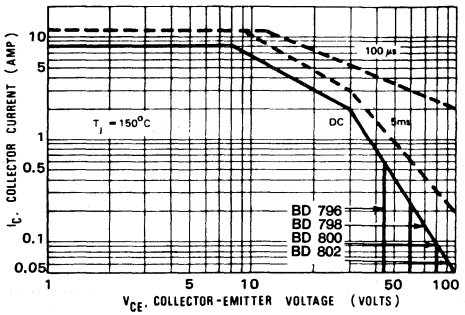

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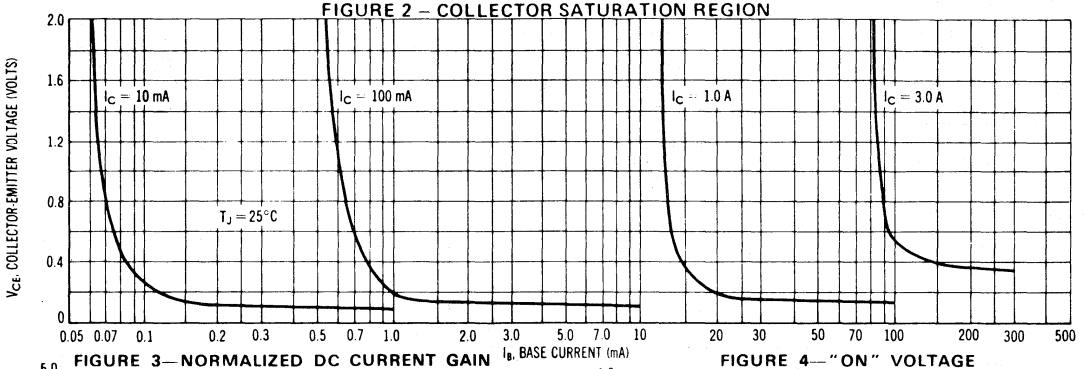
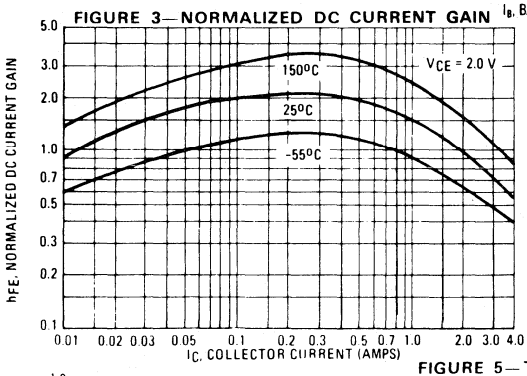


FIGURE 3—NORMALIZED DC CURRENT GAIN



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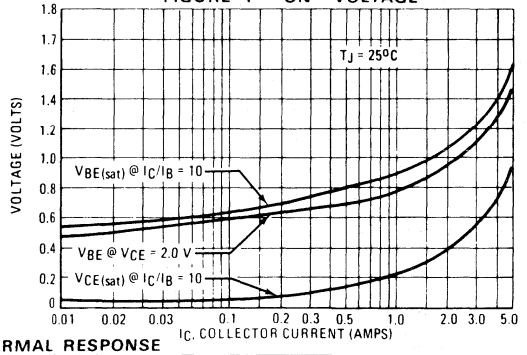
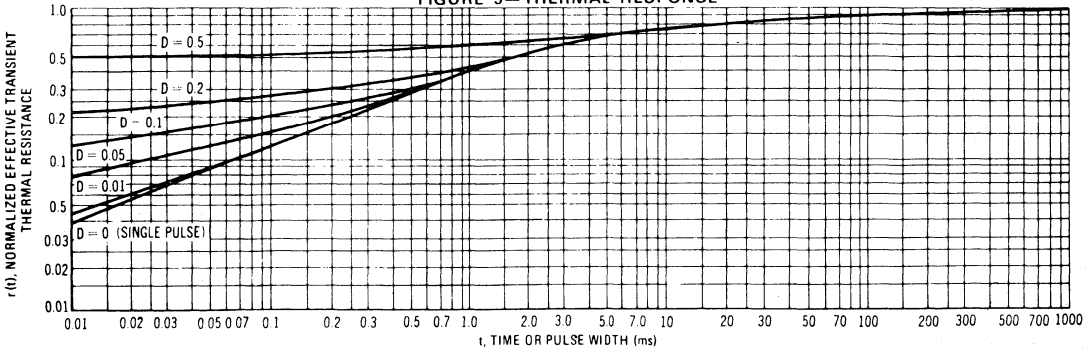


FIGURE 5—THERMAL RESPONSE



BD805
BD807 • BD809

PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

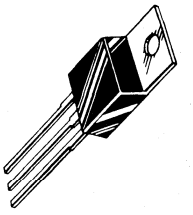
. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current—h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 805, 807, 809 are complementary with BD 806, 808, 810

10 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD805 BD807 BD809	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD805 BD807 BD809	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C=25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		—55 to +150	°C

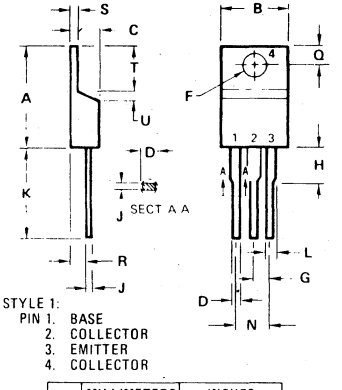
THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}		1.39	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 0.2 Adc, I_B = 0)	BV_{CEO}*	BD805 BD807 BD809	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 55 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	BD805 BD807 BD809	— — —	1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC current Gain (I_C = 2A, V_{CE} = 2 V) (I_C = 4A, V_{CE} = 2 V)	h_{FE}*		30 15	— —	
Collector-Emitter Saturation Voltage* (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$*		—	1.1	Vdc
Base-Emitter On Voltage* (I_C = 4 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1.6	Vdc
Current-Gain-Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
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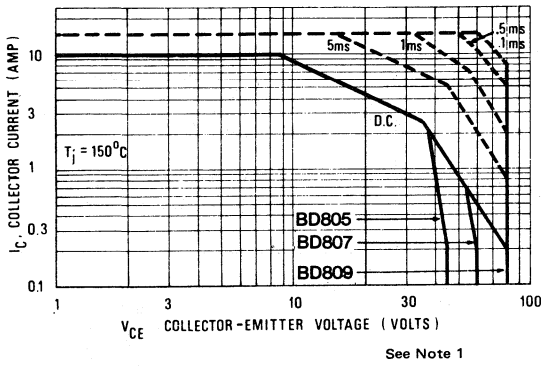
CASE 221A-02
TO-220AB

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA



See Note 1

FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

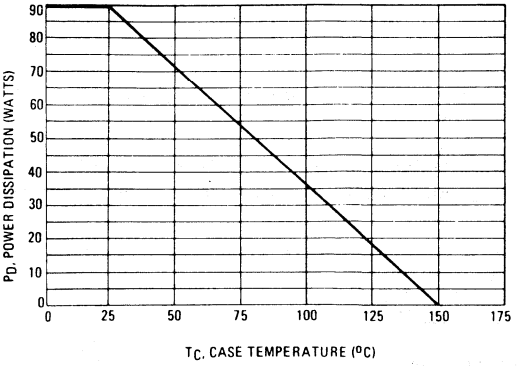


FIGURE 3 — "ON" VOLTAGES

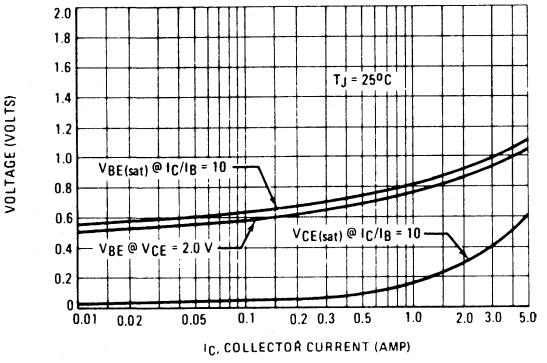
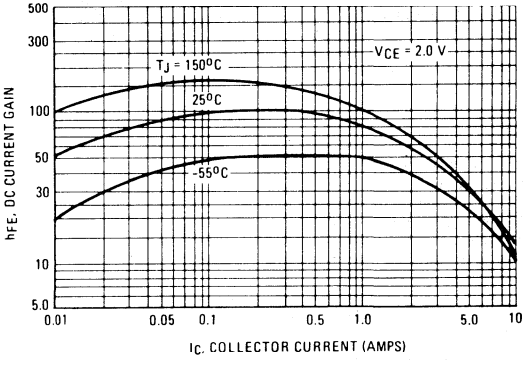


FIGURE 4 — CURRENT GAIN



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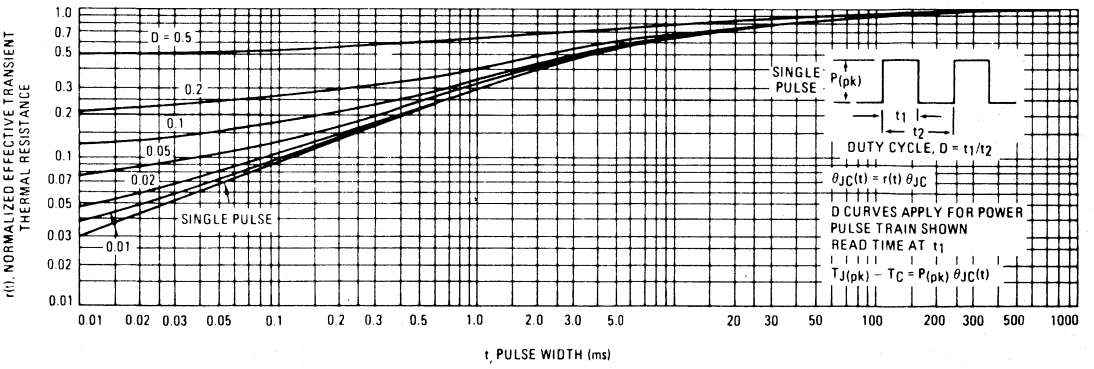

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

BD806
BD808 • BD810

PLASTIC HIGH POWER
SILICON PNP TRANSISTOR

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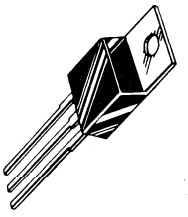

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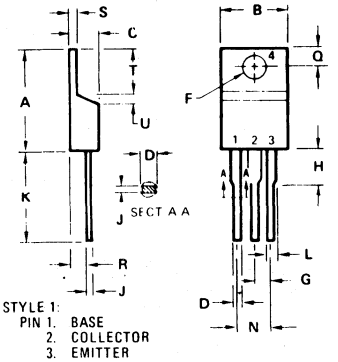

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CASE 221A-02
TO-220AB

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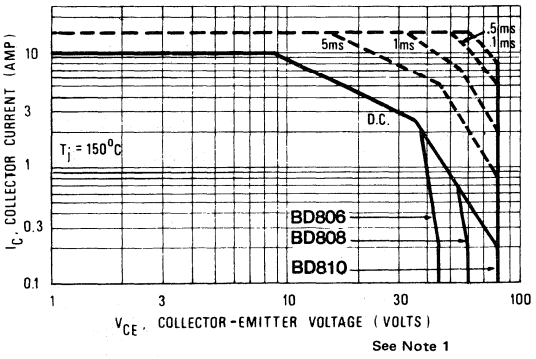

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FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

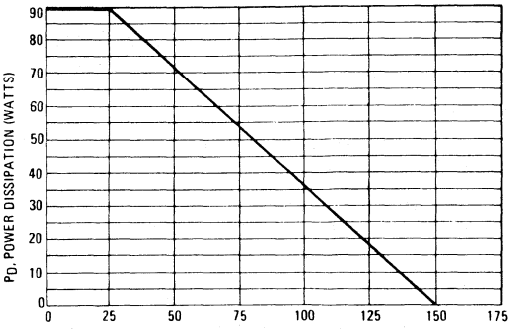


FIGURE 3 — "ON" VOLTAGES

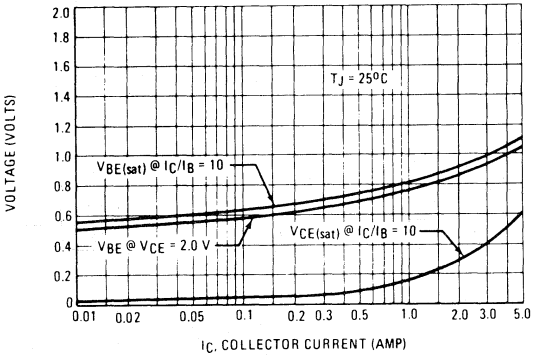


FIGURE 4 — CURRENT GAIN

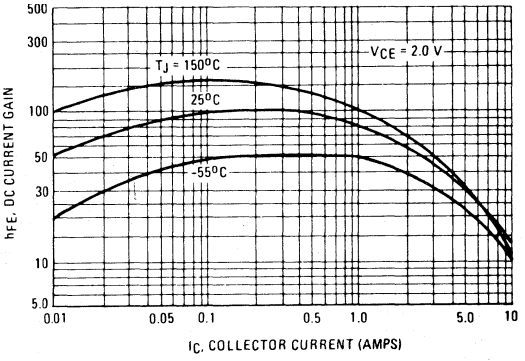
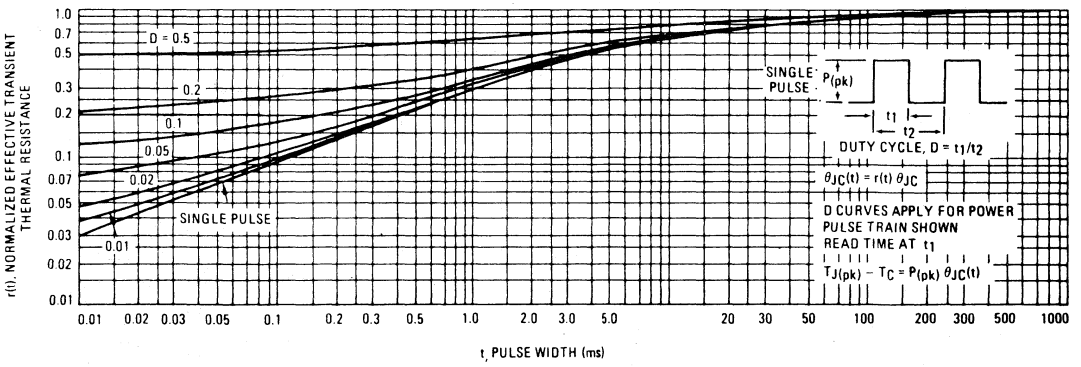


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

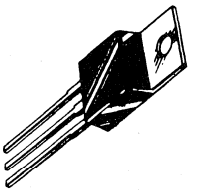
BD895, 895A • BD897, 897A
BD899, 899A • BD901

PLASTIC MEDIUM-POWER
PNP TRANSISTORS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain –
  h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- BD895A, 897, 897A, 899, 899A, 901 are complementary with BD896A, 898, 898A, 900, 900A, 902
- Electrical equivalents to BD695A, 697, 697A, 699, 699A, 701

DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTORS
45-60-80-100 VOLTS
70 WATTS



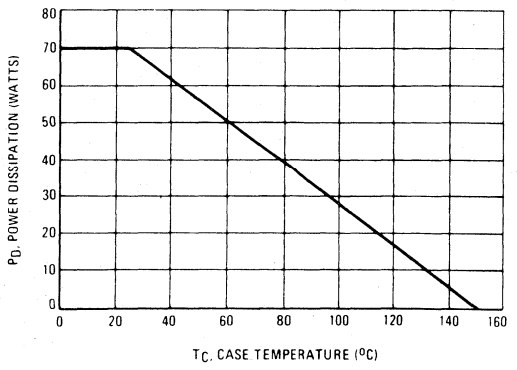
MAXIMUM RATINGS

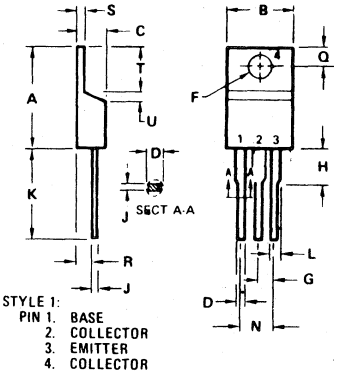
Rating	Symbol	BD895 BD895A	BD897 BD897A	BD899 BD899A	BD901	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

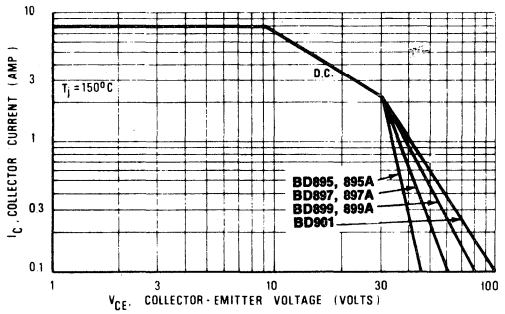
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD895, 895A BD897, 897A BD899, 899A BD901	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	h_{FE}	750 750	– –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 4.0 Adc, I_B = 16 mAdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{CE(sat)}$	– –	2.5 2.8	Vdc
Base-Emitter On Voltage[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{BE(on)}$	– –	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

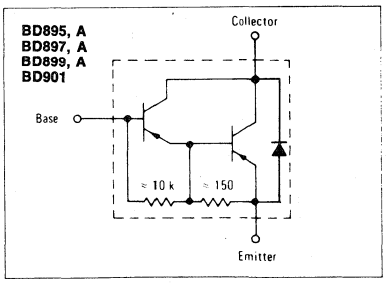
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate i_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



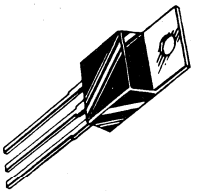
BD896, 896A • BD898, 898A
BD900, 900A • BD902

PLASTIC MEDIUM-POWER PNP TRANSISTORS

. . . for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- Monolithic Construction
- **BD896A, 898, 898A, 900, 900A, 902 are complementary with BD895A, 897, 897A, 899, 899A, 901**
- **Electrical equivalents to BD696A, 698, 698A, 700, 700A, 702**

DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTORS
45-60-80-100 VOLTS
70 WATTS



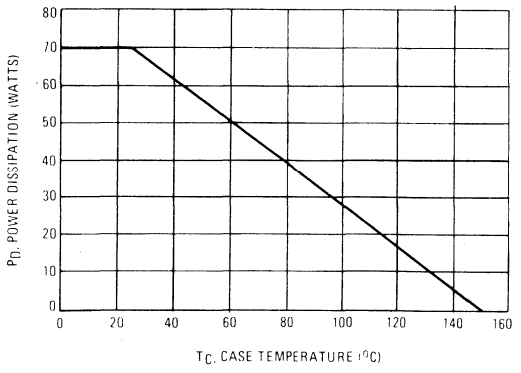
MAXIMUM RATINGS

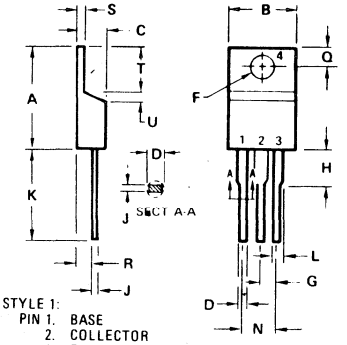
Rating	Symbol	BD696 BD696A	BD898 BD898A	BD900 BD900A	BD902	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
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N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

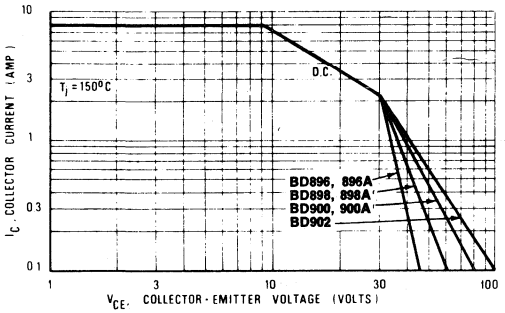
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage[1] (I_C = 100 mAdc, I_B = 0)	BD896, 896A BD898, 898A BD900, 900A BD902	BV_{CEO}	45 60 80 100	– – – –	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	 BD896, 898, 900, 902 BD896A, 898A, 900A	h_{FE}	 750 750	 – –	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 4.0 Adc, I_B = 16 mAdc)	 BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{CE(sat)}$	 – –	 2.5 2.8	Vdc
Base-Emitter On Voltage[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	 BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{BE(on)}$	 – –	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

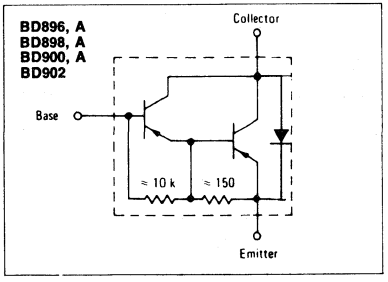
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



BDX53, 53A, 53B, 53C (NPN)
BDX54, 54A, 54B, 54C (PNP)

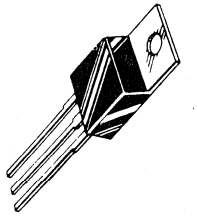
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BDX53, 54
  = 60 Vdc (Min) — BDX53A, 54A
  = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
65 WATTS



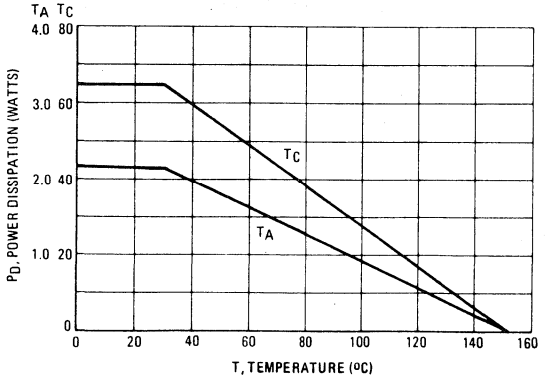
*MAXIMUM RATINGS

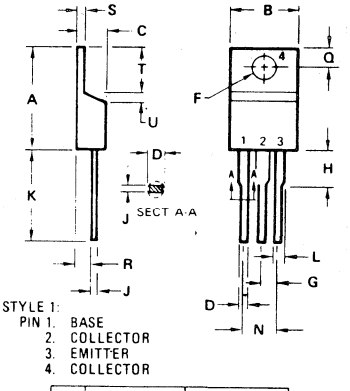
Rating	Symbol	BDX53 BDX54	BDX53A BDX54A	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	8				Adc
Peak		12				
Base Current	I_B	0.2				Adc
Total Device Dissipation @ T_C = 25°C	P_D	60				Watts
Derate above 25°C		0.48				W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
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Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BDX53, BDX54	$V_{CEO(sus)}$	45		Vdc
	BDX53A, BDX54A		60	–	
	BDX53B, BDX54B		80	–	
	BDX53C, BDX54C		100	–	
Collector Cutoff Current		I_{CEO}		0.5	mAdc
(V_{CE} = 22 Vdc, I_B = 0)	BDX53, BDX54		–	0.5	
(V_{CE} = 30 Vdc, I_B = 0)	BDX53A, BDX54A		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	BDX53B, BDX54B		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	BDX53C, BDX54C				
Collector Cutoff Current		I_{CBO}		0.2	mAdc
(V_{CB} = 45 Vdc, I_E = 0)	BDX53, BDX54		–	0.2	
(V_{CB} = 60 Vdc, I_E = 0)	BDX53A, BDX54A		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	BDX53B, BDX54B		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	BDX53C, BDX54C				
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}	750	–	–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)				–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
			–	4.0	
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)		$V_{BE(sat)}$	–	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53, 53A, 53B, 53C		–	300	
	BDX54, 54A, 54B, 54C		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

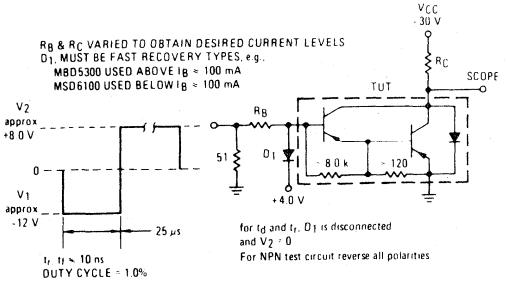


FIGURE 3 – SWITCHING TIMES

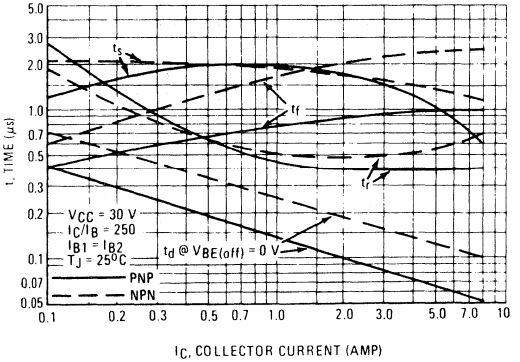


FIGURE 4 – THERMAL RESPONSE

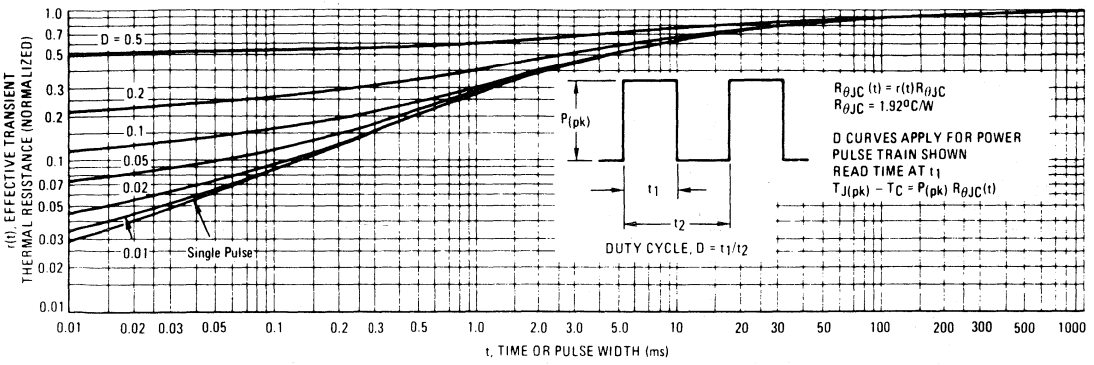
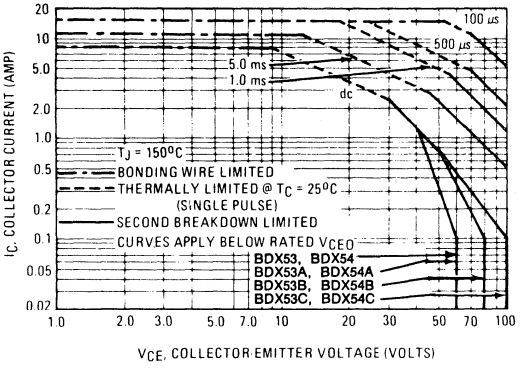


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

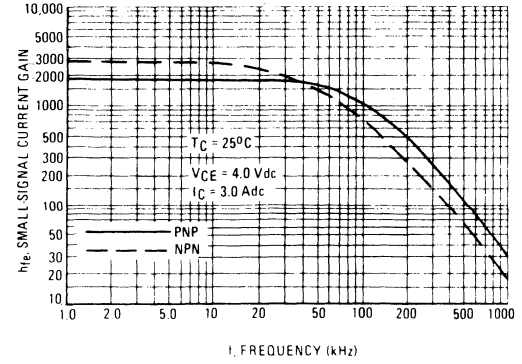
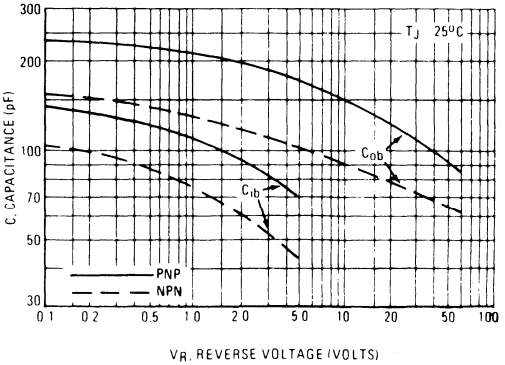


FIGURE 7 – CAPACITANCE



NPN

BDX53, BDX53A, BDX53B, BDX53C

PNP

BDX54, BDX54A, BDX54B, BDX54C

FIGURE 8 – DC CURRENT GAIN

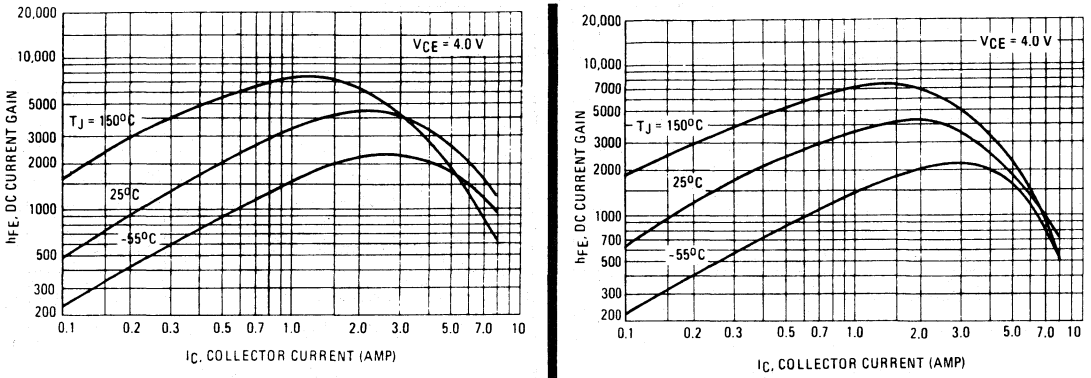


FIGURE 9 – COLLECTOR SATURATION REGION

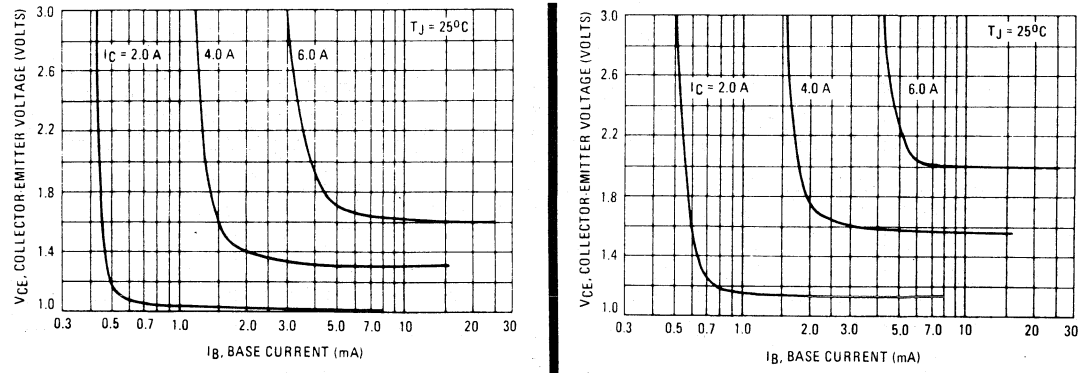
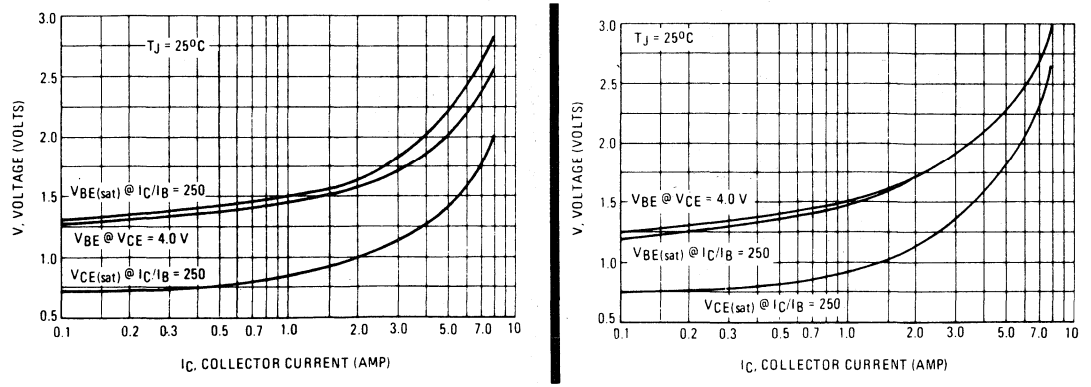


FIGURE 10 – "ON" VOLTAGES



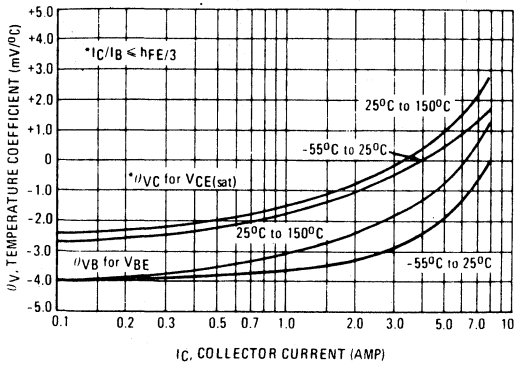
NPN

BDX53, BDX53A, BDX53B, BDX53C

PNP

BDX54, BDX54A, BDX54B, BDX54C

FIGURE 11 – TEMPERATURE COEFFICIENTS



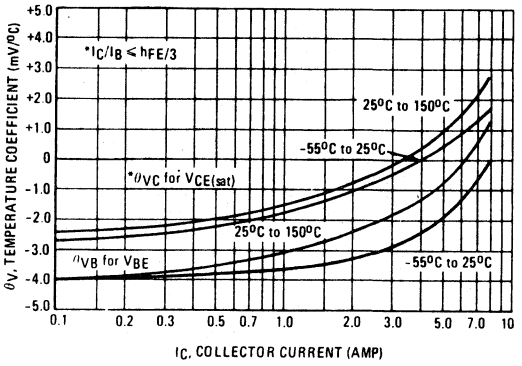
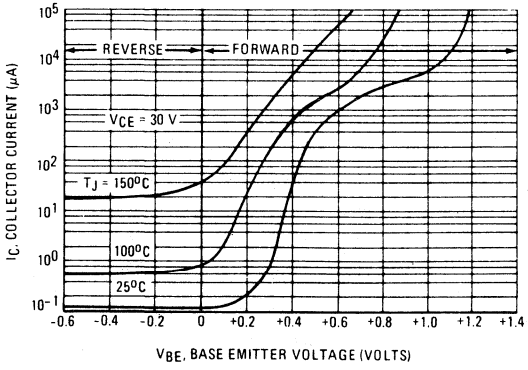


FIGURE 12 – COLLECTOR CUT-OFF REGION



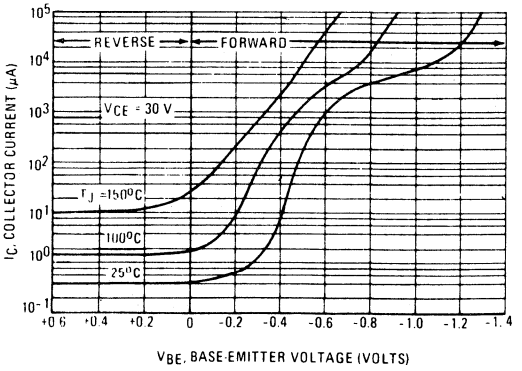
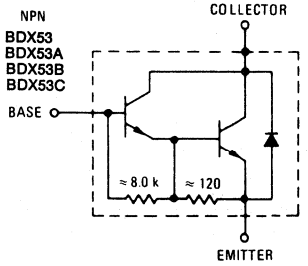
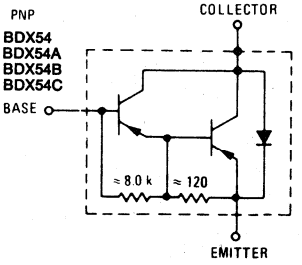


FIGURE 13 – DARLINGTON SCHEMATIC





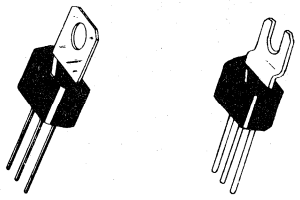
BF380
BF381 • BF382

NPN SILICON ANNULAR* TRANSISTORS

. . . designed for high-voltage video and luminance output stages in TV receivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 300, 250, and 180 Vdc @ I_C = 10 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance —
  C_{cb} = 3.0 pF (Max) @ V_{CB} = 30 Vdc

NPN SILICON HIGH VOLTAGE AMPLIFIER TRANSISTORS



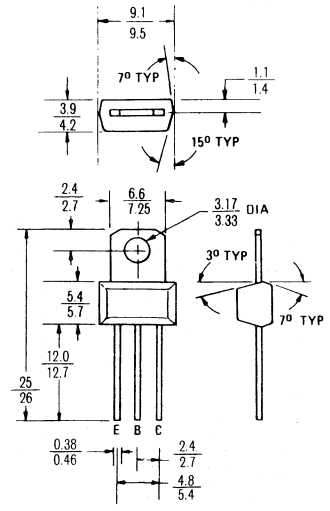
(1) Standard package: BF380/381/382.
(2) Tab formed for flat mounting:
BF380-1/BF381-1/BF382-1
Leads formed to TO-5 configuration:
BF380-5/BF381-5/BF382-5

MAXIMUM RATINGS

Rating	Symbol	BF 380	BF 381	BF 382	Unit
Collector-Emitter Voltage	V_{CEO}	180	250	300	Vdc
Collector-Base Voltage	V_{CB}	180	250	300	Vdc
Emitter-Base Voltage	V_{EB}	—	5	—	Vdc
Collector Current—Continuous	I_C	—	500	—	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
Collector connected to tab

CASE 152

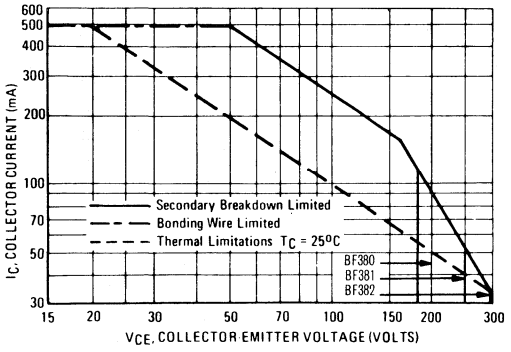
* Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}				Vdc
(I_C = 10 mAdc, I_B = 0)	BF 380		180	—	—	
	BF 381		250	—	—	
	BF 382		300	—	—	
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 100 μAdc, I_E = 0)	BF 380		180	—	—	
	BF 381		250	—	—	
	BF 382		300	—	—	
Emitter-Base Breakdown Voltage		BV_{EBO}		—	—	Vdc
(I_E = 10 μAdc, I_C = 0)			5.0			
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 100 Vdc, I_E = 0)	BF 380		—	—	50	
(V_{CB} = 200 Vdc, I_E = 0)	BF 381		—	—	50	
(V_{CB} = 250 Vdc, I_E = 0)	BF 382		—	—	50	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}		—	—	—
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			25			
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 30 mAdc, I_B = 6.0 mAdc)			—	0.3	0.75	
Collector-Emitter Knee Voltage (T_J = 150 °C)		V_{CEK}				Vdc
(I_C = 30 mAdc) (2)			—	11	—	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product		f_T				MHz
(I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)			—	90	—	
Collector-Base Capacitance		C_{CB}				Pf
(V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)			—	2.2	3.0	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Value of V_{CE} at which h_{FE} is 80% of its value at V_{CE} = 50 Vdc, I_C = 30 mAdc.

GURE 1 -- DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C—V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2—DC CURRENT GAIN

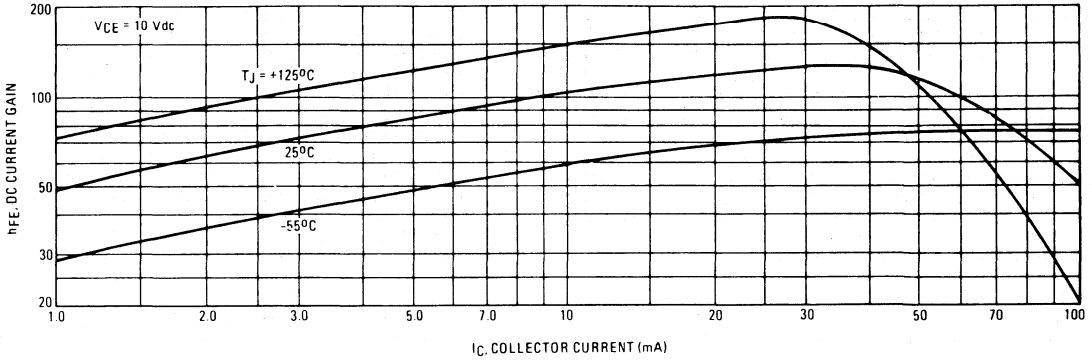


FIGURE 3—CAPACITANCES

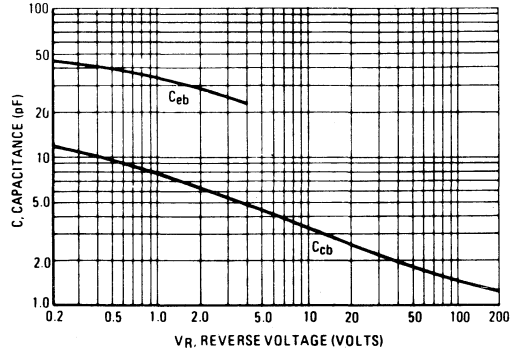


FIGURE 4—CURRENT-GAIN—BANDWIDTH PRODUCT

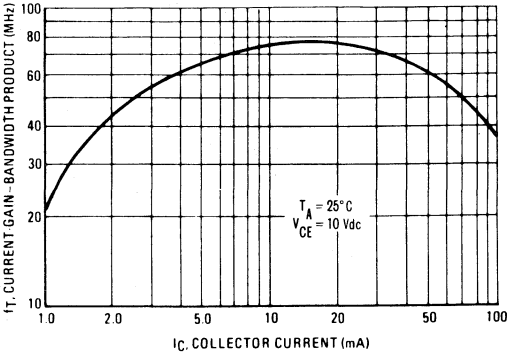
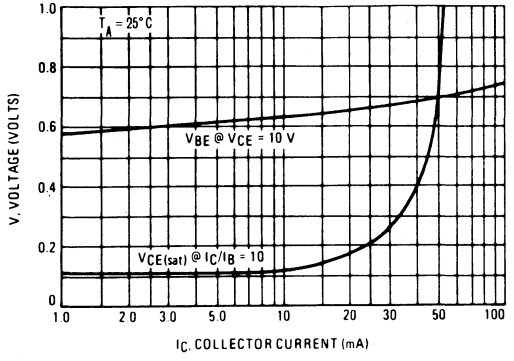


FIGURE 5—"ON" VOLTAGES



APPLICATIONS INFORMATION

The BF 382 is primarily designed for use in the R, G, and B output stages of color television receivers and with a high BV_{CEO}, it can supply the video amplitude requirements of any known system. The low feedback capacitance provides good video bandwidth with modest drive current requirements. Typical drive is from an emitter-follower with a 4.7 k emitter-resistor operated from a 20-Volt supply. It will, therefore, be operable directly from a number of available chroma demodulators. The low output capacitance of this device adds little to the total load capacitance, allowing improved bandwidth for a given collector load resistor. Two typical applications for the BF 382 are shown in Figures 6 and 7.

Device dissipation will reach approximately 1.6 Watts under worst-case signal conditions and some heat sinking is required. At an operating ambient temperature of 65°C, a thermal resistance $\theta_{JA} = 150\text{-}65/1.6 = 53\,^{\circ}C/W$ will be required. The junction-to-case thermal resistance, θ_{JC}, of the device is 12.5°C/W, thus a heat dissipator of 40.5°C/W, or lower, will be required. A black anodized 0.020" thick aluminum plate measuring 1" × 2" can be folded into a channel shape and formed with «feet» to snap into a printed circuit panel for support. This will provide the safety factor.

Used as a color difference output, where drive and bandwidth requirements are less severe, the BF 382 can be operated with 27 k ohm load resistors (worst-case dissipation would then be only 0.6 Watts). The device can, therefore, be operated as a color-difference output without any heat radiator in ambient temperatures to 150-0.6 (125) = 75°C.

In addition the safe operating area of the BF 382 will fill the requirements of the luminance output function with a total equivalent load of 5.0 kilohms. Worst-case dissipation can reach 3 Watts, this requires a total θ_{JA} of 150-65/3 = 28.4°C/W. This 28.4°C/W means a heat dissipator of 15.9°C/W, (approximately 2" × 3" aluminum plate) will be required.

FIGURE 6—BF 382 AS RGB OUTPUT, MATRIXING COLOR DIFFERENCE AND LUMINANCE INPUTS

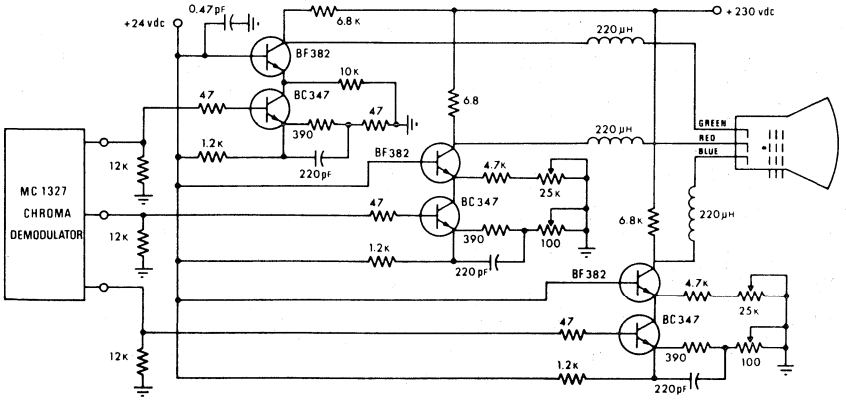


FIGURE 7—HEAT SINK VERSUS SURFACE AREA

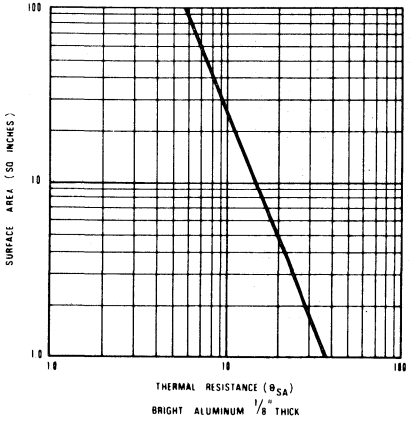
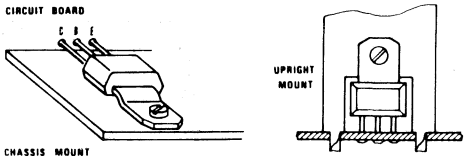


FIGURE 8—TYPICAL THERMAL RESISTANCE DATA—TAB TO SINK

CONDITION	θ_{CS} in °C/W	MOUNTING SCREW TORQUE (in/lbs)
NO GREASE	4.25	5
WITH DOW-340	2.1	2
THERMAL COMPOUND	1.7	5
WITH DOW-340 AND 2 MIL	4.7	2
MICA WASHER	4.3	5

FIGURE 9—TYPICAL MOUNTING METHODS

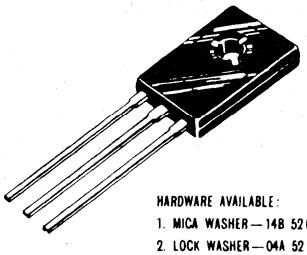


BF457
BF458 • BF459

NPN PLANAR SILICON MEDIUM
POWER TRANSISTORS

- For Video output Stages in Television Receivers

0.1 AMPERE
POWER TRANSISTOR
NPN SILICON



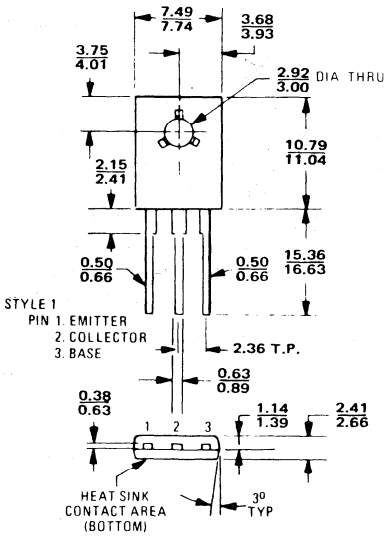
HARDWARE AVAILABLE:
1. MICA WASHER—14B 52600 F03
2. LOCK WASHER—04A 52200 F01

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BF457 BF458 BF459	160 250 300	Vdc
Collector-Base Voltage	V_{CBO}	BF457 BF458 BF459	160 250 300	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		0.1	Adc
Base Current	I_B		0.05	Adc
Total Device Dissipation $T_A = 25^o$ C $T_C = 25^o$ C Derate above 25° C	P_D		 1.2 12.5 100	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−55 to + 150	°C

THERMAL CHARACTERISTICS

	Symbol		Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}		10	°C/W



When mounting the device, torque not to exceed 0.07 m-kg

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend

All dimensions in millimeters

CASE 77-03

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ C unless otherwise noted)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage ($I_C = 100\mu A$, $I_B = 0$)	BF457 BF458 BF459	BV_{CEO}	160 250 300			Vdc
Collector-Base Breakdown Voltage ($I_C = 100\mu A$, $I_B = 0$)	BF457 BF458 BF459	BV_{CBO}	160 250 300			Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\mu A$, $I_C = 0$)		BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB}=100V, I_E=0) (V_{CB}=200V, I_E=0) (V_{CB}=250V, I_E=0)	BF457 BF458 BF459	I_{CBO}			50 50 50	nA dc
Emitter Cutoff Current ($V_{EB} = 3V$)		I_{EBO}			50	nA dc
DC Current Gain ($I_C = 30$ mA, $V_{CE} = 10V$)		h_{FE}	25			
Collector Emitter Saturation Voltage ($I_C = 30$ mA, $I_B = 6$ mA)		$V_{CE\ (Sat)}$			1.0	Vdc
Feedback Capacitance (V_{CB}= 30 V, $I_E = 0$, f = 1 MHz)		C_{12e}		4.2		pF
Output Capacitance (V_{CB}= 30V, $I_E = 0$, f = 1 MHz)		C_{22e}		5.5		pF
Current Gain-Bandwidth Product (V_{CE}= 10V, I_C = 15 mA, f = 20 MHz)		f_T		90		MHz

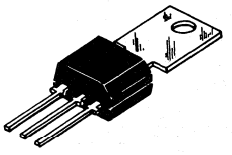
BF460
BF461 • BF462

NPN SILICON ANNULAR♦ HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – BF462
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance – C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package – 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to PNP BF463/464/465

NPN SILICON AMPLIFIER TRANSISTORS



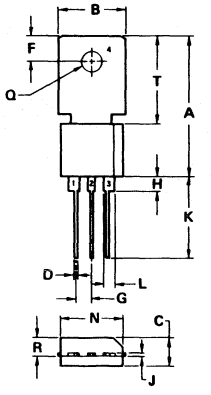
MAXIMUM RATINGS

Rating	Symbol	BF460	BF461	BF462	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	← 6.0 →			Vdc
*Collector Current – Continuous Peak	I_C	← 0.5 → ← 0.7 →			Adc
*Base Current	I_B	← 250 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

♦Annular Semiconductors Patented by Motorola Inc.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

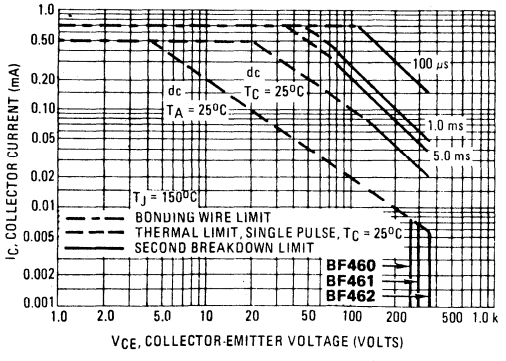
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	BF460		250	–	
	BF461		300	–	
	BF462		350	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BF460		250	–	
	BF461		300	–	
	BF462		350	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	6.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF460		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF461		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF462		–	0.2	
Emitter Cutoff Current		I_{EBO}	–	0.1	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.6	
(I_C = 50 mAdc, I_B = 5 mAdc)			–	1.5	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.0	Vdc
(I_C = 30 mAdc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	45	200	MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)					
Common-Emitter Reverse Transfer Capacitance		Cre	–	3.0	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

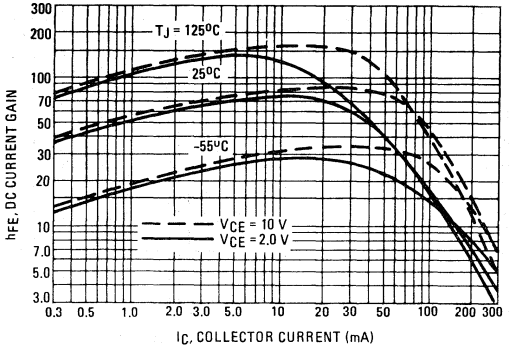


FIGURE 3 – "ON" VOLTAGES

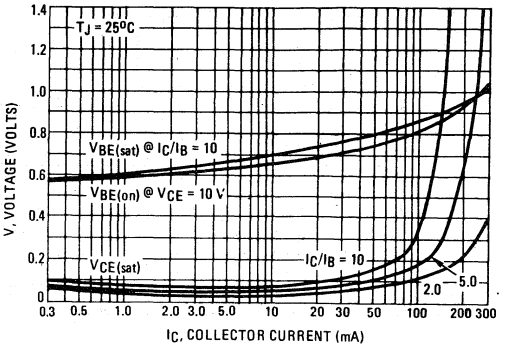


FIGURE 4 – COLLECTOR SATURATION REGION

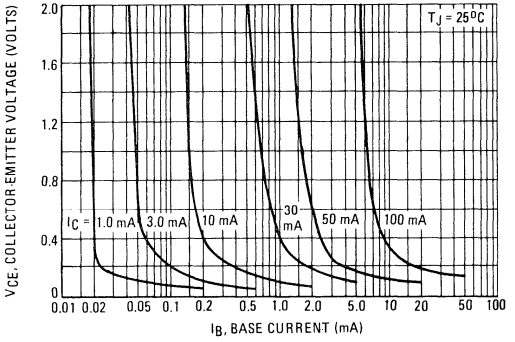


FIGURE 5 – TEMPERATURE COEFFICIENTS

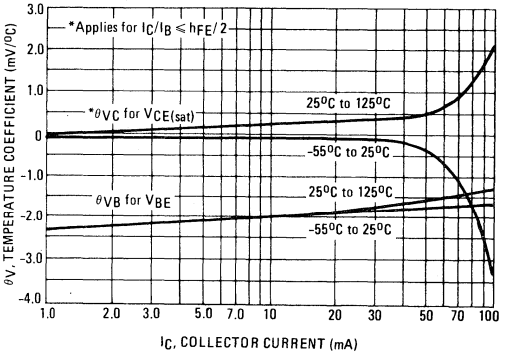
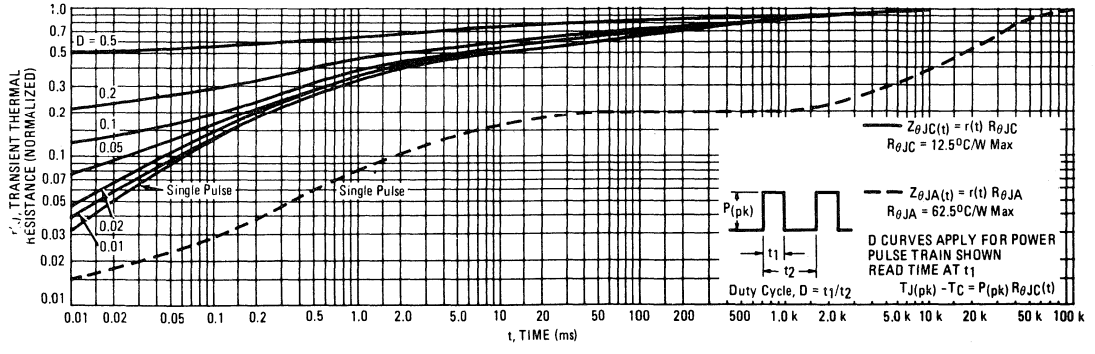


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

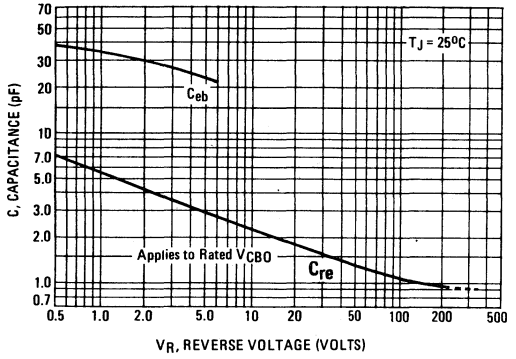
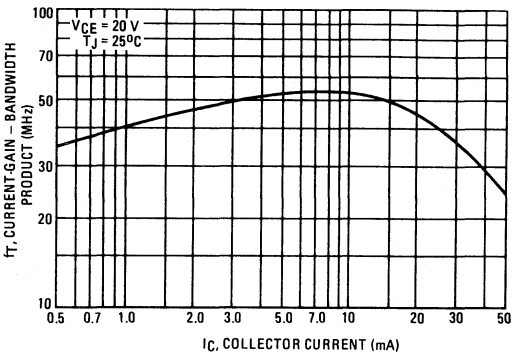


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT



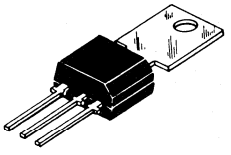
BF463
BF464 • BF465

PNP SILICON ANNULAR♦ HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – BF465
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75V (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance –
  C_{re} = 3.0 pF (Max) @ V_{CB} = 60 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complementary to NPN BF460/BF461/BF462

PNP SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

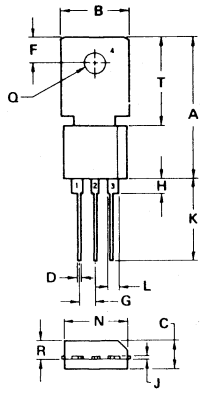
Rating	Symbol	BF463	BF464	BF465	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	← 5 V →			Vdc
*Collector Current – Continuous Peak	I_C	← 0.5 → ← 0.7 →			Adc
*Base Current	I_B	← 250 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.

♦Annular Semiconductors Patented by Motorola Inc.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

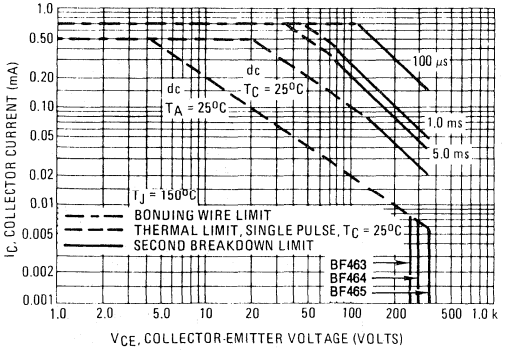
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF463	BV_{CEO}	250	–	Vdc
	BF464		300	–	
	BF465		350	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF463	BV_{CBO}	250	–	Vdc
	BF464		300	–	
	BF465		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF463		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF464		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF465		–	0.2	
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)		$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	20	200	MHz
Common Emitter Reverse Transfer Capacitance (V_{CB} = 60 Vdc, I_E = 0, f = 1.0 MHz)		Cre	–	3.0	pF

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

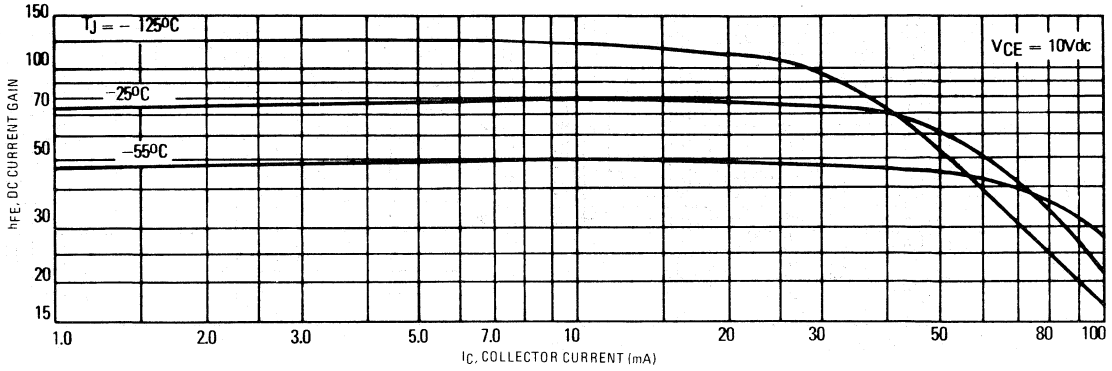


FIGURE 2 – DC CURRENT GAIN

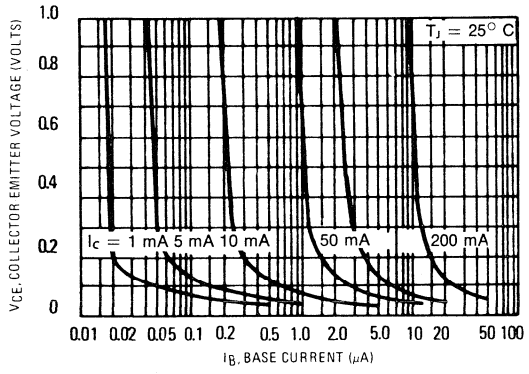


FIGURE 3 – COLLECTOR SATURATION REGION

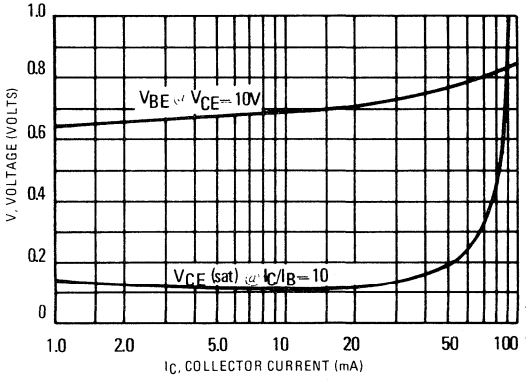


FIGURE 4 – "ON" VOLTAGES

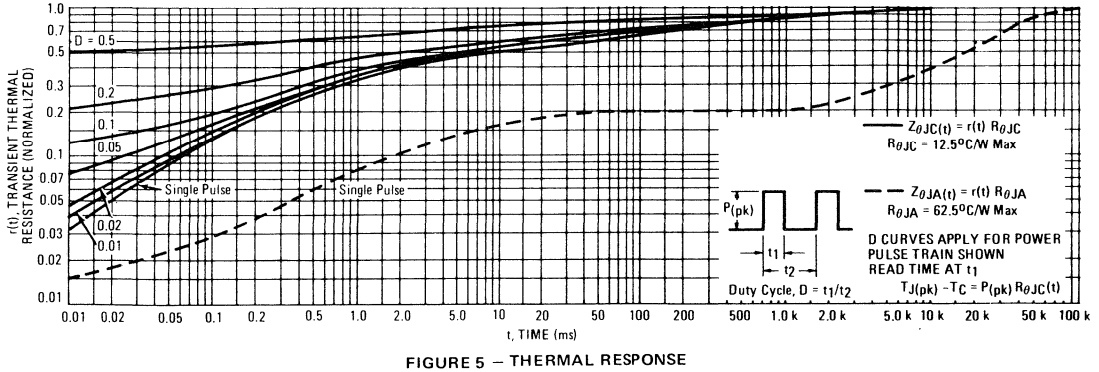


FIGURE 5 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

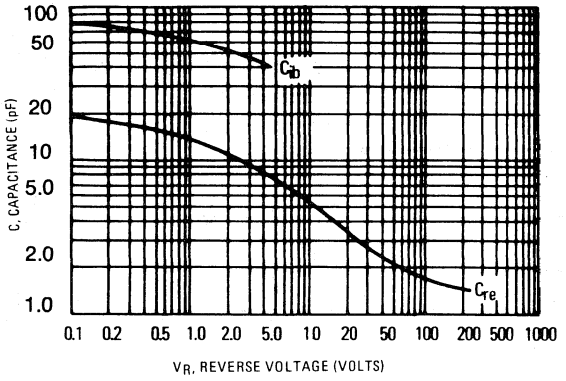


FIGURE 6 – CAPACITANCE

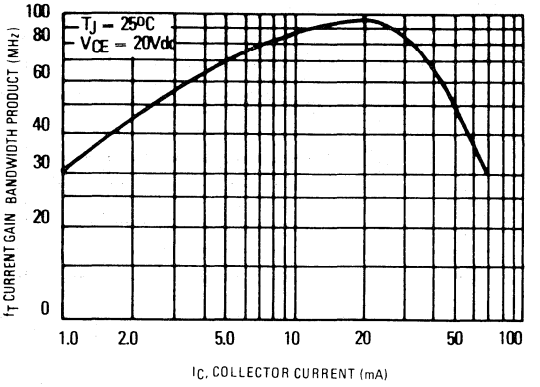


FIGURE 7 – CURRENT-GAIN – BANDWIDTH PRODUCT

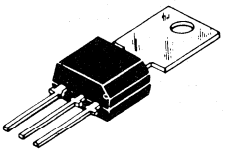
BF466
BF467 • BF468

NPN SILICON ANNULAR ♦
HIGH VOLTAGE AMPLIFER TRANSISTORS

. . . designed for horizontal driver applications in television receivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 250 Vdc (Min) @ I_C = 1.0 mAdc — BF468
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1 Vdc (Max) @ I_C = 200 mAdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

NPN SILICON
AMPLIFIER TRANSISTORS



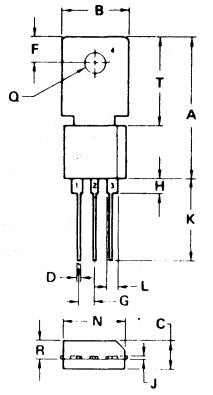
MAXIMUM RATINGS

Rating	Symbol	BF466	BF467	BF468	Unit
*Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
*Collector-Base Voltage	V_{CBO}	150	200	250	Vdc
*Emitter-Base Voltage	V_{EBO}	5			Vdc
*Collector Current – Continuous Peak	I_C	1 2			Adc
*Base Current	I_B	300			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

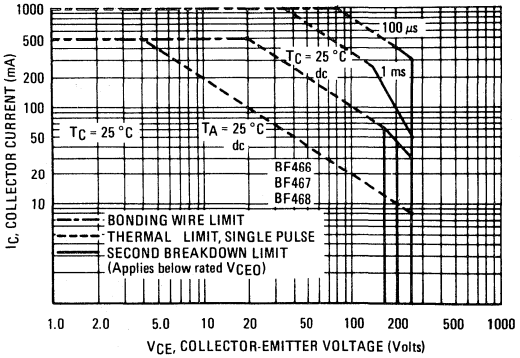
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

♦Annular Semiconductors Patented by Motorola Inc.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF466	BV_{CEO}	150	–	Vdc
	BF467		200	–	
	BF468		250	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF466	BV_{CBO}	150	–	Vdc
	BF467		200	–	
	BF468		250	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100, Vdc, I_E = 0)	BF466		–	0.1	
(V_{CB} = 150, Vdc, I_E = 0)	BF467		–	0.1	
(V_{CB} = 200, Vdc, I_E = 0)	BF468		–	0.1	
Emitter Cutoff Current (V_{BE} = 4 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mA, V_{CE} = 10 Vdc)	BF466		40	–	
(I_C = 100 mA, V_{CE} = 10 Vdc)	BF467		30		
	BF468		30		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 200 mAdc, I_B = 20 mAdc)			–	1.5	
Base-Emitter On Voltage (I_C = 200 mA, V_{CE} = 1 Vdc)		$V_{BE(on)}$	35	1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mA, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35		MHz
Collector output capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	110	pF



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS

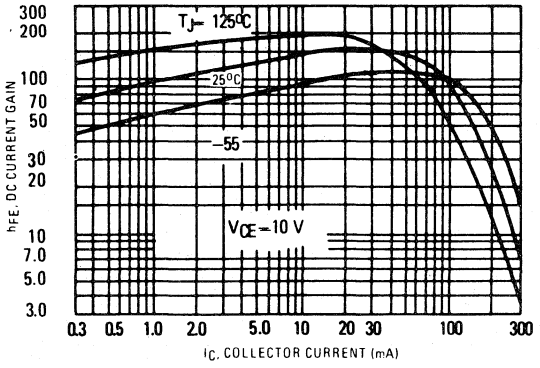


FIGURE 2 – DC CURRENT GAIN

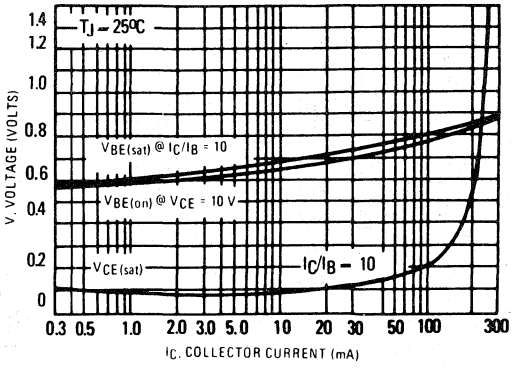


FIGURE 3 – "ON" VOLTAGES

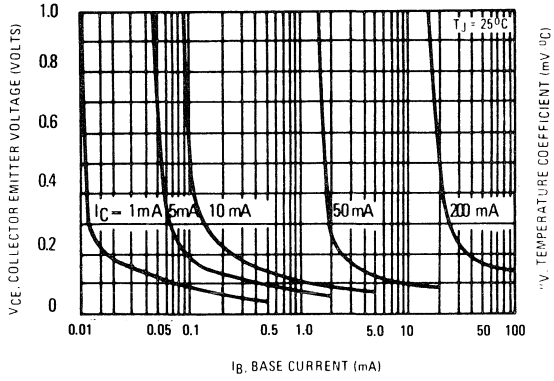


FIGURE 4 – COLLECTOR SATURATION REGION

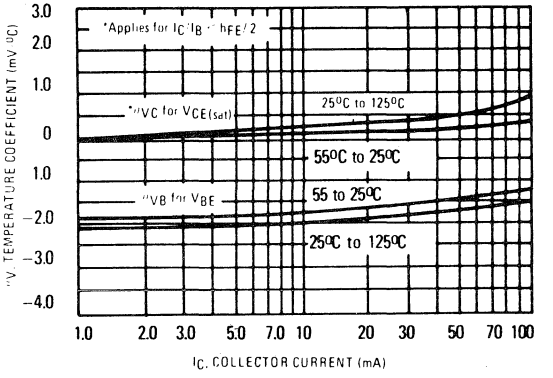


FIGURE 5 – TEMPERATURE COEFFICIENTS

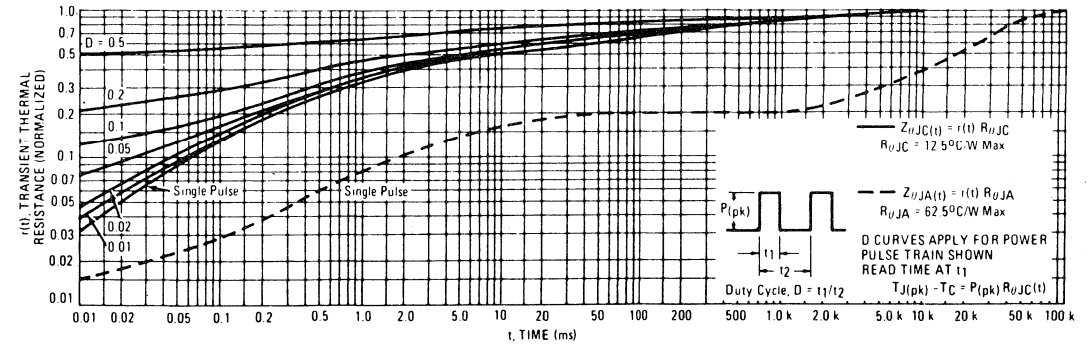


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

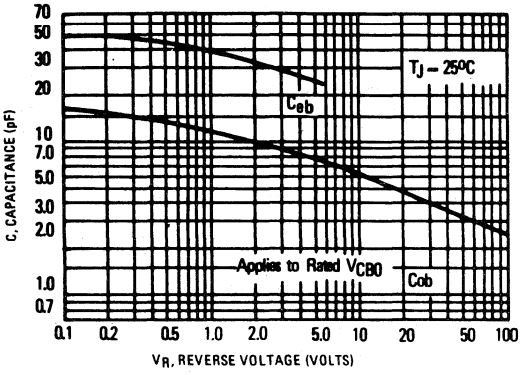


FIGURE 7 – CAPACITANCE

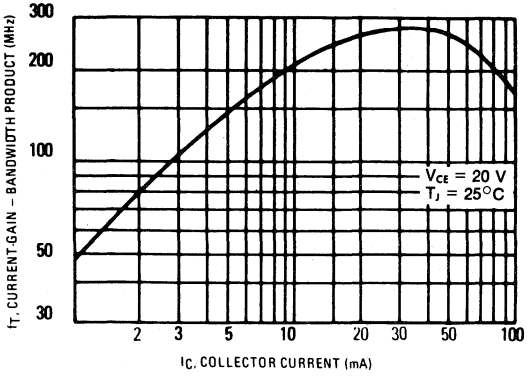


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

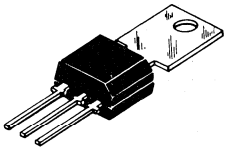
BF666
BF667 • BF668

NPN SILICON ANNULAR◆ HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal driver applications in television receivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 250 Vdc (Min) @ I_C = 1.0 mAdc — BF668
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1 Vdc (Max) @ I_C = 200 mAdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

NPN SILICON AMPLIFIER TRANSISTORS

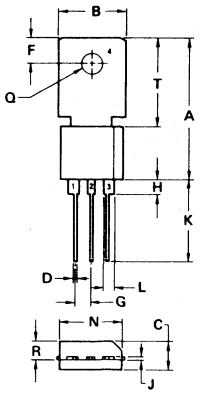


MAXIMUM RATINGS

Rating	Symbol	BF666	BF667	BF668	Unit
*Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
*Collector-Base Voltage	V_{CBO}	200	250	300	Vdc
*Emitter-Base Voltage	V_{EBO}	← 5 →			Vdc
*Collector Current — Continuous Peak	I_C	← 1 → ← 2 →			Adc
*Base Current	I_B	← →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 2:
PIN 1 EMITTER
2 COLLECTOR
3 BASE
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

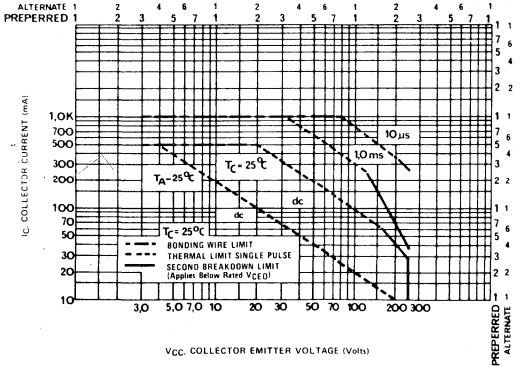
CASE 306-02

◆Annular Semiconductors Patented by Motorola Inc.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF666	BV_{CEO}	150	–	Vdc
	BF667		200	–	
	BF668		250	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF666	BV_{CBO}	200	–	Vdc
	BF667		250	–	
	BF668		300	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF666		–	0.1	
(V_{CB} = 200 Vdc, I_E = 0)	BF667		–	0.1	
(V_{CB} = 250 Vdc, I_E = 0)	BF668		–	0.1	
Emitter Cutoff Current (V_{BE} = 4 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mA, V_{CE} = 10 Vdc)			40	–	
(I_C = 100 mA, V_{CE} = 10 Vdc)			40		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–		Vdc
(I_C = 200 mAdc, I_B = 20 mAdc)			–	1	
Base-Emitter On Voltage (I_C = 200 mA, V_{CE} = 1 Vdc) c)		$V_{BE(on)}$	–	1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mA, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	100		MHz
Collector Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)		C_{ib}	–	110	pF

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

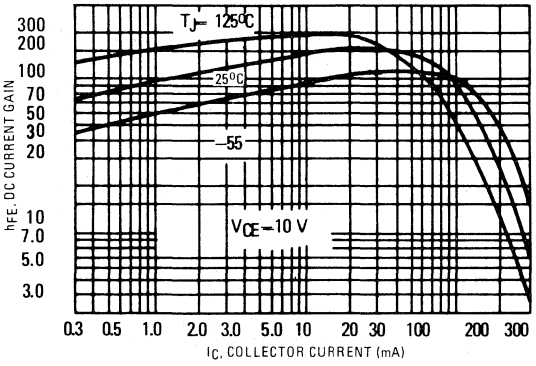


FIGURE 2 – DC CURRENT GAIN

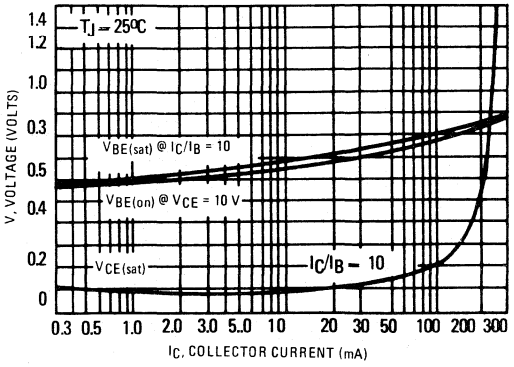


FIGURE 3 – "ON" VOLTAGES

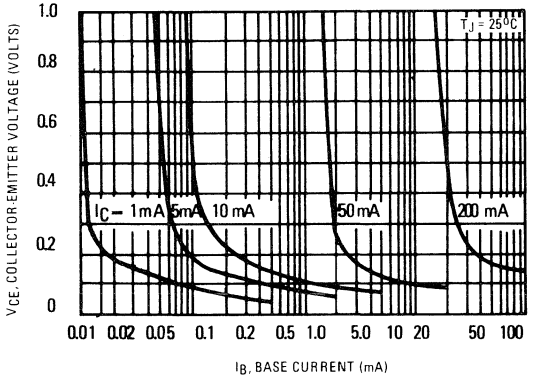


FIGURE 4 – COLLECTOR SATURATION REGION

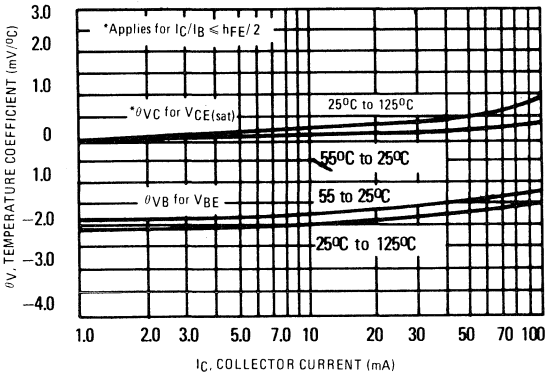


FIGURE 5 – TEMPERATURE COEFFICIENTS

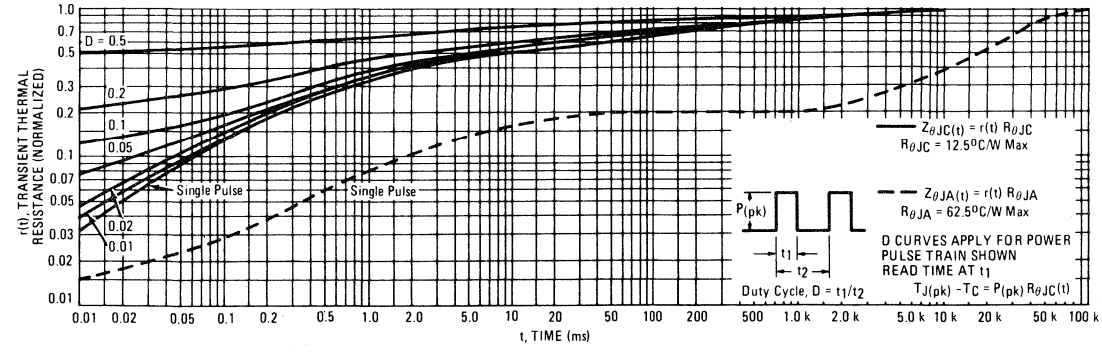


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

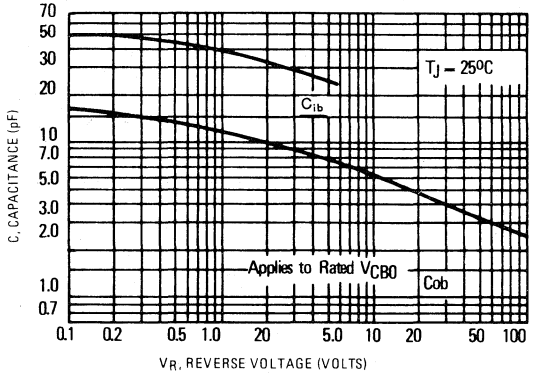


FIGURE 7 – CAPACITANCE

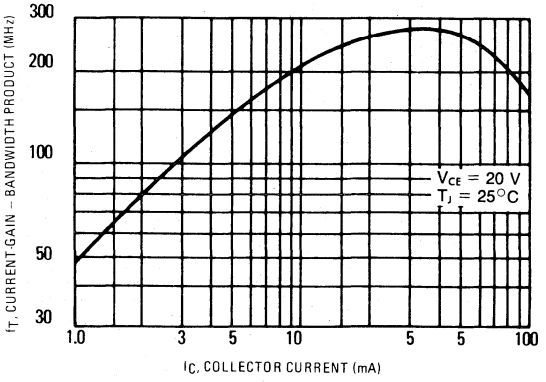


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

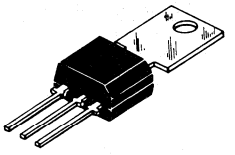
BF757
BF758 • BF759

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc — BF759
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance — C_{r_e} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package — 2 Watts Free Air Dissipation @ T_A = 25°C
- Complements to NPN BF760/BF761/BF762

NPN SILICON AMPLIFIER TRANSISTORS



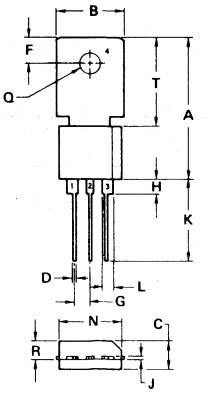
MAXIMUM RATINGS

Rating	Symbol	BF757	BF758	BF759	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	6.0			Vdc
*Collector Current — Continuous Peak	I_C	0.5 0.7			Adc
*Base Current	I_B	250			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	—	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	—	0.500	—
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

♦Annular Semiconductors Patented by Motorola Inc.

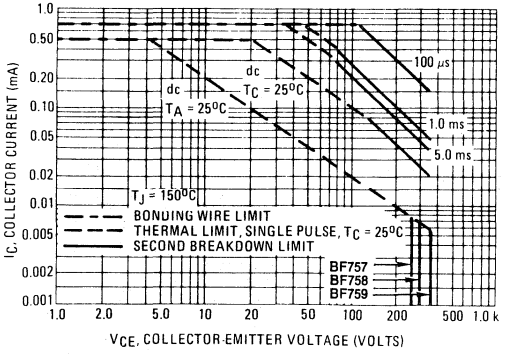
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF757	BV_{CEO}	250	–	Vdc
	BF758		300	–	
	BF759		350	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF757	BV_{CBO}	250	–	Vdc
	BF758		300	–	
	BF759		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF757		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF758		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF759		–	0.2	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.6	
(I_C = 50 mAdc, I_B = 5 mAdc)			–	1.5	
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	45	200	MHz
Common Emitter Reverse Transfer Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		Cre	–	3.0	pF

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

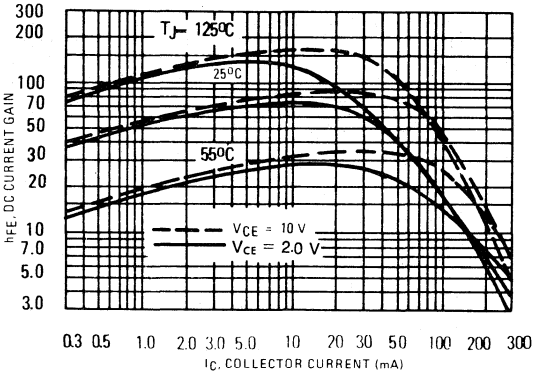


FIGURE 2 – DC CURRENT GAIN

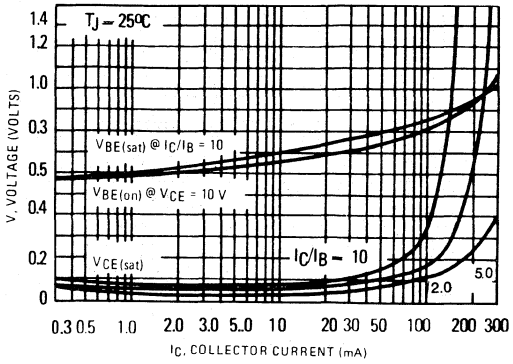


FIGURE 3 – "ON" VOLTAGES

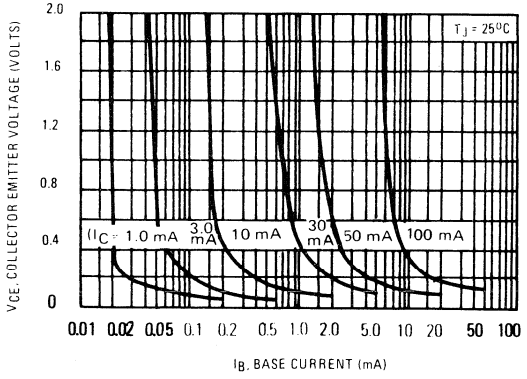


FIGURE 4 – COLLECTOR SATURATION REGION

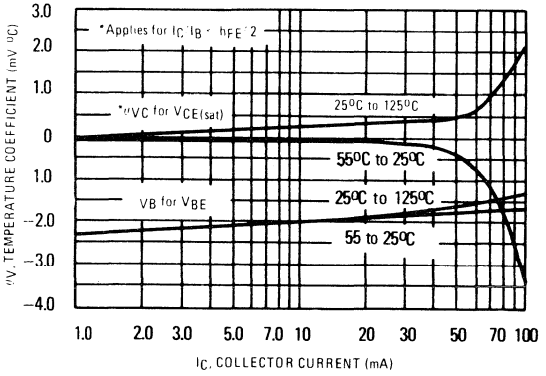


FIGURE 5 – TEMPERATURE COEFFICIENTS

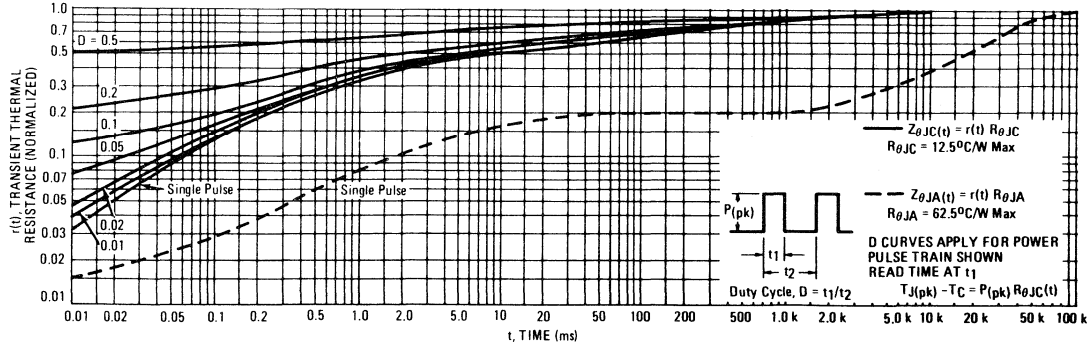


FIGURE 6 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

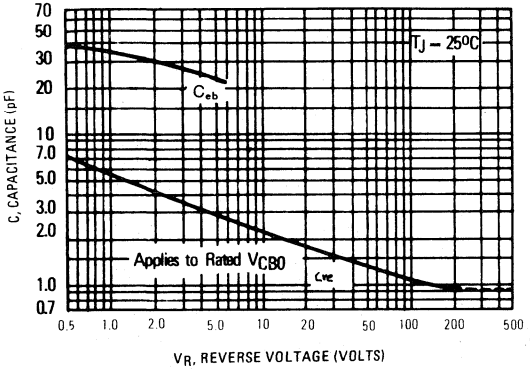


FIGURE 7 – CAPACITANCE

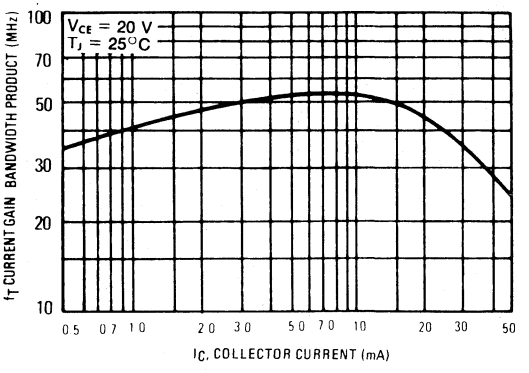


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT

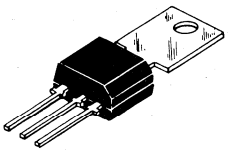
BF760
BF761 • BF762

PNP SILICON ANNULAR♦ HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – BF762
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75V (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance –
  C_{re} = 3.0 pF (Max) @ V_{CB} = 60 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C
- Complementary to NPN BF757/BF758/BF759

PNP SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

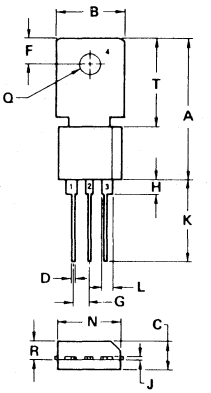
Rating	Symbol	BF760	BF761	BF762	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	← 5 →			Vdc
*Collector Current – Continuous Peak	I_C	← 0.5 → ← 0.7 →			Adc
*Base Current	I_B	← 250 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.

♦Annular Semiconductors Patented by Motorola Inc.



STYLE 2:
PIN 1 EMITTER
2 COLLECTOR
3 BASE
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-02

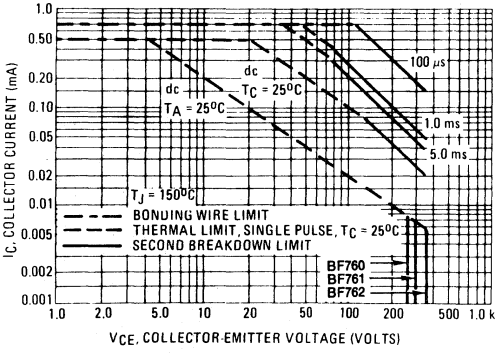
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF760	BV_{CEO}	250	–	Vdc
	BF761		300	–	
	BF762		350	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BF760	BV_{CBO}	250	–	Vdc
	BF761		300	–	
	BF762		350	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	BF760		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	BF761		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	BF762		–	0.2	
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)		$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	20	200	MHz
Common Emitter Reverse Transfer Capacitance (V_{CB} = 60 Vdc, I_E = 0, f = 1.0 MHz)		Cre	–	3	pF

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA

TYPICAL CHARACTERISTICS (continued)

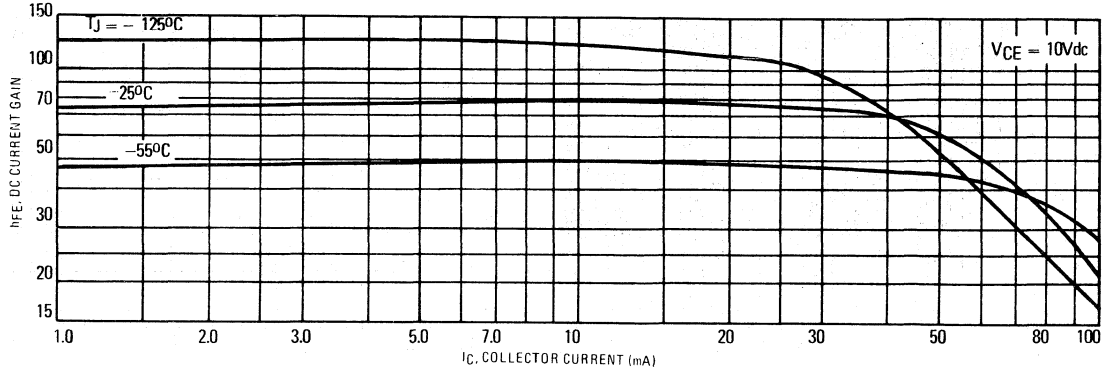


FIGURE 2 – DC CURRENT GAIN

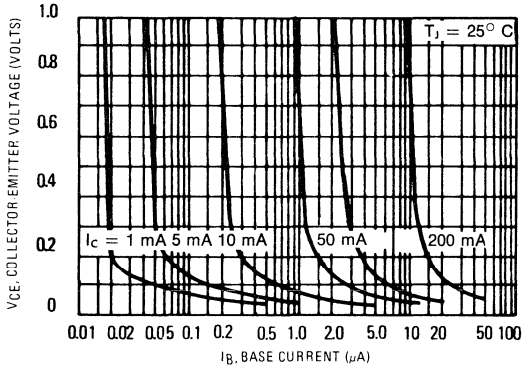


FIGURE 3 – COLLECTOR SATURATION REGION

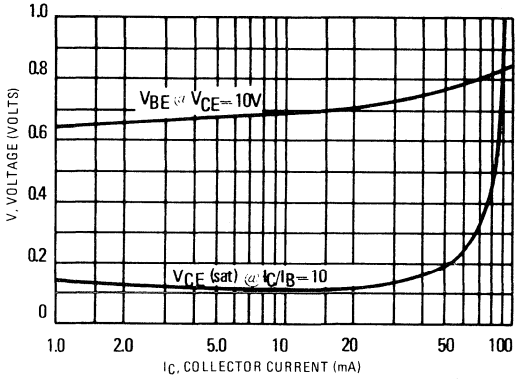


FIGURE 4 – "ON" VOLTAGES

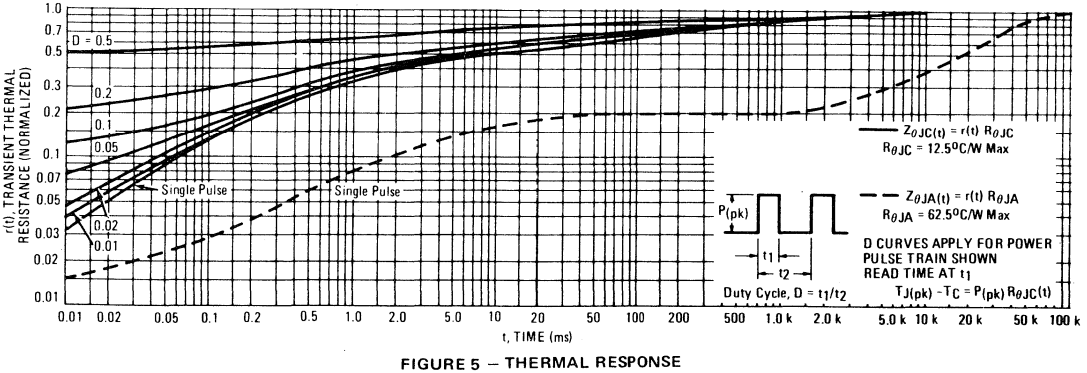


FIGURE 5 – THERMAL RESPONSE

TYPICAL CHARACTERISTICS (continued)

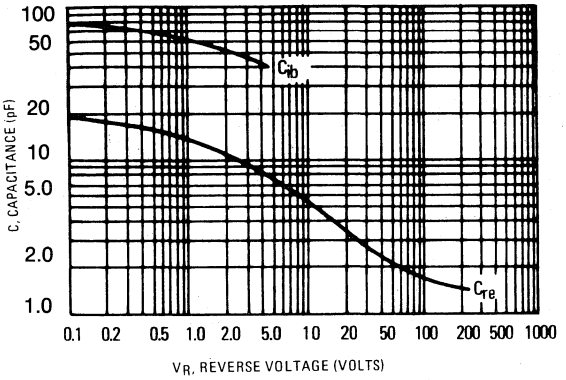


FIGURE 6 – CAPACITANCE

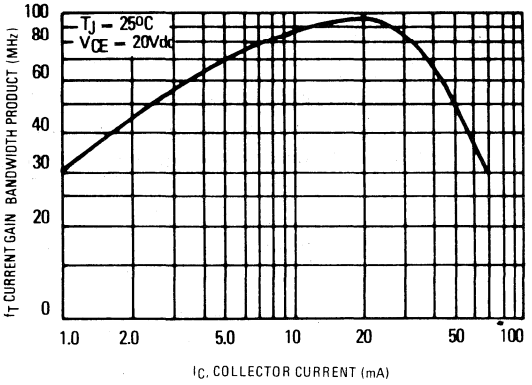


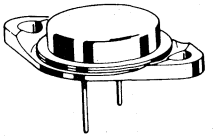
FIGURE 7 – CURRENT-GAIN – BANDWIDTH PRODUCT

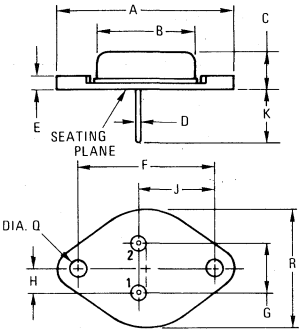
HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . Designed for use in horizontal deflection stages of black and white television receivers with 110° tubes.

- Collector-Emitter Voltage V_{CEX} = 400 V (V_{BE} = −5 V)
- Collector Current I_C = 7 A
- Gain H_{FE} = 10 to 50 at I_C = 5 A
- Fast Switching Fall Time: 1 μs max.

7 AMPERE
POWER TRANSISTOR
NPN SILICON





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

MAXIMUM RATINGS

Rating	Symbol	BU104	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	150	Vdc
Collector-Emitter Voltage (V_{BE} −5 V)	V_{CEX}	400	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	7 15	Adc
Base Current — Continuous	I_B	3	Adc
Total Power Dissipation Derate above 25 °C	P_D	85 0.5	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta$ JC	2	°C/W

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-03

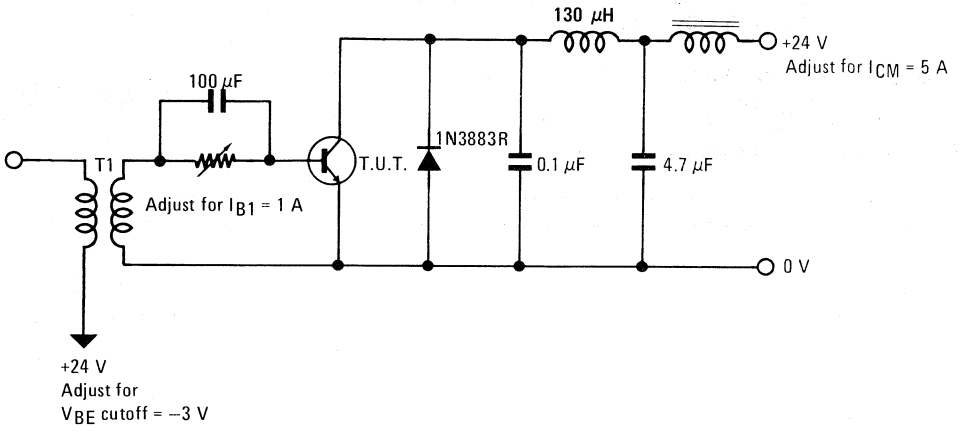
[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤10%.

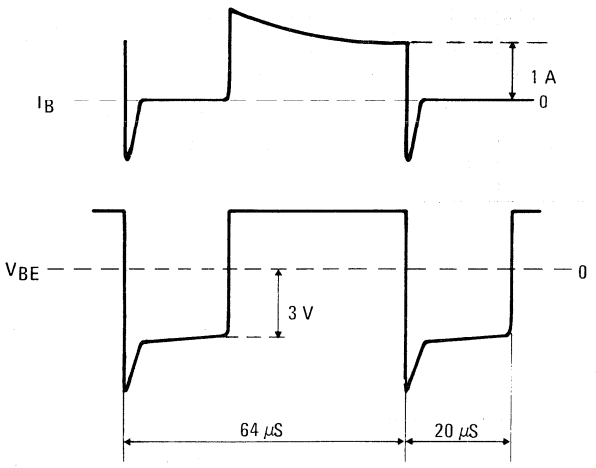
ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage[1] (I_C = 50 mA I_B = 0)	$V_{CEO\ (sus)}$	150			Vdc
Collector Base Leakage Current (V_{CB} = 250 V, I_E = 0)	I_{CBO}			0.5	mAdc
Collector Cutoff Current (V_{CE} = 400 V, I_{BE} = −5 V)	I_{CEX}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 10 V, I_C = 0)	I_{EBO}			10	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased (V_{CE} = 42.5 V)	$I_{S/b}$	2			Adc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 5 A, V_{CE} = 1.75 V)	h_{FE}	10		50	–
Collector-Emitter Saturation Voltage (I_C = 7 A, I_B = 1 A)	$V_{CE\ (sat)}$			2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 7 A, I_B = 1 A)	$V_{BE\ (sat)}$			2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T		10		MHz
SWITCHING CHARACTERISTICS **See Test Circuit**					
Fall Time (I_C = 5 A, I_{B1} = 1 A, $V_{BE\ (off)}$ = −3 V)	t_f			1	μs

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

FALL TIME TEST CIRCUIT





T1 Primary resistance = **4 Ohms**
Secondary resistance = **75 mOhms**
Leakage inductance = 0.8 μH
Turns ratio = 7.7/1

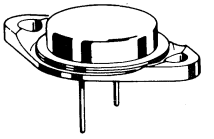
BU109

HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . Designed for use in horizontal deflection stages of black and white television receivers with 110° tubes.

- Collector-Emitter Voltage V_{CEX} = 330 V (V_{BE} = −5 V)
- Collector Current I_C = 10 A
- Gain H_{FE} = 15 min. at I_C = 5 A
- Fast Switching Fall Time: 1 μs max.

10 AMPERE
POWER TRANSISTOR
NPN SILICON



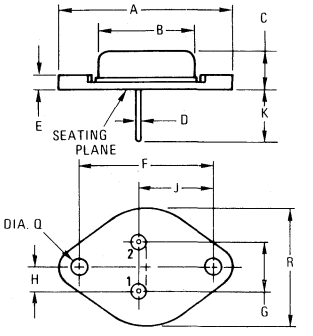
MAXIMUM RATING

Rating	Symbol	BU109	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	120	Vdc
Collector-Emitter Voltage (V_{BE} −5 V)	V_{CEX}	330	Vdc
Collector-Base Voltage	V_{CBO}	330	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous — Peak[1]	I_C I_{CM}	10 15	Adc
Base Current — Continuous	I_B	3	Adc
Total Power Dissipation Derate above 25 °C	P_D	85 0.5	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	2	°C/W

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

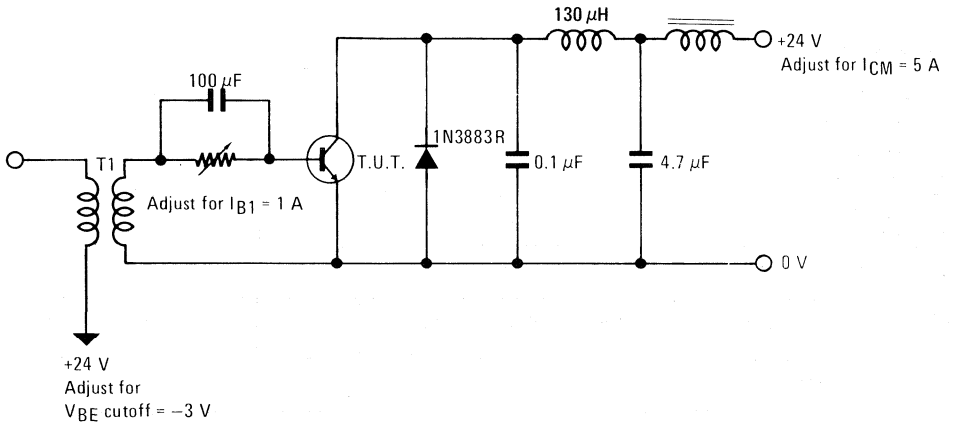
Collector connected to case
CASE 11-03

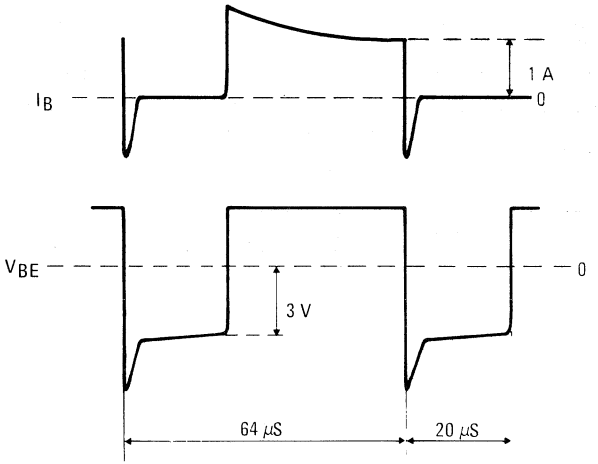
ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]					
Collector-Emitter Sustaining Voltage[1] (I_C = 50 mA I_B = 0)	$V_{CEO\ (sus)}$	120			Vdc
Collector Base Leakage Current (V_{CB} = 250 V I_E = 0)	I_{CBO}			0.5	mAdc
Collector Cutoff Current (V_{CE} = 330 V V_{BE} = −5 V)	I_{CEX}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 10 V I_C = 0)	I_{EBO}			10	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased (V_{CE} = 42.5 V)	$I_{S/b}$	2			Adc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 5 A V_{CE} = 1.5 V) (I_C = 7 A V_{CE} = 4 V)	h_{FE}	15	20		—
Collector-Emitter Saturation Voltage (I_C = 7 A I_B = 1 A)	$V_{CE\ (sat)}$			2	Vdc
Base-Emitter Saturation Voltage (I_C = 7 A I_B = 1 A)	$V_{BE\ (sat)}$			2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 500 mAdc V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T		10		MHz
SWITCHING CHARACTERISTICS					
SEE TEST CIRCUIT					
Fall Time (I_C = 5 A I_{BI} = 1 A $V_{BE\ (off)}$ = −3 V)	t_f			1	μs

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FALL TIME TEST CIRCUIT





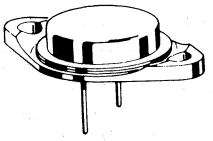
T1 Primary resistance = **4 Ohms**
Secondary resistance = **75 mOhms**
Leakage inductance = 0.8 μH
Turns ratio = 7.7/1

HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . Designed for use in horizontal deflection stages of black and white television receivers.

- Collector-Emitter Voltage V_{CEV} = 330 V (V_{BE} = −3.5 V)
- Collector-Current I_C = 10 A
- Collector-Emitter Saturation Voltage 1.5 V max. at I_C = 7 A
- Fast Switching Fall Time 1 μs max.

10 AMPERE
POWER TRANSISTOR
NPN SILICON



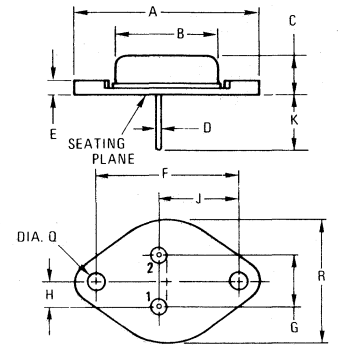
MAXIMUM RATINGS

Rating	Symbol	BU110	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	150	Vdc
Collector-Emitter Voltage (V_{BE} = 3.5 V)	V_{CEV}	330	Vdc
Collector-Base Voltage	V_{CBO}	330	Vdc
Emitter-Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous — Peak[1]	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak[1]	I_B I_{BM}	2 3	Adc
Total Power Dissipation Derate above 25 °C	P_D	90 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.66	°C/W

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case

CASE 11-03

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO\ (sus)}$	150		Vdc
Collector-Base Leakage Current (V_{CB} = 250 V, I_E = 0)			0.5	mAdc
Collector-Cutoff Current (V_{CE} = 330 V, V_{BE} = −3.5 V)	I_{CEX}		1.0	mAdc
Collector-Cutoff Current (V_{CE} = 330 V, V_{BE} = OT$_C$ = 150 °C)	I_{CES}		15	mAdc
Emitter-Cutoff Current (V_{EB} = 6 V)	I_{EBO}		10	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 18 V, t = 1 sec.)	$I_{S/b}$	5		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 7 A, V_{CE} = 1.5 V)	h_{FE}	5		–
Collector-Emitter Saturation Voltage (I_C = 7 A, I_B = 1.4 A)	$V_{CE\ (sat)}$		1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 7 A, I_B = 1.4 A)	$V_{BE\ (sat)}$		1.7	Vdc
SWITCHING CHARACTERISTICS				
Resistive Load (Table 1)				
Fall Time (I_C = 6 A, I_{B1} = I_{B2} = 1.2 A, V_{CE} = 60 V)	tf		1.0	μs

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

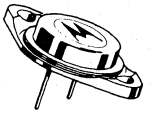
HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for use in the switched mode power supply of 90° and 110° colour television receivers.

- High collector-emitter voltage
  V_{CES} = 700V, 750V
- Collector current
  I_C = 4Adc
- Low Collector emitter saturation voltage
  $V_{CE(sat)}$ = 5Vdc, @ I_C = 4A, I_B = 1A
- Fall time @ I_C = 2,5A, $I_{B\ (end)}$ = 0,25A
  t_f = 0,15μsec (typ)

4 AMPERE
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON

700, 750 VOLTS
50 WATTS



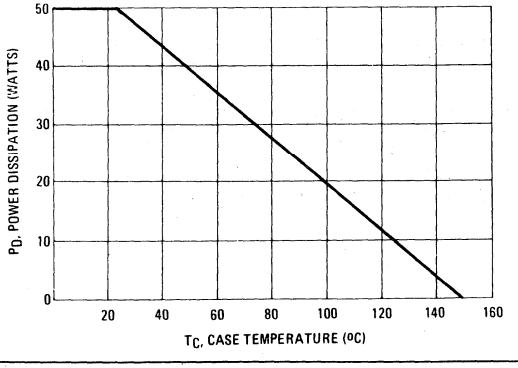
MAXIMUM RATINGS

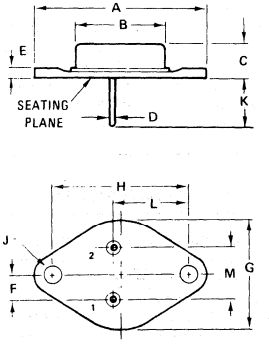
Rating	Symbol	BU126	BU126A	Unit
Collector-Emitter Voltage	V_{CEO}	300	250	Vdc
Collector-Emitter Voltage VBE=O	V_{CES}	750	700	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current —Continuous Peak	I_C	4.0 6.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Junction Temperature	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θJC	2.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	1.550	–	39.370
B	–	0.830	–	21.080
C	0.250	0.300	6.350	7.620
D	0.039	0.043	0.991	1.090
E	–	0.135	–	3.430
F	0.205	0.225	5.210	5.720
G	–	1.050	–	26.670
H	1.177	1.197	29.900	30.400
J	0.151	0.161	3.840	4.090
K	0.440	0.480	11.180	12.190
L	0.655	0.675	16.640	17.150
M	0.420	0.440	10.670	11.180

All JEDEC dimensions and notes apply

CASE 11
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage I_C = 100 mA, L = 25 MH, BU126 See Fig. 6 BU126A	V_{CEO}	 300 250			Vdc
Collector Cutoff Current V_{CES} = Rated Value, T_C = 25 °C V_{CES} = Rated Value, T_C = 125 °C	I_{CES}			 0.5 2.0	mAdc
Emitter Cutoff Current V_{BE} = 6 Vdc, I_C = 0	I_{EBO}			 5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain I_C = 1.0 Adc, V_{CE} = 5 Vdc	H_{FE}	 15		 60	
Collector Emitter Saturation Voltage I_C = 2.5 Adc, I_B = 0.25 Adc I_C = 4 Adc, I_B = 1 Adc	$V_{CE\ (sat)}$			 10 5	Vdc
Base Emitter Saturation Voltage I_C = 4 Adc, I_B = 1 Adc	$V_{BE\ (sat)}$			 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product I_C = 0.2 Adc, V_{CE} = 10 Vdc, F = 1 MHz	F_T		 8		MHz
Output Capacitance I_E = 0, V_{CB} = 10 Vdc, F = 1 MHz	C_{OB}		 85		pF
Input Capacitance I_C = 0, V_{EB} = 2 Vdc, F = 1 KHz	C_{IB}		 1400		pF
SWITCHING CHARACTERISTICS					
Storage Time I_C = 2.5 Adc, $I_{B(end)}$ = 0.25 Adc	t_s		 1.2		μs
Fall Time I_C = 2.5 Adc, $I_{B(end)}$ = 0.25 Adc	t_f		 0.15		μs

FIGURE 2 – DC CURRENT GAIN

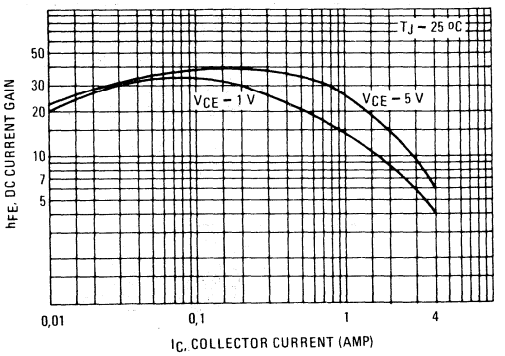


FIGURE 3 – COLLECTOR SATURATION REGION

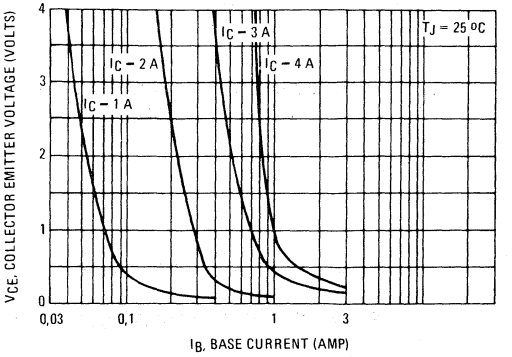


FIGURE 4 – "SATURATION" AND "ON" VOLTAGES

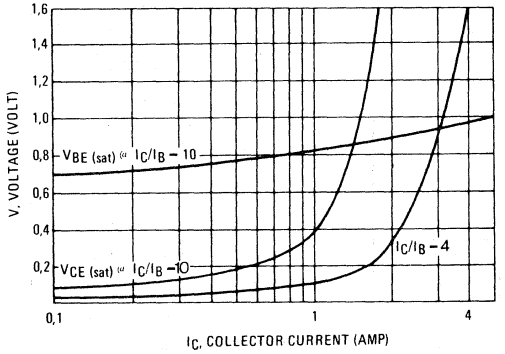


FIGURE 5 – FORWARD BIAS SAFE OPERATING AREA

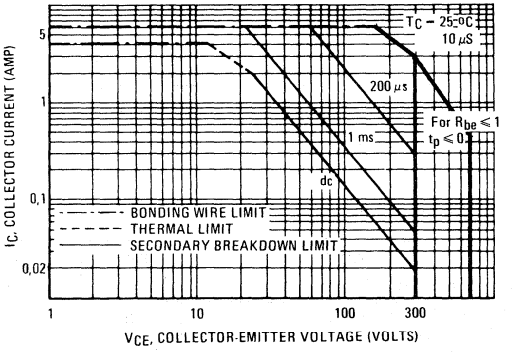
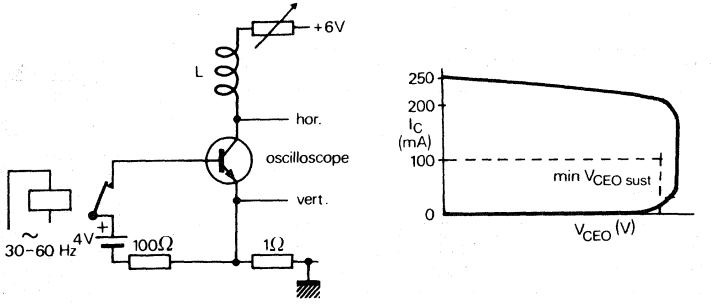


FIGURE 6 – SUSTAINING VOLTAGE TEST CIRCUIT



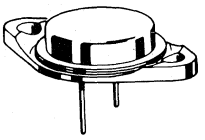
BU205

HORIZONTAL DEFLECTION SILICON TRANSISTORS

. . . designed for use in color television receivers.

- Collector-Emitter Voltage V_{CES} = 1500 Vdc
- Collector Current I_C = 2.5 A
- Fall Time @ I_C = 4.5 Adc, I_B = 1.8 A
  t_f = 0.75 μs (Typ) • t_f = 1.0 μs (Max.)

2.5 AMPERE
TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON
1500 VOLTS
36 WATTS

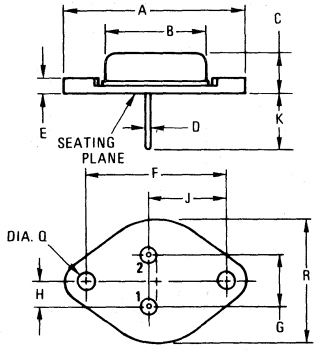


MAXIMUM RATINGS

Rating	Symbol	BU205	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage (V_{BE} = 0)	V_{CES}	1500	Vdc
Collector-Base Voltage	V_{CB}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.5 3.0	Adc
Base Current	I_B	2.5	Adc
Total Device Dissipation @ T_C = 25 °C Derate Above 25 °C	P_D	56 0.4	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta JC$	2.5	°C/W



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO\ (sus)}$	700			Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}			1.0	mAdc
Emitter-Base Voltage (I_C = 0, I_E = 10 mA)	V_{EBO}	5.0	7		Vdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}			10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 A, V_{CE} = 5 V)	H_{FE}	2			
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 1.0 Adc)	$V_{CE\ (sat)}$			5.0	Vdc
Base Emitter Saturation Voltage (I_C = 2 Adc, I_B = 1.0 Adc)	$V_{BE\ (sat)}$			1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased (t = 1.0 s, V_{CE} = 100 Vdc)	$I_{S/b}$	200			mAdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}		65		pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2 Adc, I_{B1} = 1 Adc, L_B = 25 μH)	t_f		0.75	1.0	μs

BU208 • BU208A

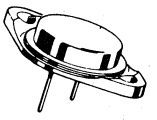
Full data in preparation. Available December 1977.

HORIZONTAL DEFLECTION SILICON TRANSISTORS

. . . designed for use in large screen color television receivers.

- Collector-Emitter Voltage V_{CES} = 1500 Vdc
- Collector Current I_C = 5.0 Adc
- Fall Time @ I_C = 4.5 Adc, I_B = 1.8 A
  t_f = 0.4 μS (Typ.) • t_f = 1.0 μS (Max.)
- Saturation voltage $V_{CE\ (sat)}$ 1 V (Max.)
  at I_C = 4.5 A (BU208 A)

5.0 AMPERE
TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON
1500 VOLTS
56 WATTS



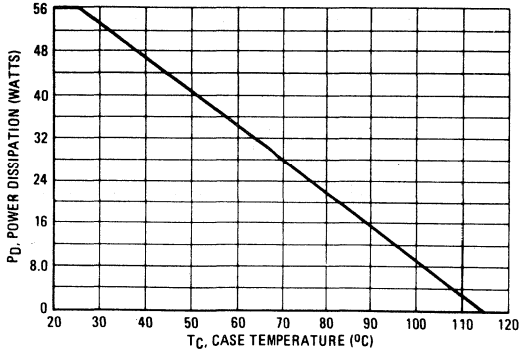
MAXIMUM RATINGS

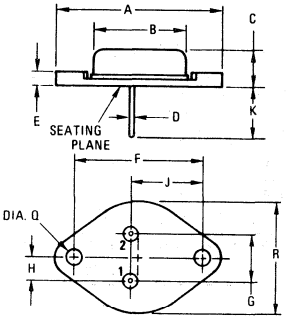
Rating	Symbol	BU208/BU208A	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage (V_{BE} = 0)	V_{CES}	1500	Vdc
Collector-Base Voltage	V_{CB}	1500	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous — Peak	I_C	5.0 10	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25 °C Derate Above 25 °C	P_D	56 0.625	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta JC$	2.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11 (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Collector-Emitter Voltage (I_C = 100 mA, L = 25 mH)	BU208 BU208A	$V_{CEO\ (sus)}$	700 700			Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	BU208 BU208A	I_{CES}			1.0 1.0	mAdc
Emitter-Base Voltage (I_C = 0, I_E = 100 mA)	BU208 BU208A	V_{EBO}	7.0 7.0	12 12		Vdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	BU208 BU208A	I_{EBO}			10 10	mAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 4.5 A, V_{CE} = 5 V)	BU208 BU208A	H_{FE}	2.25 2.25			
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	BU208 BU208A	$V_{CE\ (sat)}$			5.0 1.0	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2.0 Adc)	BU208 BU208A	$V_{BE\ (sat)}$			1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased (t = 1.0 s, V_{CE} = 100 Vdc)	BU208, BU208A	$I_{S/b}$	200			mAdc
DYNAMIC CHARACTERISTICS						
Current Gain — Bandwidth Product[2] (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	BU208 BU208A	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BU208 BU208A	C_{ob}		125		pF
SWITCHING CHARACTERISTICS						
Fall Time (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	BU208 BU208A	t_f		0.4	1.0	μs

[2] $f_T = |h_{fe}| \bullet f_{test}$

BU311
BU312

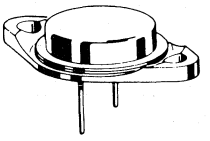
HIGH VOLTAGE NPN SILICON TRANSISTOR

. . . Designed for use in horizontal deflection stages of black and white television receivers.

- Collector-Emitter Voltage V_{CEV} = 200 V
- Collector-Current I_C = 6 A
- Gain H_{FE} = 15 min. at I_C = 5 A (BU311)
- Fast Switching Fall Time: 1 μs max.

6 AMPERE

POWER TRANSISTORS
NPN SILICON

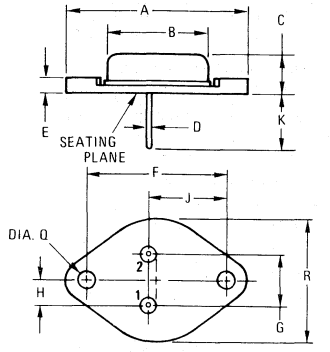


MAXIMUM RATINGS

Rating	Symbol	BU312	BU311	Unit
Collector-Emitter Voltage	$V_{CEO\ (sus)}$	150	125	Vdc
Collector-Emitter Voltage (V_{BE} = −3.5 V)	V_{CEX}	280	200	Vdc
Collector-Base Voltage	V_{CBO}	280	200	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	6		Adc
Base Current — Continuous	I_B	2		Adc
Total Power Dissipation Derate above 25 °C	P_D	50 0.33		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta JC$	3	°C/W



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67		1.050

Collector connected to case

CASE 11-03

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS[1]					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO\ (sus)}$			Vdc
(I_C = 10 mA, I_B = 0)	BU312		150		
	BU311		125		
Collector-Cutoff Current		I_{CEX}			mAdc
(BU312 V_{CE} = 280 V, V_{BE} = −3.5 V)				1	
(BU311 V_{CE} = 200 V, V_{BE} = −3.5 V)					
Collector Cutoff Current		I_{CES}			mAdc
(BU311 V_{CE} = 150 V, V_{BE} = 0, T_C = 150 °C)				15	
(BU312 V_{CE} = 210 V, V_{BE} = 0 T_C = 150 °C					
Emitter-Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6 V)	Both types			1	
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$			Adc
(V_{CE} 20 V, t = 1 sec.	Both types		2.5		
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			–
(I_C = 5 A, V_{CE} = 1.5 V)	BU312		10		
	BU311		15		
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$			Vdc
(I_C = 5 A, I_B = 0.5 A	BU312			1.5	
	BU311			1.0	
Base-Emitter Saturation Voltage		$V_{BE\ (sat)}$			Vdc
(I_C = 5 A, I_B = 0.5 A	BU312			1.5	
	BU311			1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Fall Time	Both types	t_f		1.0	μs
	(I_C = 4 A, I_{B1}/I_{B2} = 0.4 A, V_{CE} = 60 V)				

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

BU322 • BU322A

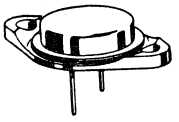
HIGH VOLTAGE SILICON POWER DARLINGTONS

Power Transistor mainly intended for use as ignition circuit output transistor.

* Specified minimum sustaining voltage:
  $V_{CER(sus)}$ – 350 V (BU322) I_C – 3 A
  425 V (BU322A)
* High S.O.A. capability:
  V_{CE} – 325 V (BU322) at I_C – 7 A
  400 V (BU322A)
* Low $V_{CE(sat)}$ – 1.7 V max. at I_C – 4 A

DARLINGTON
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON

7 AMPERE
400, 475 VOLTS
100 WATTS



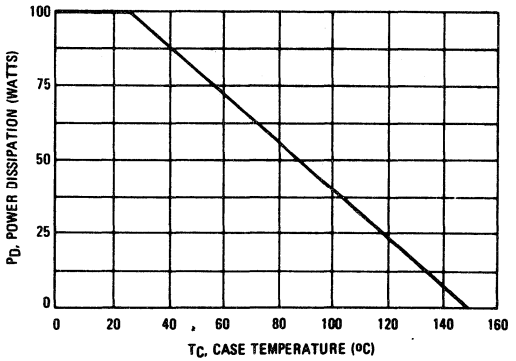
MAXIMUM RATINGS

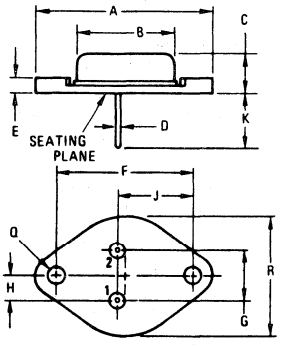
Rating	Symbol	BU322	BU322A	Unit
Collector-Emitter Voltage (R_{BE} = 100Ω)	V_{CER}	400	475	Vdc
Collector-Base Voltage	V_{CB0}	450	525	Vdc
Emitter-Base Voltage	V_{EB0}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	7.0 12.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	100 0.8		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

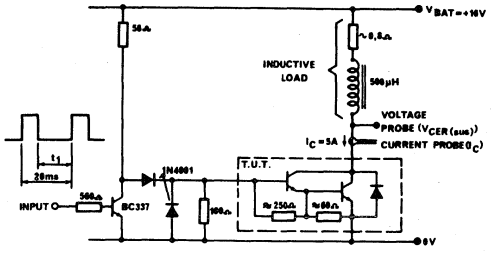
Collector connected to case.
CASE 11-01
TO–3

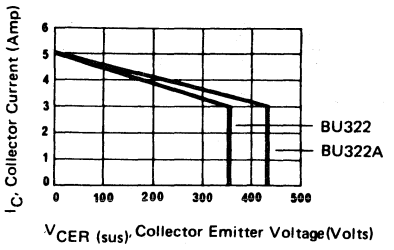
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (See Figure 2) (I_C = 3.0 A)	(BU322) (BU322A)	$V_{CER(sus)}$	350 425			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100Ω)		I_{CER}			1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)		I_{CBO}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}			30	mAdc
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 80 mAdc) (I_C = 7.0 Adc, I_B = 240 mAdc)		$V_{CE(sat)}$			 1.7 2.7	Vdc
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 80 mAdc) (I_C = 7.0 Adc, I_B = 240 mAdc)		$V_{BE(sat)}$			 2.5 3.0	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (1) (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}		150		pF

(1) $f_T = h_{fe} \cdot f_{test}$

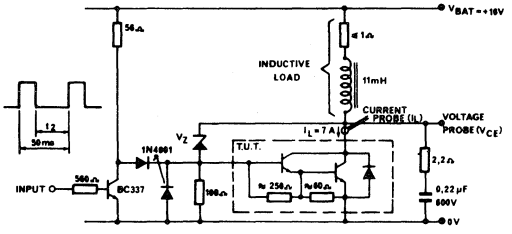
FIGURE 2 – SUSTAINING VOLTAGE TEST $V_{CER\ (sus)}$





t_1 to be selected that I_C reaches 5 Adc before switch-off
Case temperature of the power transistor: T_C = 25°C

Test conditions of the Collector-Base Clamping Circuit :



Clamping device characteristics:

V_Z = 325 V (BU322) / 400 V (BU322A) ±1% at I_Z = 20 mA

Clamping duration is around 235 μsec (BU322) / 195 μsec (BU322A)

t_2 to be selected that I_L reaches 7 Adc before switch-off

Case temperature of the power transistor: T_C = 25°C.

FIGURE 3 – S.O.A. TEST

Data sheet with improved spec. available December 1977.

BU323 • BU323A

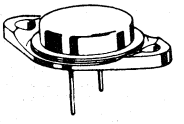
HIGH VOLTAGE SILICON POWER DARLINGTONS

Power Transistor mainly intended for use as ignition circuit output transistor.

* Specified minimum sustaining voltage:
  $V_{CER(sus)}$ – 350 V (BU323) I_C – 3 A
  425 V (BU323A)
* High S.O.A. capability:
  V_{CE} – 325 V (BU323) at I_C – 10 A
  400 V (BU323A)
* Low $V_{CE(sat)}$ – 1.7 V max. at I_C – 7 A

DARLINGTON TRIPLE DIFFUSED POWER TRANSISTORS NPN SILICON

10 AMPERE
400, 475 VOLTS
125 WATTS



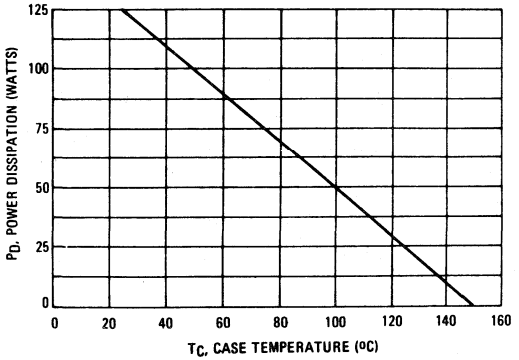
MAXIMUM RATINGS

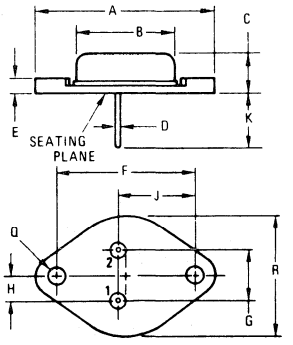
Rating	Symbol	BU323	BU323A	Unit
Collector-Emitter Voltage (R_{BE} =100Ω)	V_{CER}	400	475	Vdc
Collector-Base Voltage	V_{CBO}	450	525	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	10.0 16.0		Adc
Base Current	I_B	3.0		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	125 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

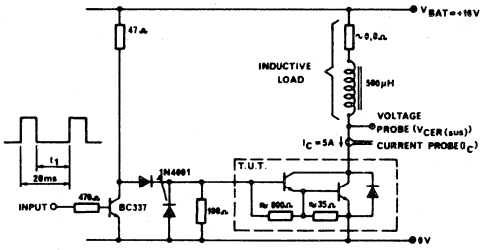
Collector connected to case.
CASE 11-01
TO–3

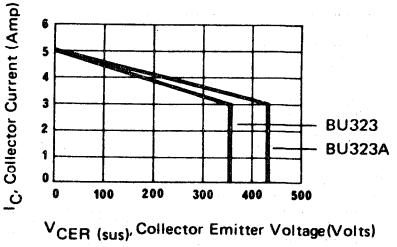
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (See Figure 2) (I_C = 3.0 A)	(BU323) (BU323A)	$V_{CER\ (sus)}$	350 425			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100Ω)		I_{CER}			1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)		I_{CBO}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}			30	mAdc
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc)		$V_{CE(sat)}$			1.7 2.7	Vdc
Base-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc)		$V_{BE(sat)}$			2.5 3.0	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (1) (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}		150		pF

(1) $f_T = h_{fe} \cdot f_{test}$

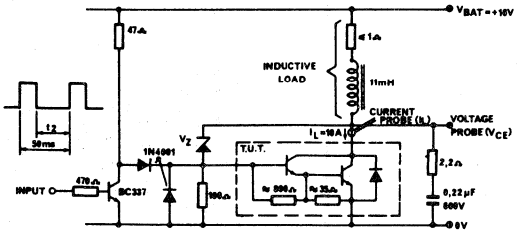
FIGURE 2 – SUSTAINING VOLTAGE TEST $V_{CER\ (sus)}$





t_1 to be selected that I_C reaches 5 Adc before switch-off
Case temperature of the power transistor: T_C = 25°C

Test conditions of the Collector-Base Clamping Circuit:



Clamping device characteristics:

V_Z = 325 V (BU323) / 400 V (BU323A) ±10% at I_Z = 20 mA

Clamping duration is around 340 μsec (BU323) / 275 μsec (BU323A)

t_2 to be selected that I_L reaches 10Adc before switch-off

Case temperature of the power transistor: T_C = 25°C.

FIGURE 3 – S.O.A. TEST

ADVANCE INFORMATION

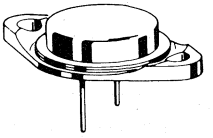
HIGH VOLTAGE NPN SILICON TRANSISTOR

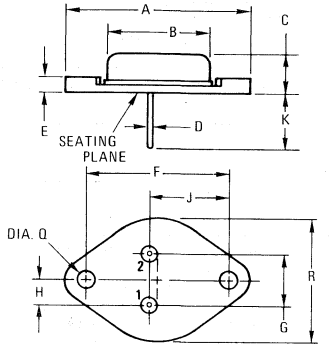
. . . Designed for use in the switch-mode power supplies of colour television receivers.

- Collector-Emitter Voltage V_{CES} = 800 V and 900 V
- Collector-Current I_C = 6 A DC
- Low collector emitter saturation voltage
  $V_{CE\ (sat)}$ = 3 V max. at I_C = 4 A
- Fall time at I_C = 2.5 A
  T_F = 1 μs max. at T_C = 100 °C

6 AMPERE

POWER TRANSISTORS
NPN SILICON





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-03

MAXIMUM RATINGS

Rating	Symbol	BU326	BU326A	Unit
Collector-Emitter Voltage	$V_{CEO\ (sus)}$	375	400	Vdc
Collector-Emitter Voltage	V_{CES}	800	900	Vdc
Emitter Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous – Peak[1]	I_C I_{CM}	6 8		Adc
Base Current – Continuous – Peak[1]	I_B I_{BM}	2 3		Adc
Reverse Base Current 20 ms max. – Peak during turn off	I_E I_{EM}	100 mA 3		mA A
Total Power Dissipation Derate above 25 °C	P_D	75 0.6		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.65	°C/W

[1] Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0, L= 25 mH)	BU326	$V_{CEO\ (sus)}$	375			Vdc
	BU326A		400			
Collector-Cutoff Current (V_{CE} = 800 V, V_{BE} = 0)	BU326	I_{CES}			1.0	mAdc
(V_{CE} = 900 V, V_{BE} = 0)	BU326A				1.0	
Collector Cutoff Current (V_{CE} = 800 V, V_{BE} = 0, T_J = 125 °C)	BU326	I_{CES}			2.0	mAdc
(V_{CE} = 900 V, V_{BE} = 0, T_J = 125 °C)	BU326A				2.0	
Emitter Cutoff Current (V_{EB} = 10 V, I_C = 0)		I_{EBO}			10	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased (V_{CE} 30 V, t = 1 sec.)		$I_{S/b}$			2.5	Adc
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = 0.6 A, V_{CE} = 5 V)		h_{FE}		30		–
Collector-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A)		$V_{CE\ (sat)}$			10	Vdc
(I_C = 4.0 A, I_B = 1.25 A)					3	
Base-Emitter Saturation Voltage (I_C = 2.5 A, I_B = 0.25 A)		$V_{BE\ (sat)}$			1.4	Vdc
(I_C = 4.0 A, I_B = 1.25 A)					1.6	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T		6		MHz
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Turn On Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V)	t_{on}			0.5	μs
Storage Time		t_s			3.5	μs
Fall Time		t_f		0.3		μs
Fall Time	(I_C = 2.5 A, I_{B1} = 0.5 A) (I_{B2} = 1.0 A, V_{CC} = 250 V, T_C = 100 °C)	t_f			1.0	μs

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

MJ900 • MJ901 (PNP)
MJ1000 • MJ1001 (NPN)

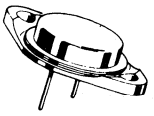
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

8.0 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-80 VOLTS
90 WATTS



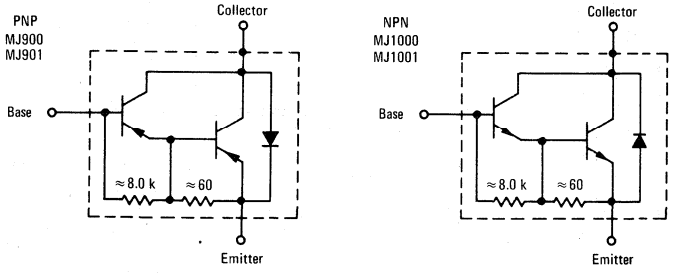
MAXIMUM RATINGS

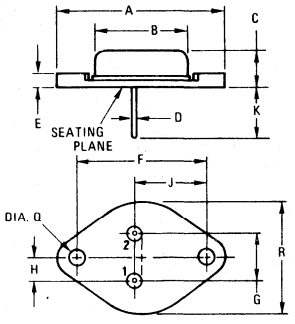
Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.94	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11 (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ900, MJ1000	BV_{CEO}	60	–	Vdc
	MJ901, MJ1001		80	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ900, MJ1000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ901, MJ1001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ900, MJ1000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ901, MJ1001		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ900, MJ1000		–	500	
(V_{CE} = 40 Vdc, I_B = 0)	MJ901, MJ1001		–	500	
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 40 mAdc)			–	4.0	
Base-Emitter Voltage(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	2.5	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

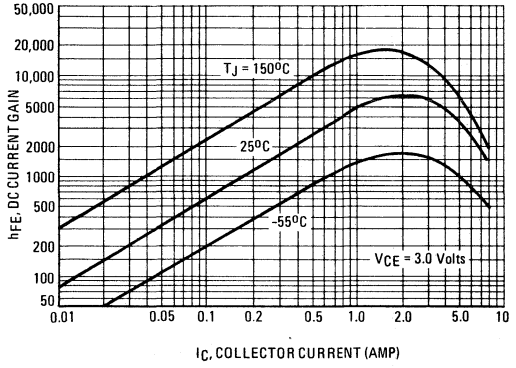


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

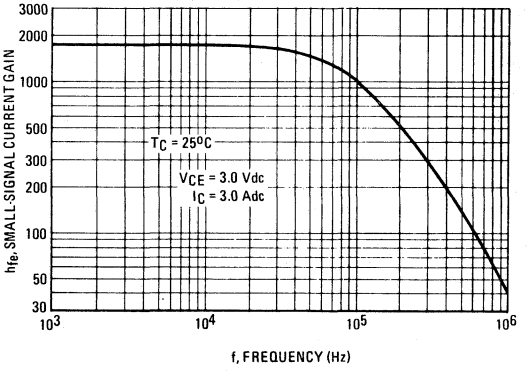


FIGURE 4 – "ON" VOLTAGES

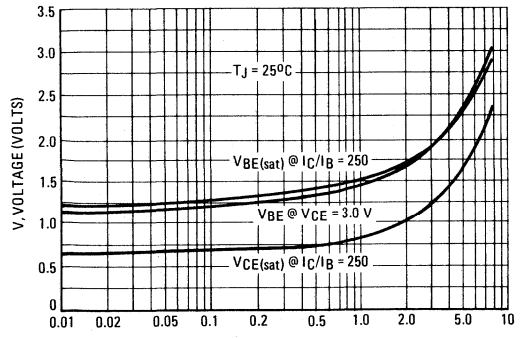
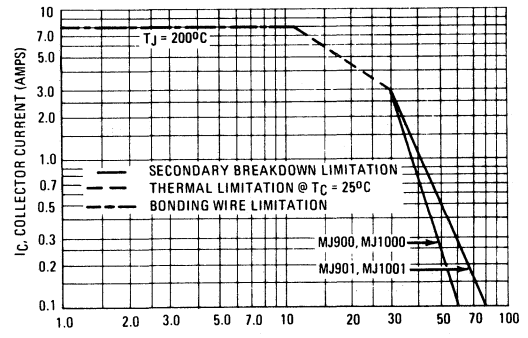


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

MJ2500 • MJ2501 (PNP)
MJ3000 • MJ3001 (NPN)

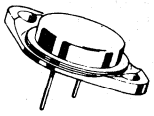
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

10 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-80 VOLTS
150 WATTS



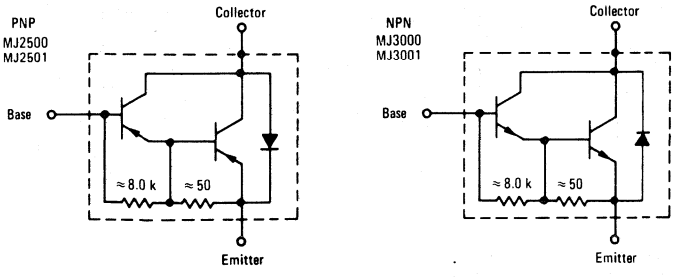
MAXIMUM RATINGS

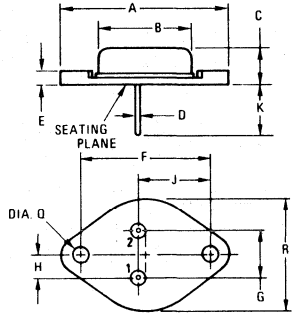
Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	150		Watts
Derate above 25^oC		0.857		$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^oC/W$

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67	–	1.050

Collector connected to case

CASE 11 (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000	BV_{CEO}	60	–	Vdc
	MJ2501, MJ3001		80	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ2500, MJ3000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ2501, MJ3001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2500, MJ3000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2501, MJ3001		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ2500, MJ3000		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ2501, MJ3001		–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 2 – DC CURRENT GAIN

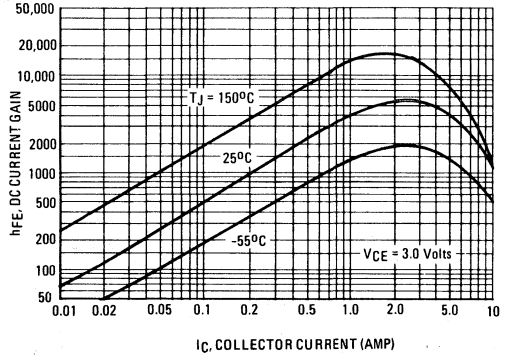


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

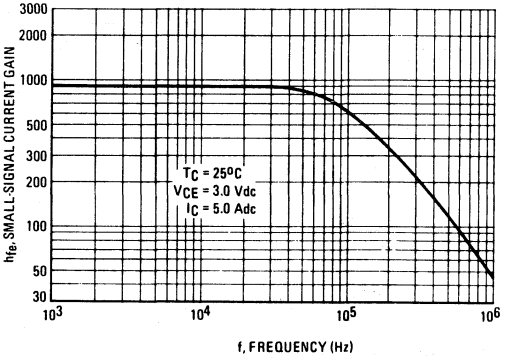


FIGURE 4 – "ON" VOLTAGES

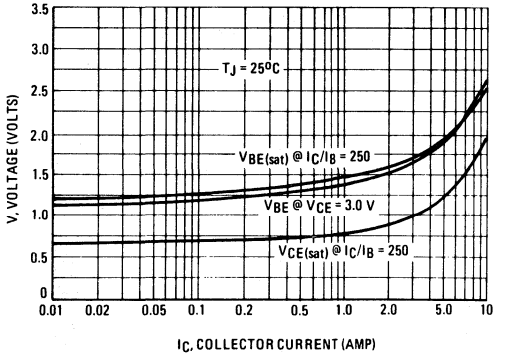
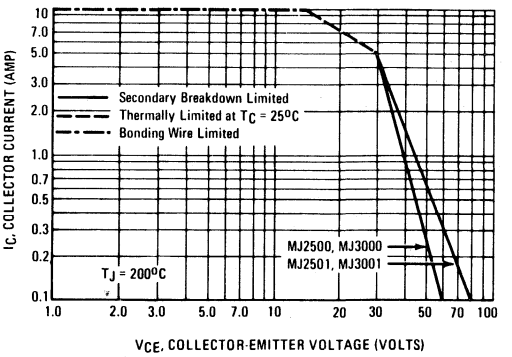


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

PNP SILICON POWER TRANSISTOR

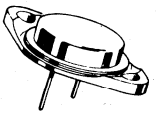
. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain –
  h_{FE} = 20-70 @ I_C = 4.0 Adc
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4.0 Adc
- Excellent Safe Operating Area
- Complement to Motorola's "Epi-Base" Transistor, 2N3055

15 AMPERE POWER TRANSISTOR

PNP SILICON

60 VOLTS
150 WATTS



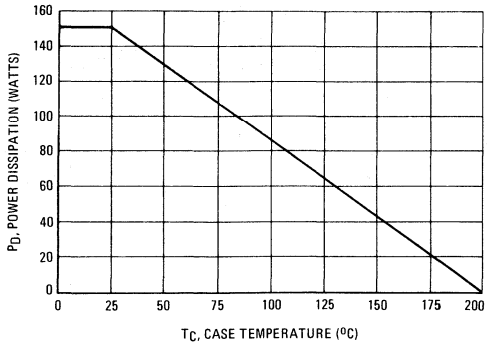
MAXIMUM RATINGS

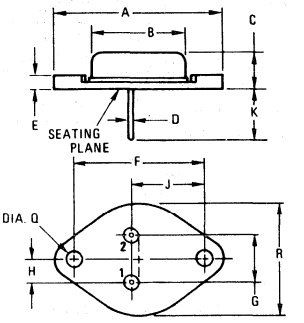
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current	I_B	7.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

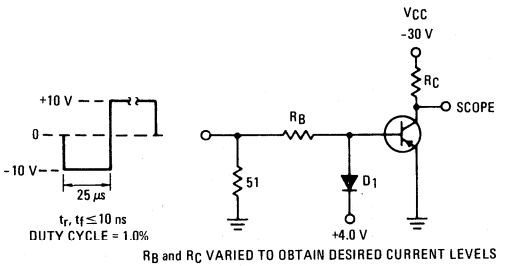
CASE 11 (TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	70	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	4.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	–	–
Small-Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	$f_{\alpha e}$	10	–	kHz

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



t_r, $t_f \leq 10$ ns
DUTY CYCLE = 1.0%

R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

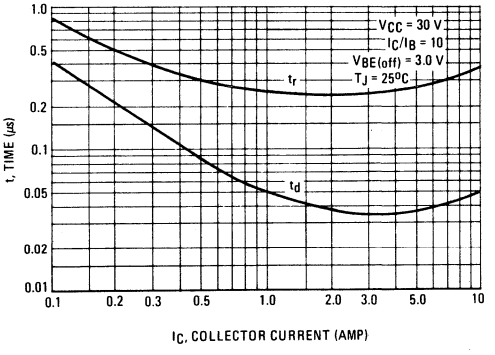


FIGURE 4 – THERMAL RESPONSE

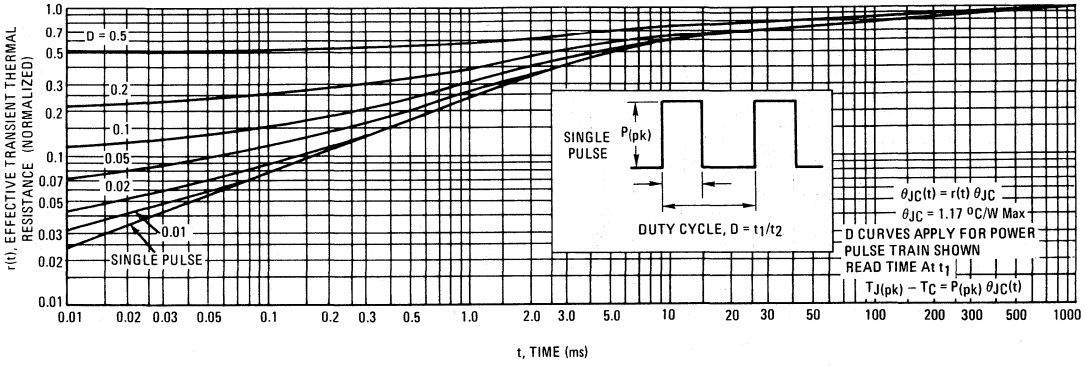
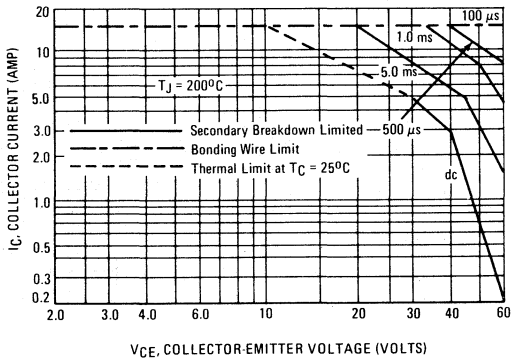


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \approx 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

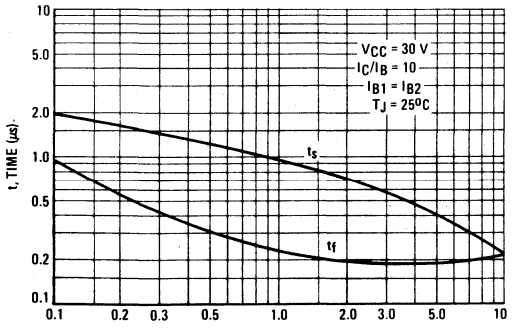


FIGURE 7 – CAPACITANCE

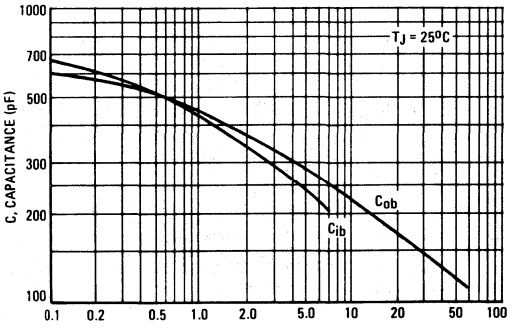


FIGURE 8 – DC CURRENT GAIN

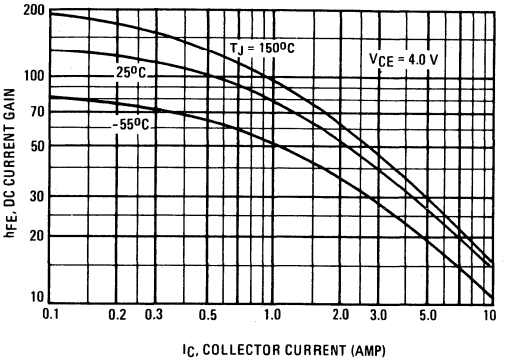


FIGURE 9 – COLLECTOR SATURATION REGION

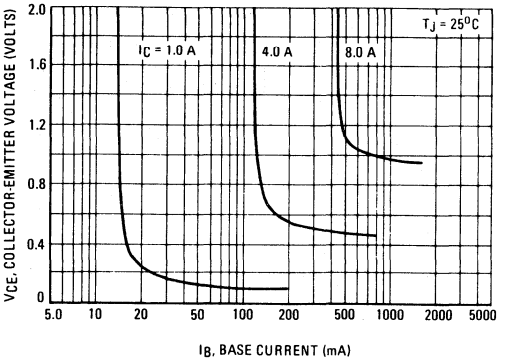


FIGURE 10 – "ON" VOLTAGES

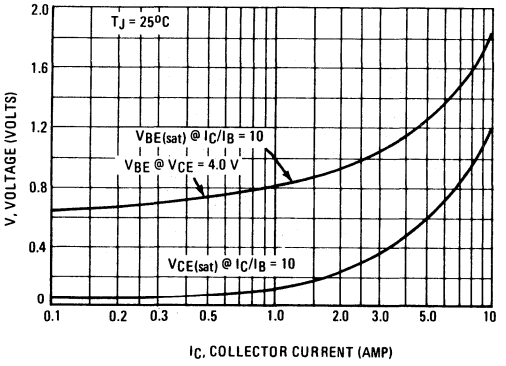


FIGURE 11 – TEMPERATURE COEFFICIENTS

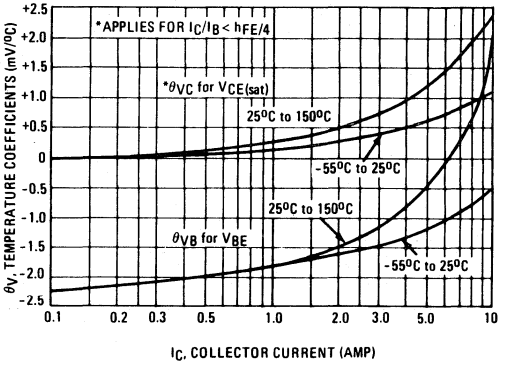


FIGURE 12 – COLLECTOR CUTOFF REGION

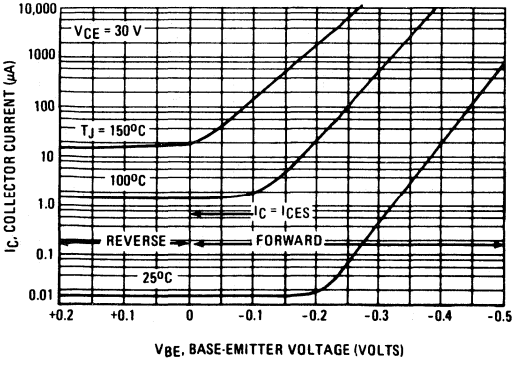
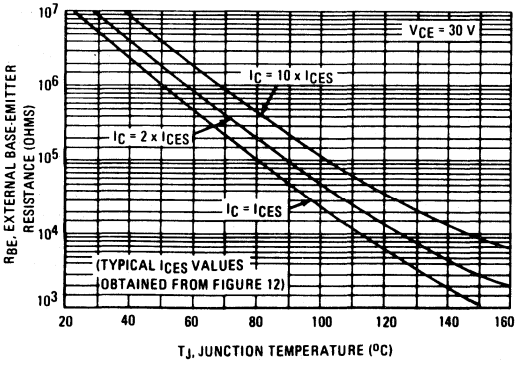


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

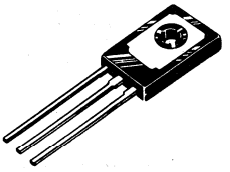
. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad ▲ Construction Provides High Power Dissipation Rating for High Reliability
- Choice of Packages – MJE340 – Case 77

0.5 AMPERE POWER TRANSISTOR

NPN SILICON

300 VOLTS
20.8 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20.8 0.167	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

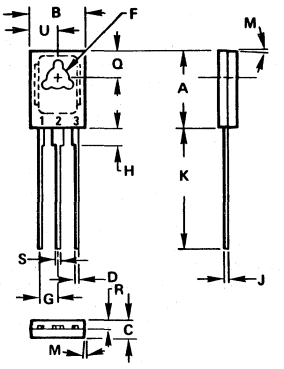
THERMAL CHARACTERISTICS

Characteristic	Symbol		Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.0	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–

▲Trademark of Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3^0 TYP		3^0 TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

CASE 77-03

FIGURE 1 – POWER TEMPERATURE DERATING

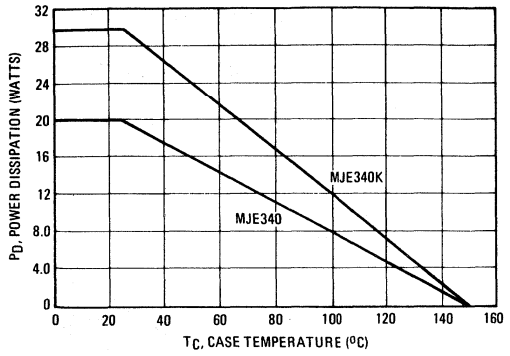
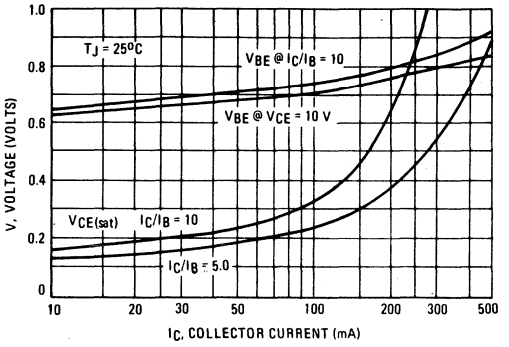


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 3 – MJE340

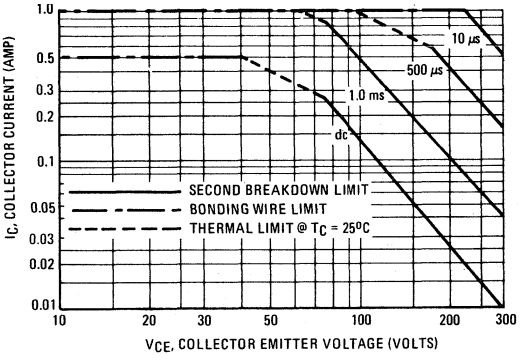
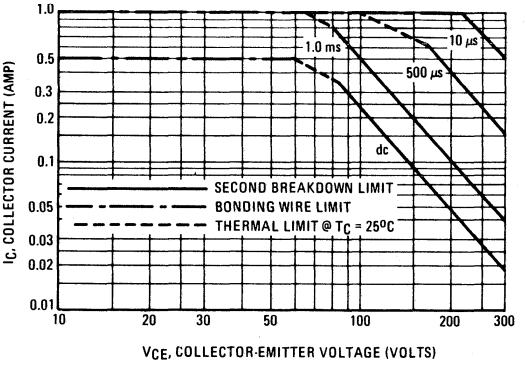


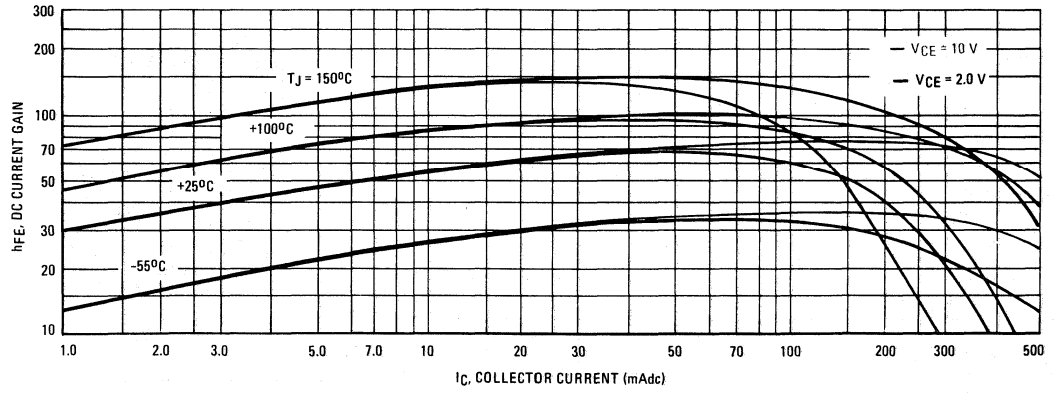
FIGURE 4 – MJE340K



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (Seee AN-415)

FIGURE 5 – DC CURRENT GAIN



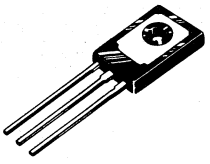
PLASTIC MEDIUM POWER PNP SILICON TRANSISTOR

. . . designed for use in line-operated audio and television applications and as low power, line-operated series pass and switching regulators.

- High Collector-Emitter Sustaining Voltage – $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain – h_{FE} = 30-240 @ I_C = 50 mAdc
- Plastic Thermopad▲ Package

0.5 AMPERE POWER TRANSISTOR PNP SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

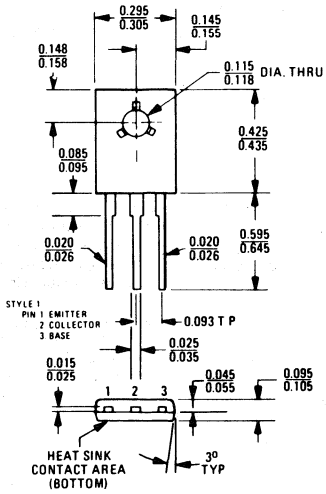
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–



CASE 77-03

FIGURE 1 – DC CURRENT GAIN

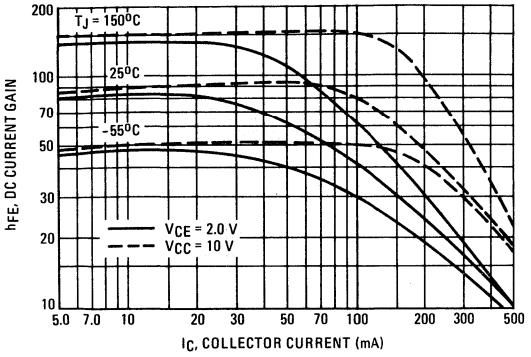


FIGURE 2 – "ON" VOLTAGES

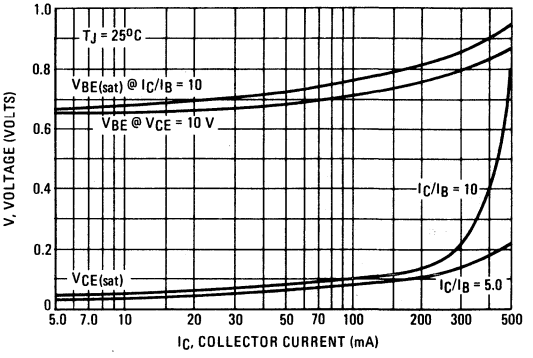


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

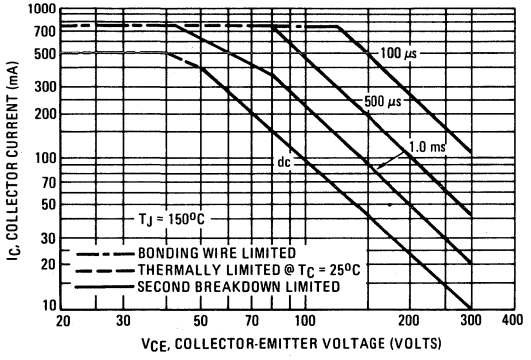
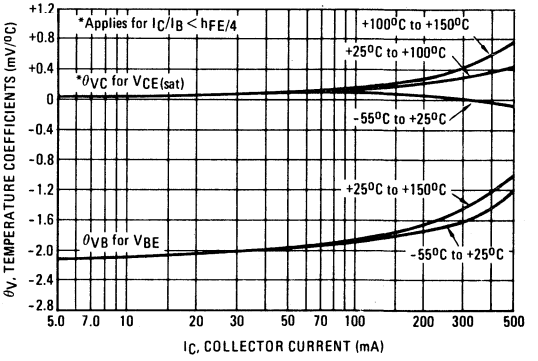


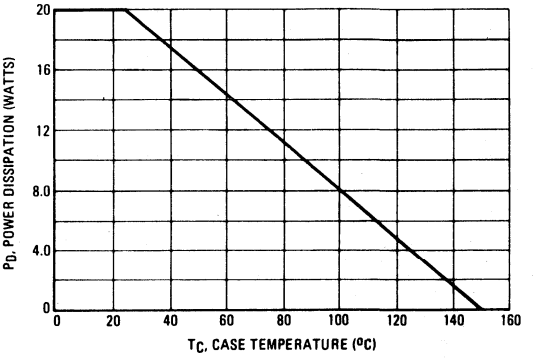
FIGURE 4 – TEMPERATURE COEFFICIENTS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 5 – POWER DERATING



HIGH POWER PNP SILICON TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current-Gain — Bandwidth Product — f_T = 2.0 MHZ (Min) @ I_C = 500 mAdc
- Thermopad▲ High-Efficiency Compact Package
- **Complement to NPN MJE3055, MJE3055T**
- **Choice of Packages — MJE2955-Case 90, MJE2955T TO-220**

10 AMPERE POWER TRANSISTORS PNP SILICON

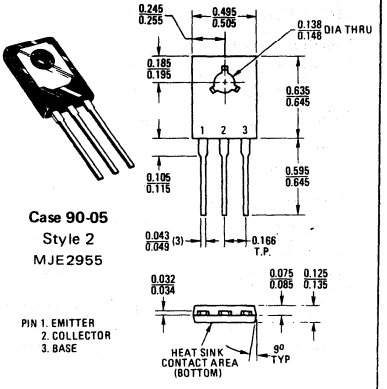
60 VOLTS
90, 75 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJE 2955	MJE 2955T	Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	70		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	10		Adc
Base Current-Continuous	I_B	6.0		Adc
Total Device Dissipation @ T_C = 25 °C[1] Derate above 25 °C	P_D	90 0.718	75 0.6	Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

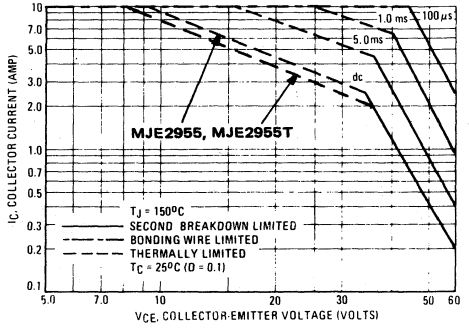
Characteristic	Symbol	Max.		Unit.
Thermal Resistance, Junction to Case	θ_{JC}	1.39	1.67	°C/W



Case 90-05
Style 2
MJE2955

To convert inches to millimeters multiply by 25.4

FIGURE 1 — ACTIVE REGION SAFE OPERATING AREAS



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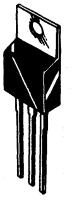
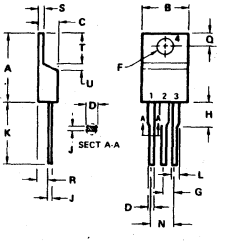
The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415)

(1)Safe Area Curves are indicated by Figure 1 — Both thermal and safe area limits are applicable and must be observed.

MJE2955T





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

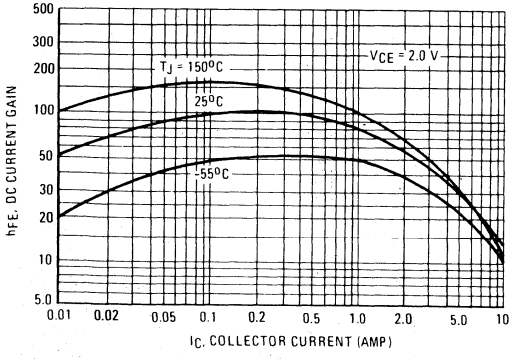
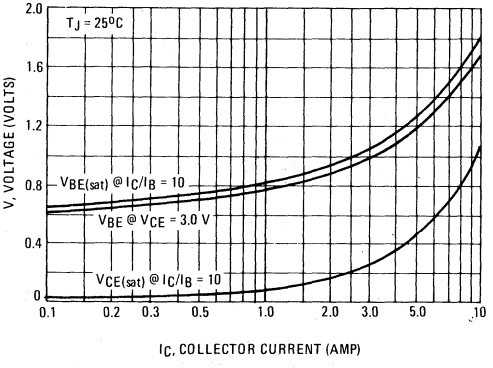


FIGURE 3 – "ON" VOLTAGES



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- DC Current Gain Specified to 10 Amperes
- High Current Gain – Bandwidth Product – f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Thermopad ▲ High-Efficiency Compact Package
- Complement to PNP MJE2955, MJE2955T
- Choice of Packages – MJE3055 – Case 90
  MJE3055T – TO-220

10 AMPERE POWER TRANSISTORS

NPN SILICON

60 VOLTS
90, 75 WATTS

MAXIMUM RATINGS

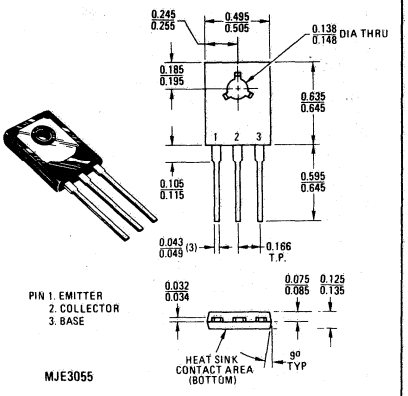
Rating	Symbol	MJE 3055	MJE 3055T	Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	70		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	10		Adc
Base Current-Continuous	I_B	6.0		Adc
Total Device Dissipation @ T_C = 25 °C[1] Derate above 25 °C	P_D	90 0.718	75 0.6	Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.		Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	1.67	°C/W

[1] Safe Area Curves are indicated by figure 1 – Both thermal and safe area limits are applicable and must be observed.

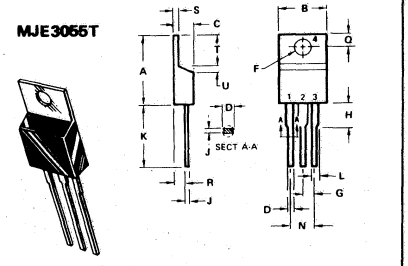
▲ Trademark of Motorola Inc.



To convert inches to millimeters multiply by 25.4

CASE 90-05

MJE3055T



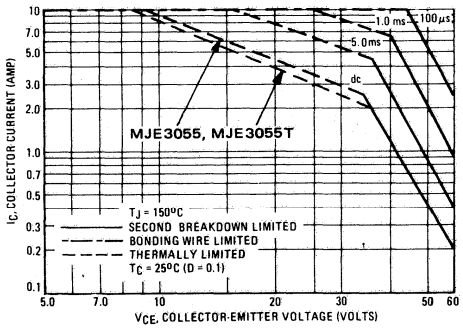
CASE 221A-02
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 1.0 5.0	mAdc
Colltector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 – –	 1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2.0%.

FIGURE 2 – DC CURRENT GAIN

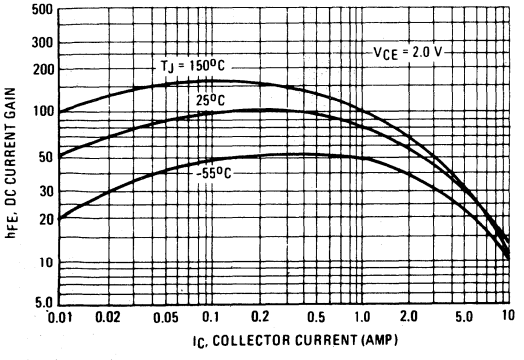
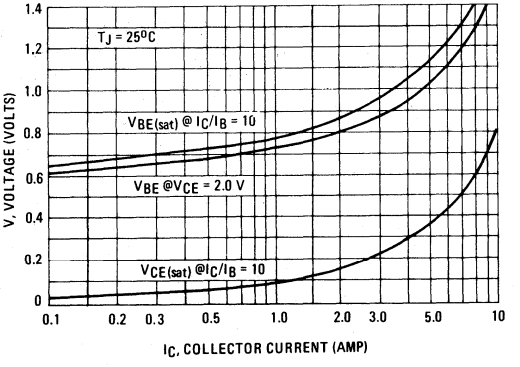


FIGURE 3 – "ON" VOLTAGES



MJE13002
MJE13003

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13002 and MJE13003 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

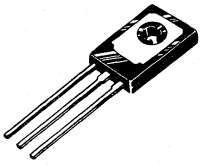
SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C . . . t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

1.5 AMPERE
NPN SILICON POWER TRANSISTORS
300 and 400 VOLTS
40 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



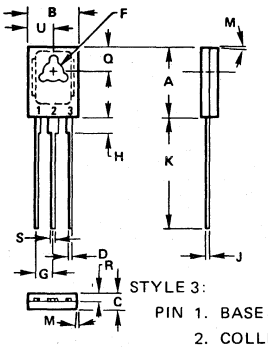
MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.42 11.5		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	88	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

CASE 77-03
Similar to TO-126

▲Trademark of Motorola Inc.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13002	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13003		400	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			Adc
ON CHARACTERISTICS[1]					
DC Current Gain	h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 2 Vdc)		8	–	40	
(I_C = 1 Adc, V_{CE} = 2 Vdc)		5	–	25	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)		–	–	0.5	
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)		–	–	3	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		–	–	1	
Base-Emitter Sautration Voltage	$V_{BE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)		–	–	1	
(I_C = 1 Adc, I_B = 0.25 Adc)		–	–	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		–	–	1.1	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	5	10	–	MHz
Output Capacitance (V_{CB} - 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 1 A,	t_d	–	0.05	0.1	μs
Rise Time I_{B1} = I_{B2} = 0.2 A, t_p - 25 μs,	t_r	–	0.5	1	μs
Storage Time Duty Cycle ≤ 1%)	t_s	–	2	4	μs
Fall Time	t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 1 A, V_{clamp} = 300 Vdc,	t_{sv}	–	1.7	4	μs
Commutation Time I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.29	0.75	μs

[1] Pulse Test: Pulse width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATION AREA

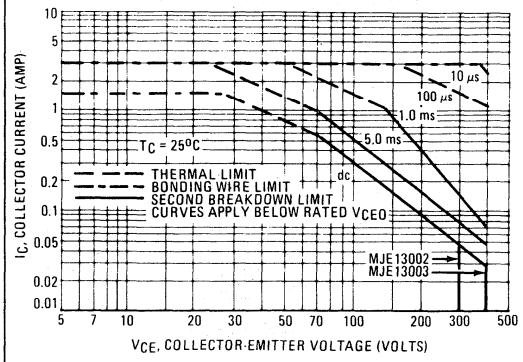
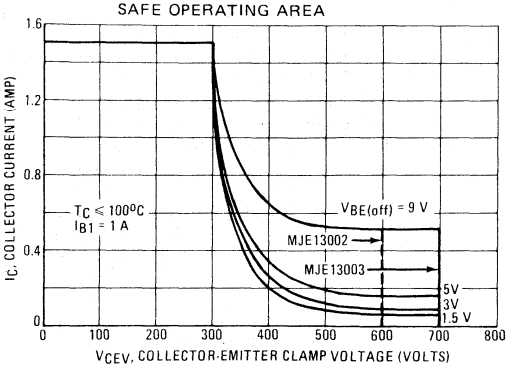
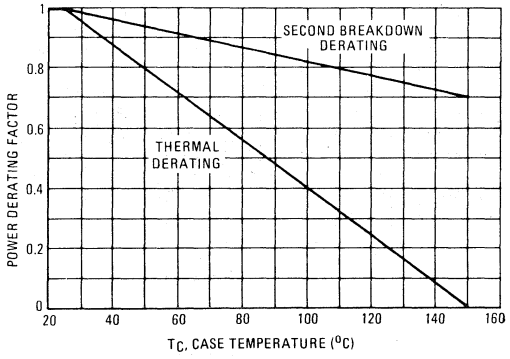


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the designer's application section.

FIGURE 4 – THERMAL RESPONSE

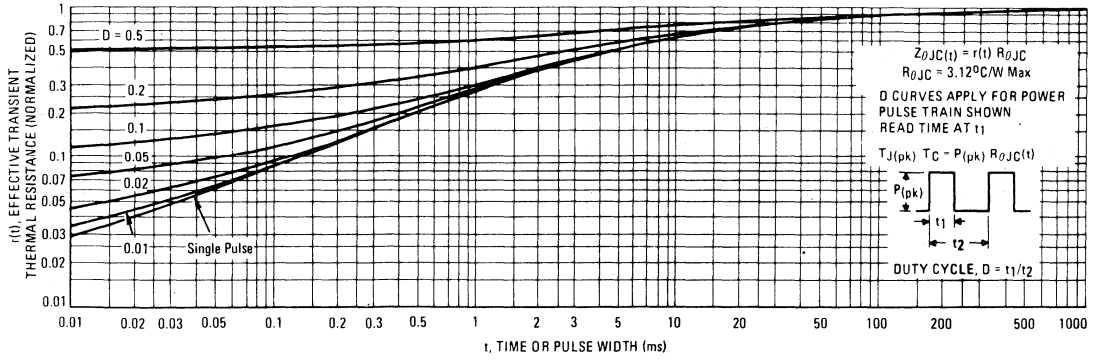


FIGURE 5 – DC CURRENT GAIN

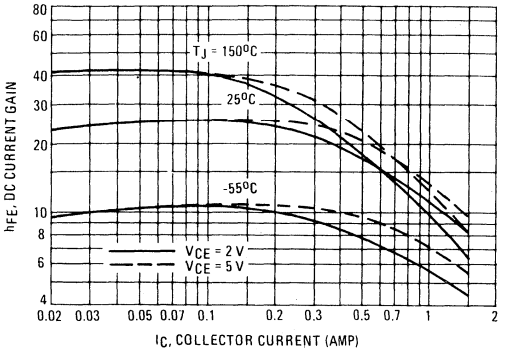


FIGURE 6 – COLLECTOR SATURATION REGION

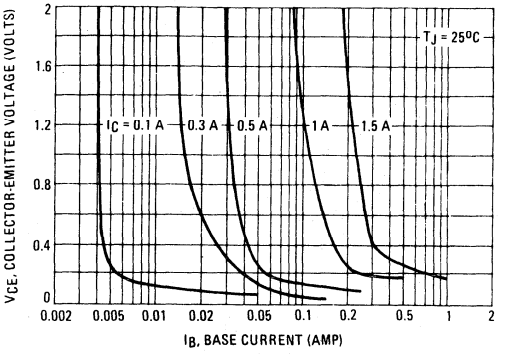


FIGURE 7 – BASE-EMITTER VOLTAGE

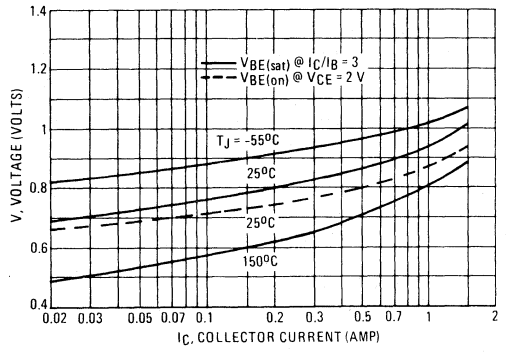


FIGURE 8 – COLLECTOR-EMITTER SATURATION REGION

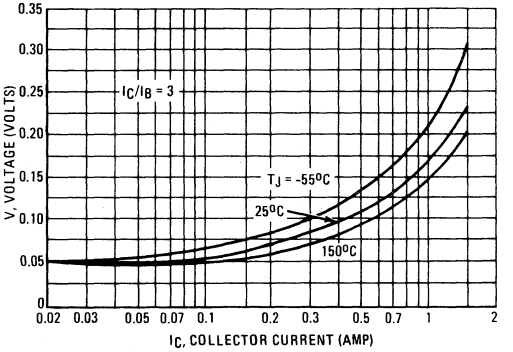


FIGURE 9 – COLLECTOR CUTOFF REGION

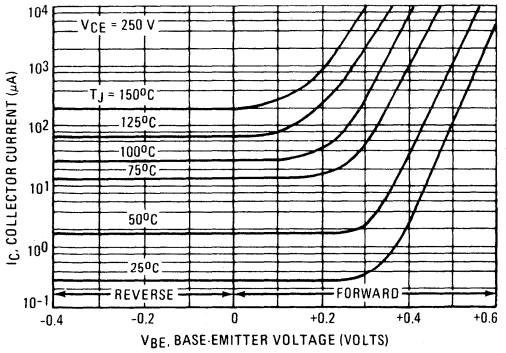


FIGURE 10 – CAPACITANCE

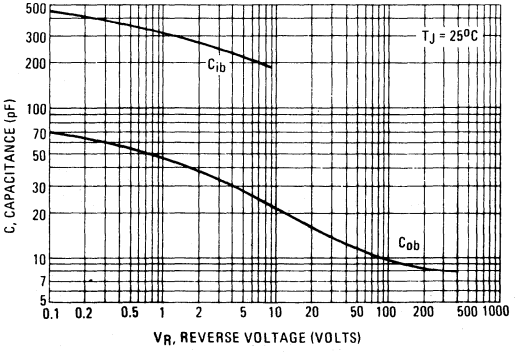
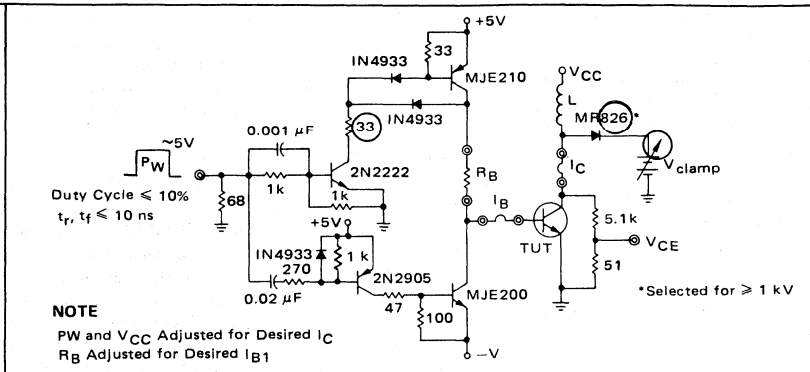
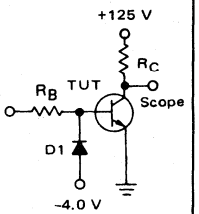
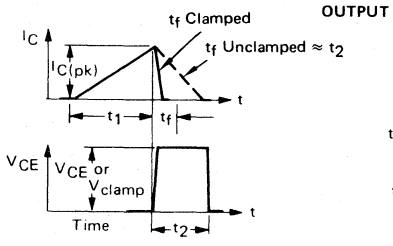
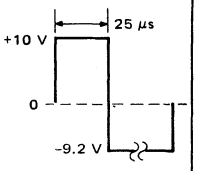


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	R_B SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equiv. R_B = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737 and Engineering Bulletin EB-39.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 1 ampere which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

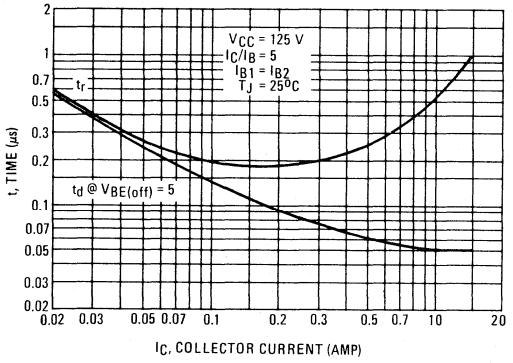


FIGURE 12 – TURN-OFF TIME

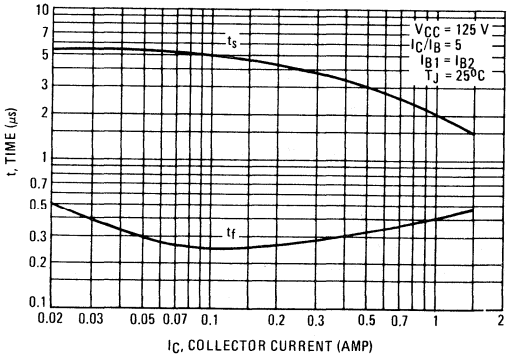


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

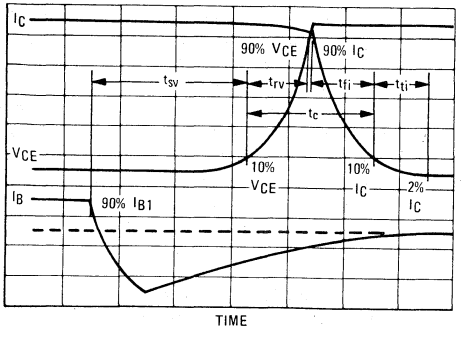


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 1 A with I_{B1} = 0.2 A and $V_{BE(off)}$ = 5.0 V)

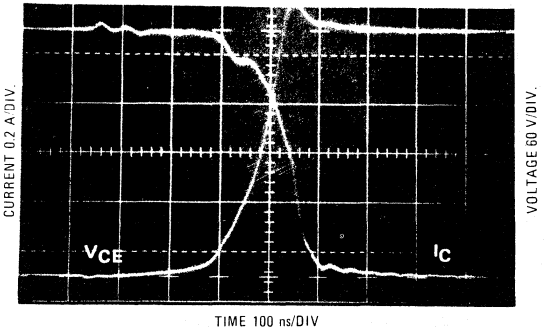


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

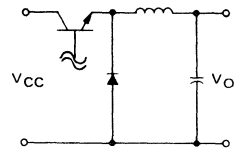
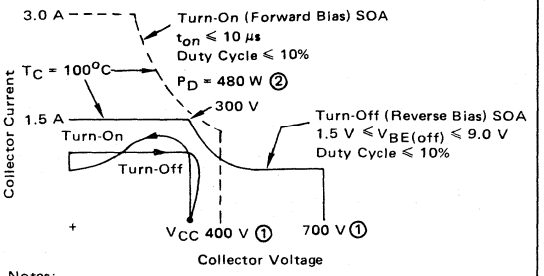
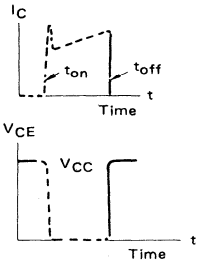
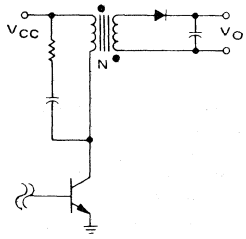
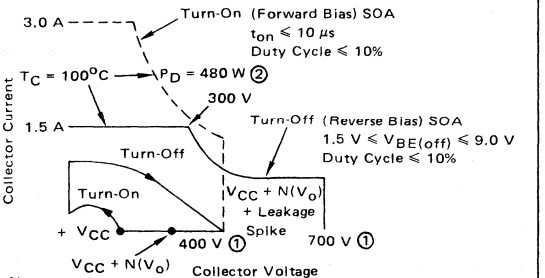
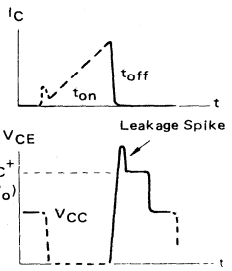
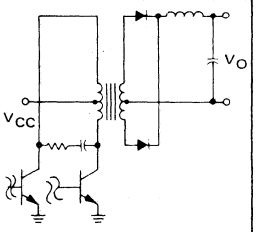
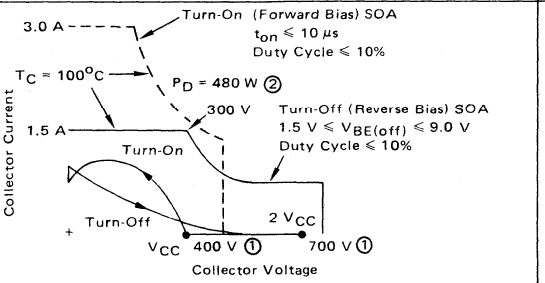
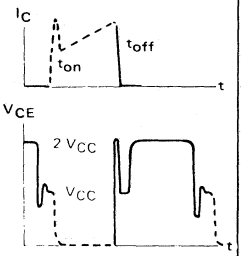
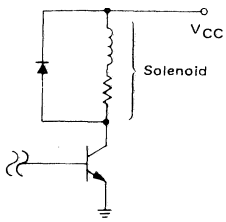
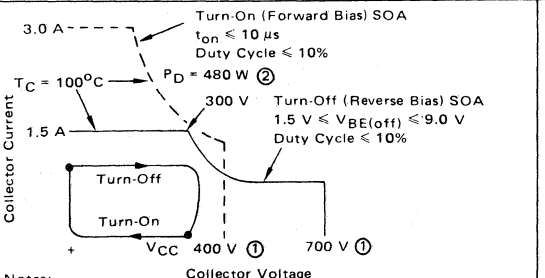
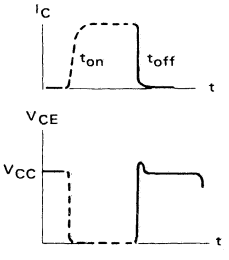
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13002 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PWM PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE}

t_{rv} = Voltage Rise Time, 10-90% V_{CE}

t_{fi} = Current Fall Time, 90-10% I_C

t_{ti} = Current Tail, 10-2% I_C

t_c = Commutation Time, 10% V_{CE} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the commutation interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TO-126 MOUNTING NOTE (CASE 77)

The preferred mounting technique for high-voltage applications is to direct mount the transistor and to insulate the heat sink. However, if the transistor must be insulated from the heat sink, a 4-40 screw with a compression washer and a 3 mil mica washer with grease (DC340) can be used to mount these TO-126 transistors. Typical hi-pot readings from the collector to this mounting hardware are 500 V dry and 1500 V with grease. For added safety, an insulated screw may be used.

MJE13006
MJE13007

Designers▲ Data Sheet

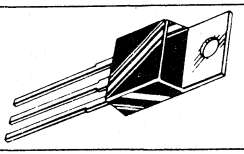
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C
  ... t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

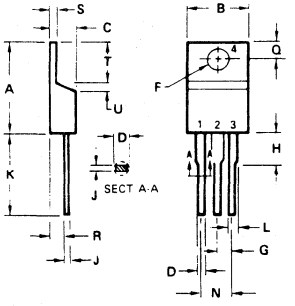
MAXIMUM RATINGS

Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	8 16		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	4 8		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	12 24		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

▲Trademark of Motorola Inc

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13006	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13007		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased		–	See Figure 2			
***ON CHARACTERISTICS**						
DC Current Gain		h_{FE}				
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	–	40	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			6	–	30	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			–	–	1	
(I_C = 5 Adc, I_B = 1 Adc)			–	–	1.5	
(I_C = 8 Adc, I_B = 2 Adc)			–	–	3	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			–	–	1.2	
(I_C = 5 Adc, I_B = 1 Adc)			–	–	1.6	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	110	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 5 A,	t_d	–	0.05	0.1	μs
Rise Time	I_{B1} = I_{B2} = 1 A, t_p = 25 μs,	t_r	–	0.5	1	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1	3	μs
Fall Time		t_f	–	0.15	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 5 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.86	2.3	μs
Crossover Time	I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.14	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

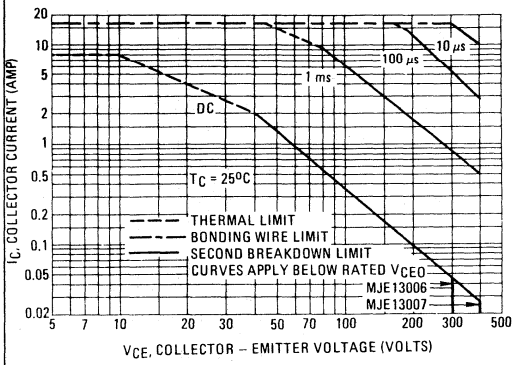
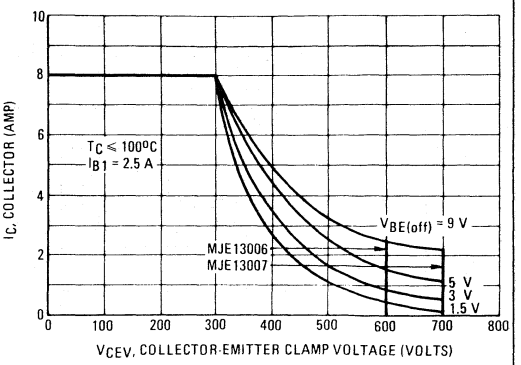
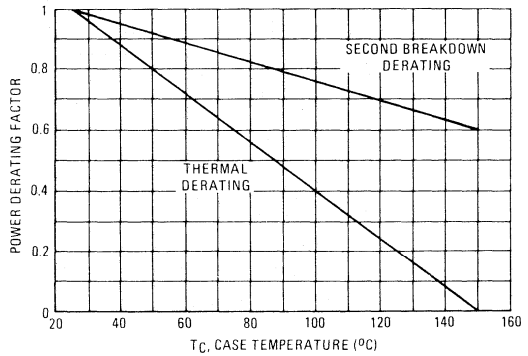


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

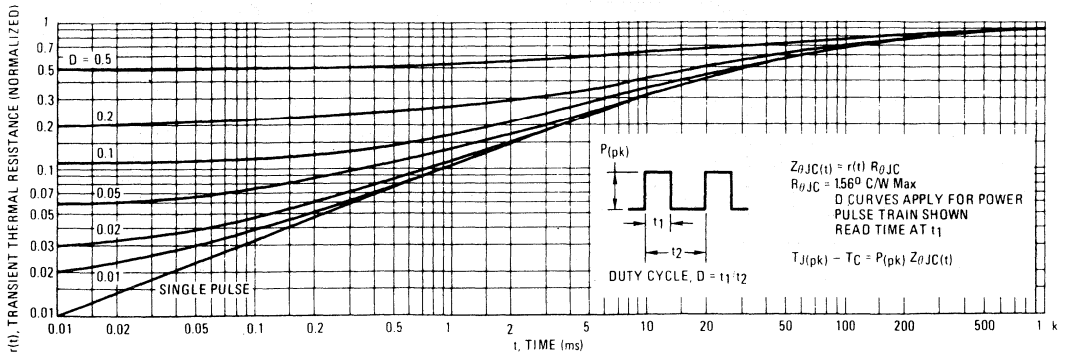


FIGURE 5 –DC CURRENT GAIN

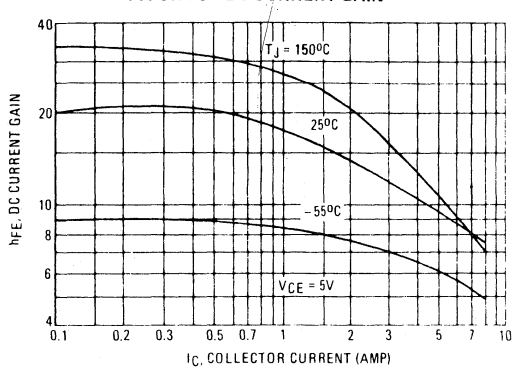


FIGURE 6 – COLLECTOR SATURATION REGION

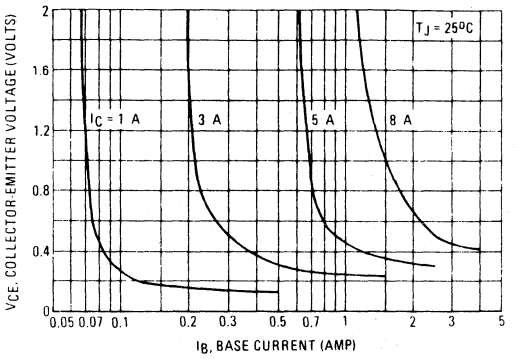


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

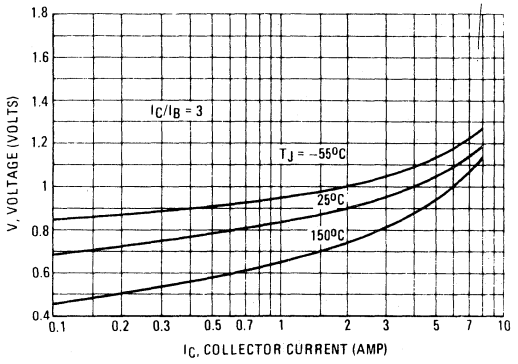


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

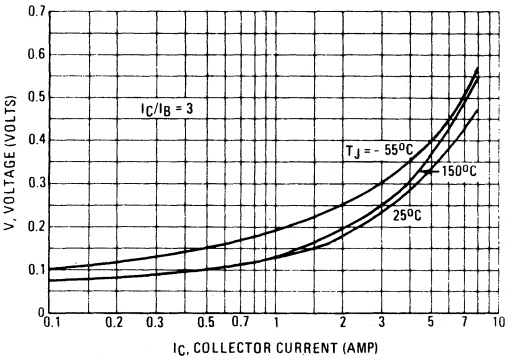


FIGURE 9 – COLLECTOR CUTOFF REGION

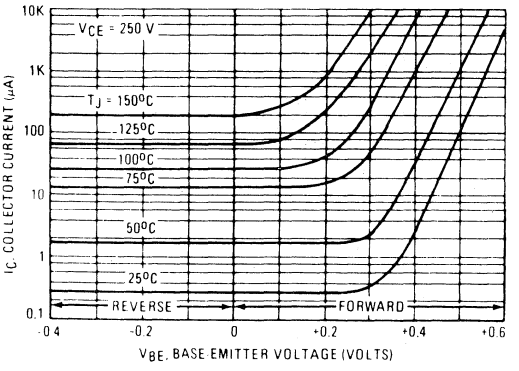


FIGURE 10 – CAPACITANCE

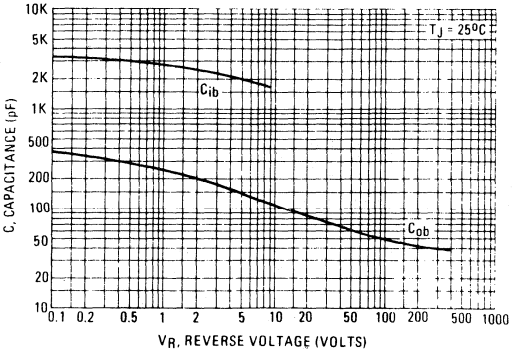
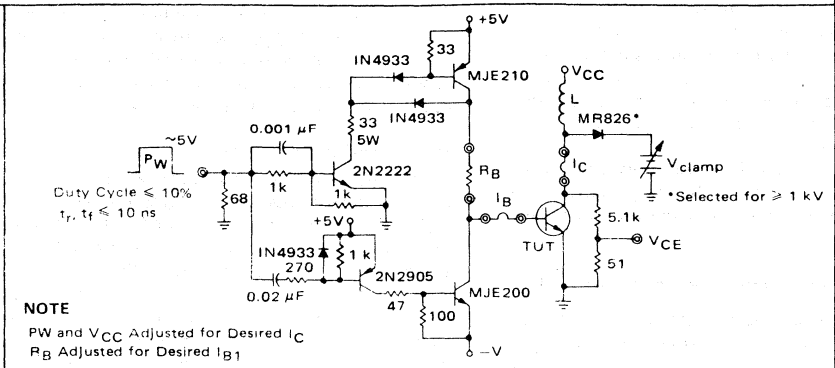
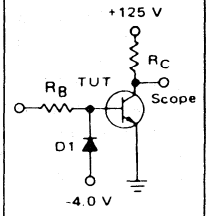
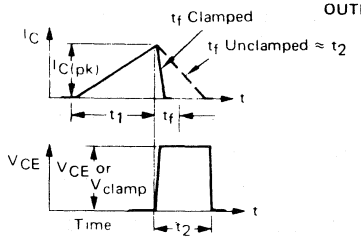
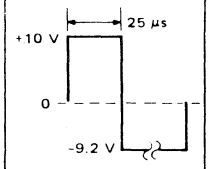


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A Lcoil = 200 μH VCC = 20 V Vclamp = 300 Vdc	VCC = 125 V RC = 24.7 Ω D1 = 1N5820 or Equiv RB = 10Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t1 Adjusted to Obtain IC $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 tr, tf < 10 ns Duty Cycle = 1.0% RB and RC adjusted for desired IB and IC

APPLICATIONS INFORMATION FOR SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

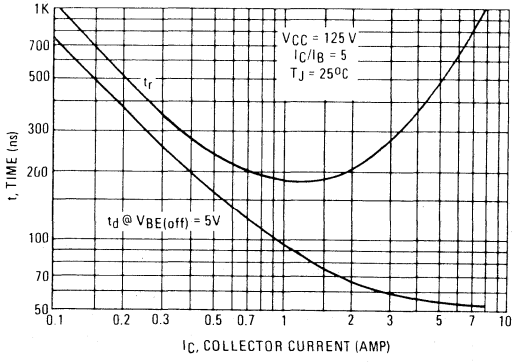


FIGURE 12 – TURN-OFF TIME

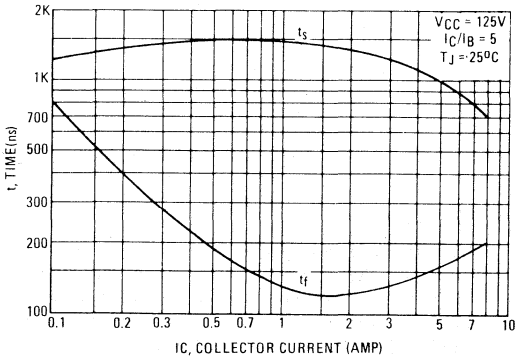


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

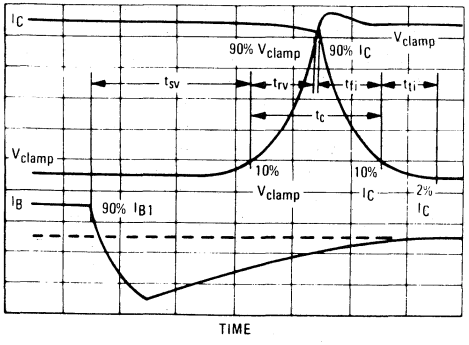


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 8A with I_{B1} = 1.6A and $V_{BE(off)}$ = 5 V)

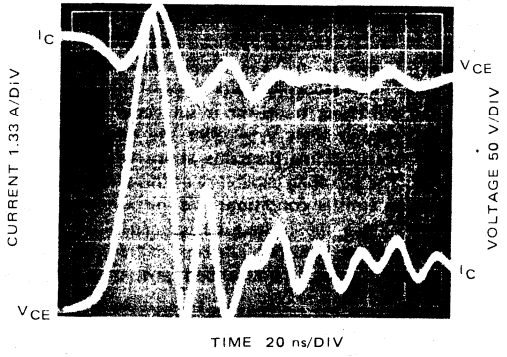


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

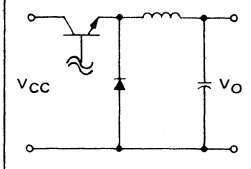
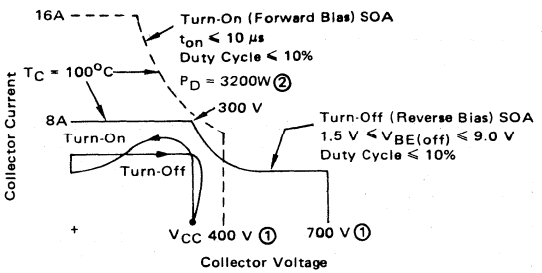
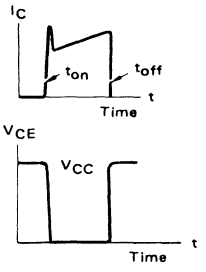
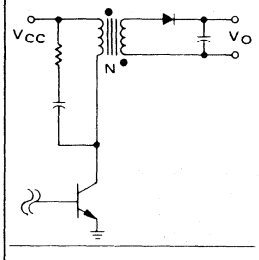
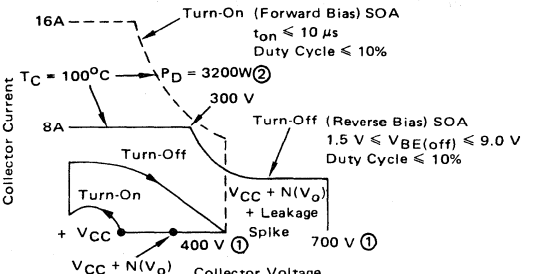
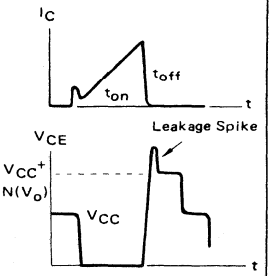
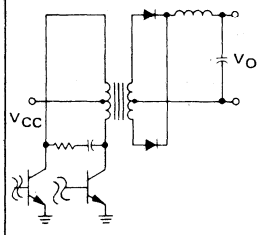
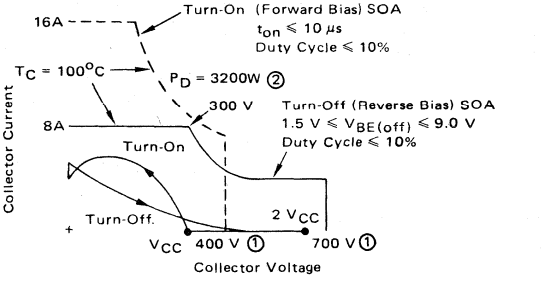
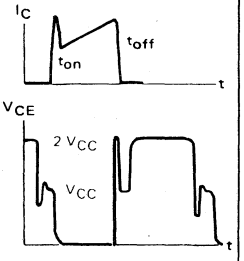
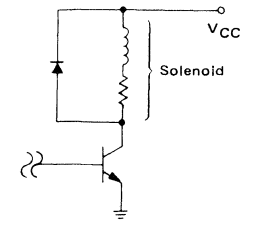
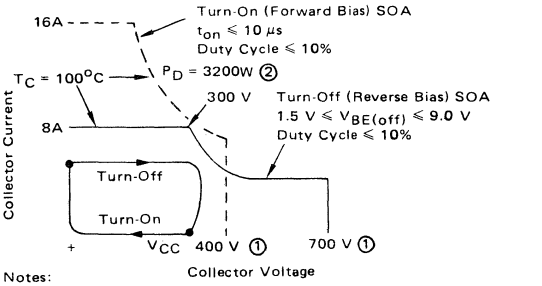
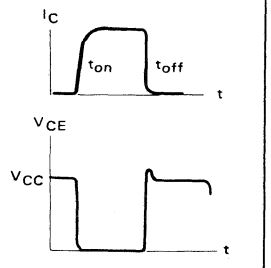
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MJE13008
MJE13009

Designers▲ Data Sheet

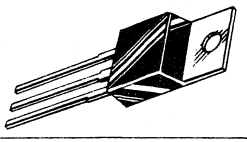
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C
  . . . t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

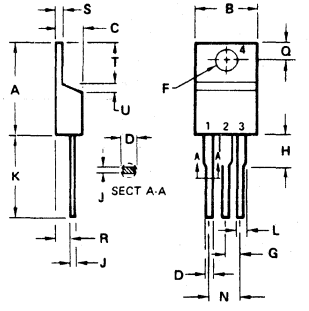
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	100 800		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4 COLLECTOR

NOTE.
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13008	$V_{CEO(sus)}$	300	–	–	Vdc
MJE13009		400	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				
(I_C = 5 Adc, V_{CE} = 5 Vdc)		8	–	40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	–	30	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1Adc)		–	–	1	
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		–	–	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1.2	
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 8 A,	t_d	–	0.06	0.1	μs
Rise Time I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs,	t_r	–	0.45	1	μs
Storage Time Duty Cycle ≤ 1%)	t_s	–	1.3	3	μs
Fall Time	t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 8 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.92	2.3	μs
Crossover Time I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

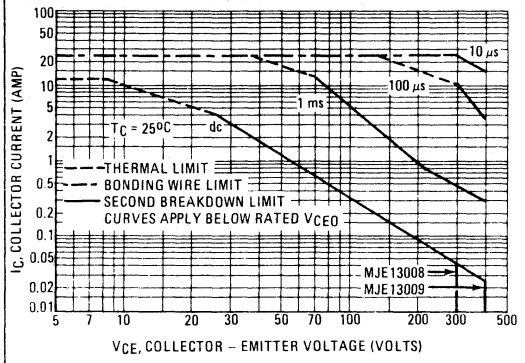
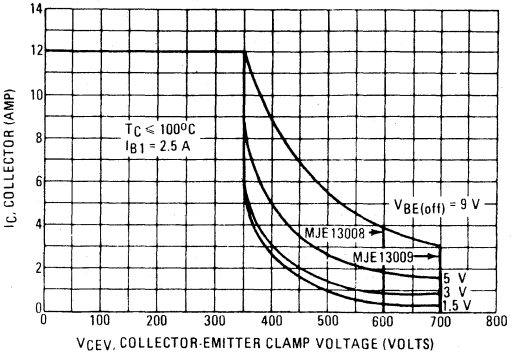
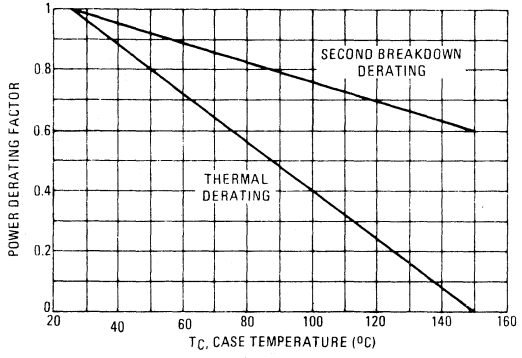


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

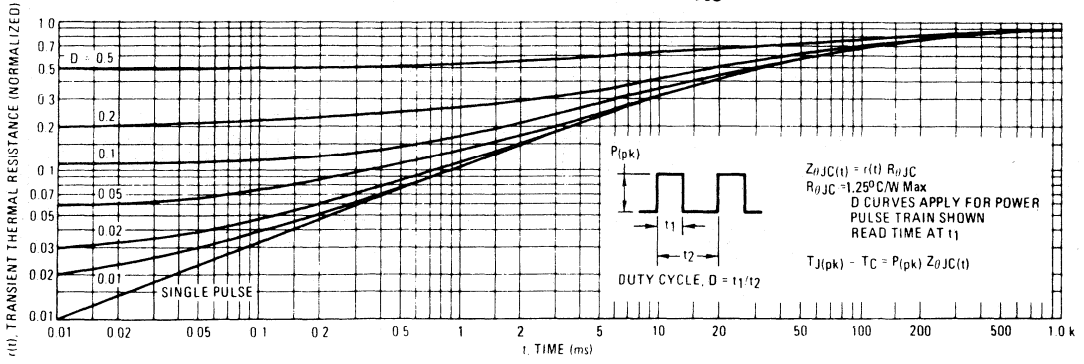


FIGURE 5 – DC CURRENT GAIN

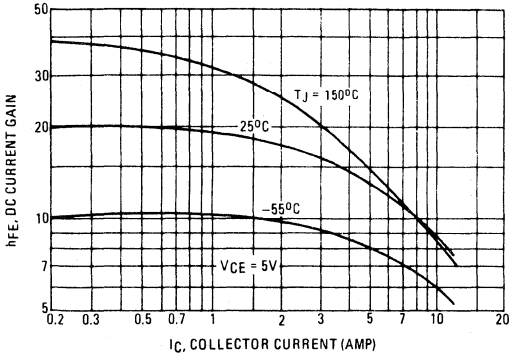


FIGURE 6 – COLLECTOR SATURATION REGION

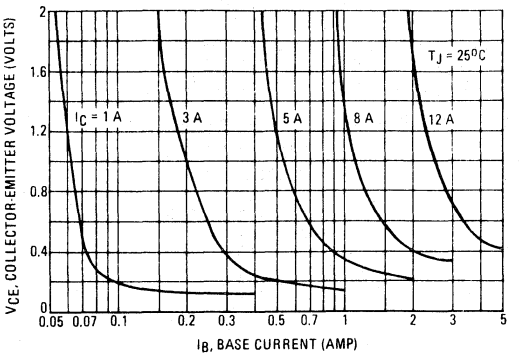


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

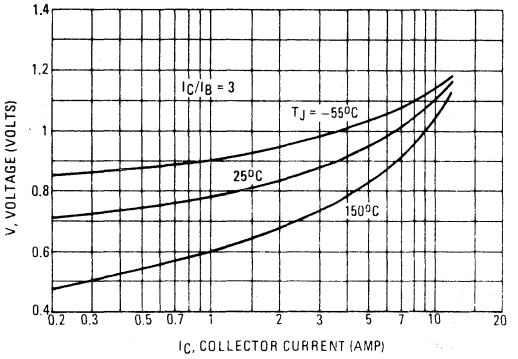


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

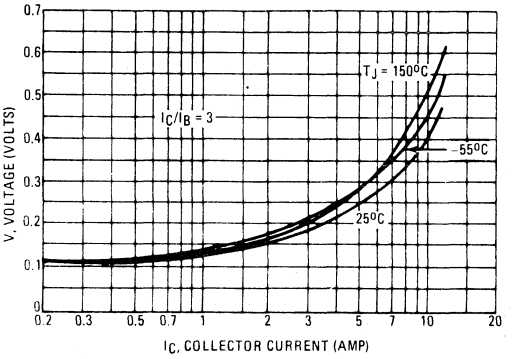


FIGURE 9 – COLLECTOR CUTOFF REGION

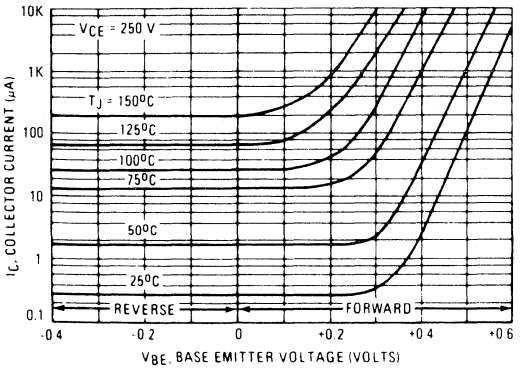


FIGURE 10 – CAPACITANCE

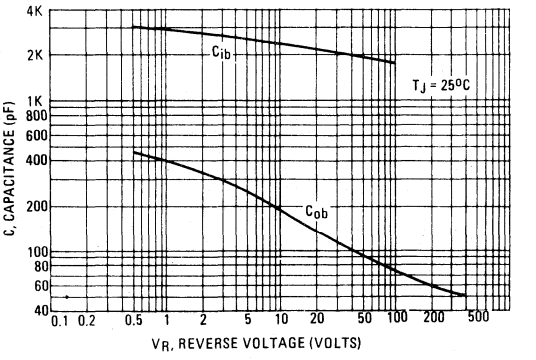
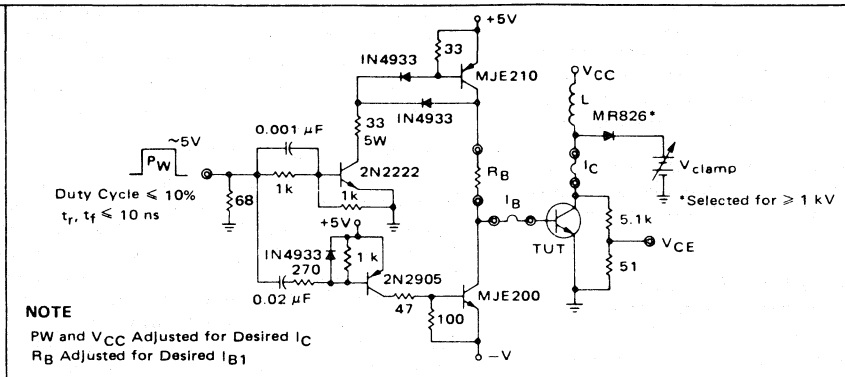
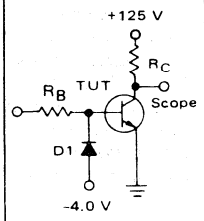
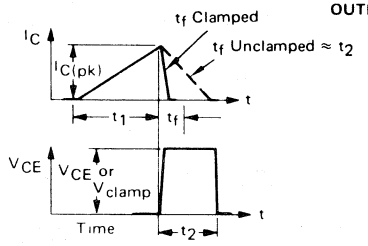
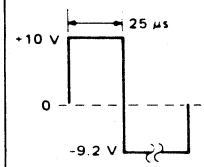


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15.4 Ω D1 = 1N5820 or Equiv R_B = 5Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 10% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

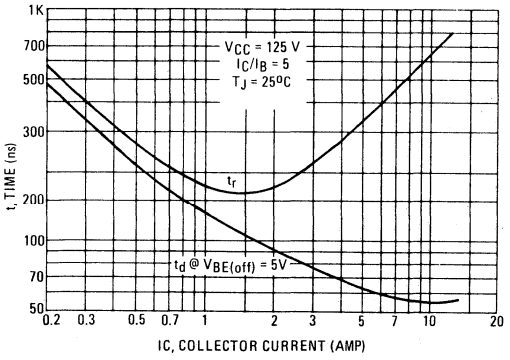


FIGURE 12 – TURN-OFF TIME

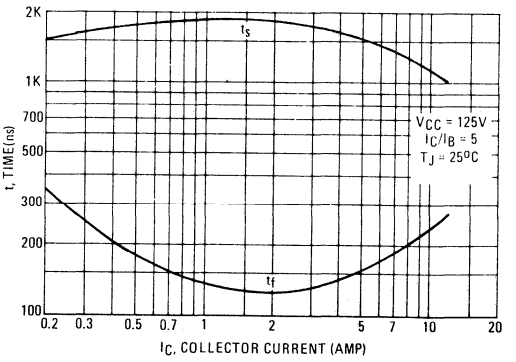


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

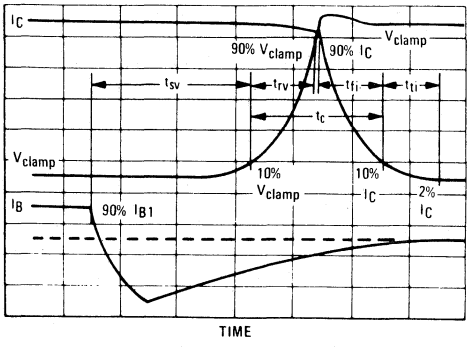


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

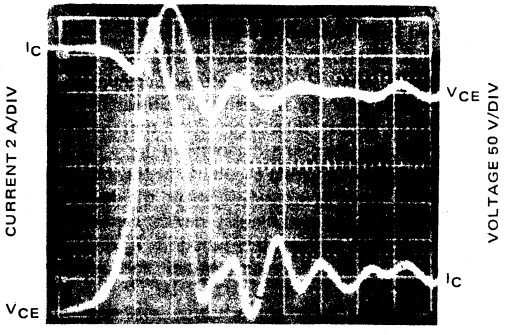


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

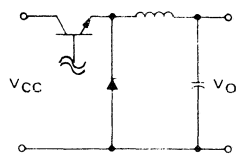
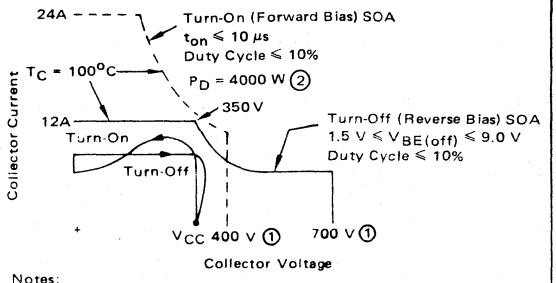
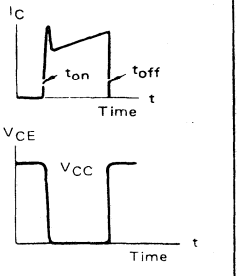
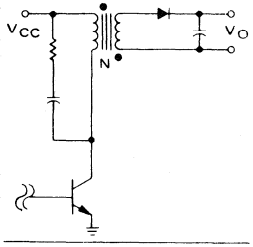
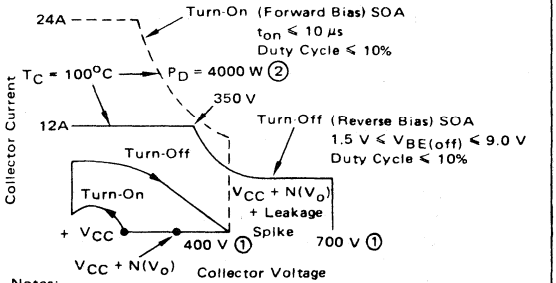
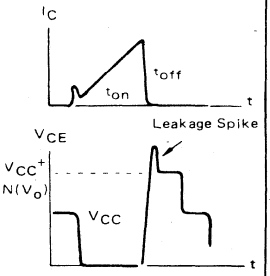
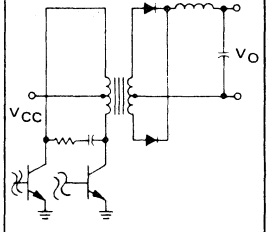
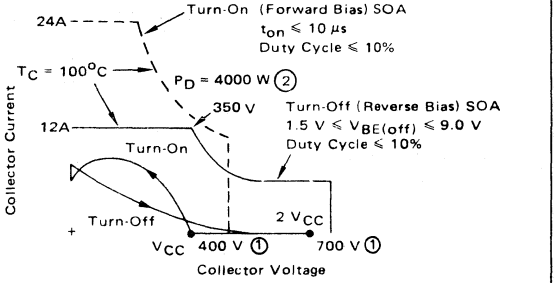
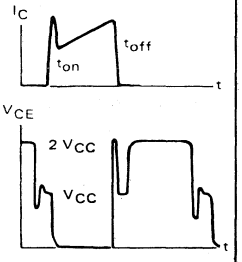
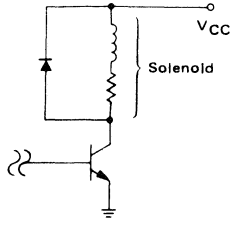
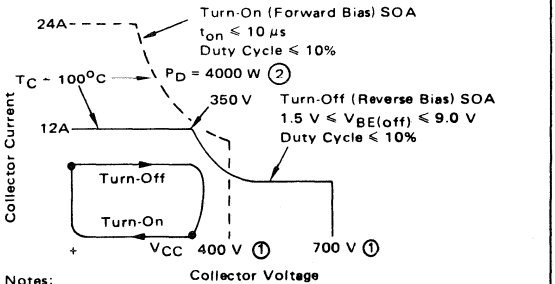
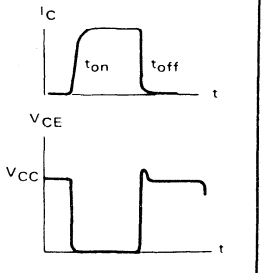
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: (1) MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. (2) See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: (1) MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. (2) See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: (1) MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. (2) See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: (1) MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. (2) See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

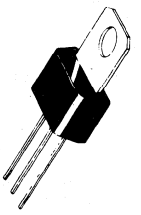
MPS-U45

NPN SILICON DARLINGTON
AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

NPN SILICON DARLINGTON TRANSISTOR

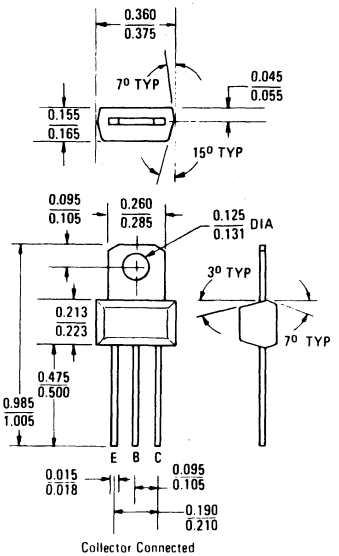


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W



CASE 152

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	12	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	65,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	35,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	1.0	3.2	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	6.0	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

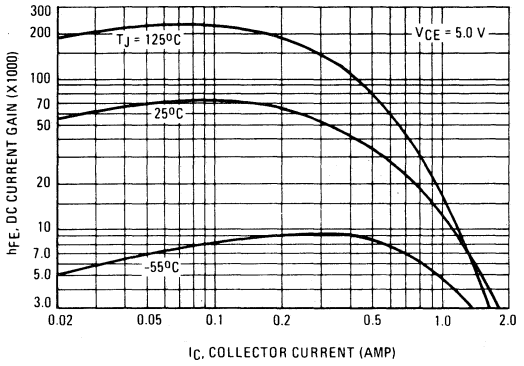


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

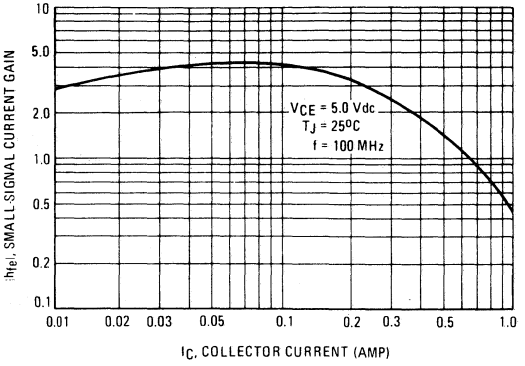


FIGURE 3 – "ON" VOLTAGES

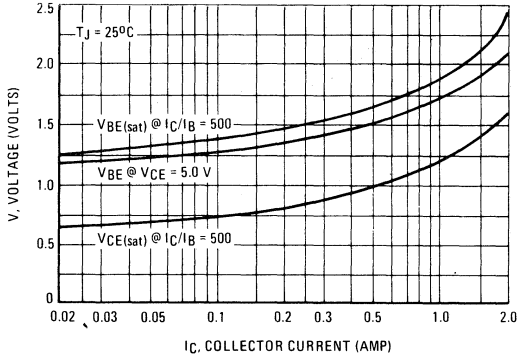


FIGURE 4 – TEMPERATURE COEFFICIENT

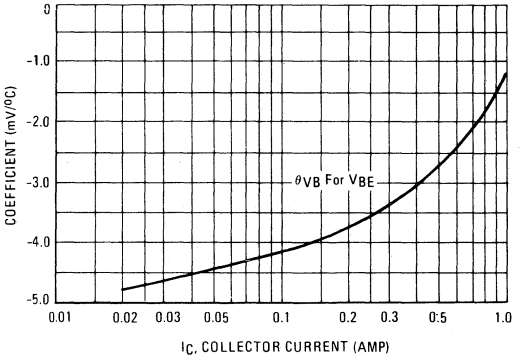
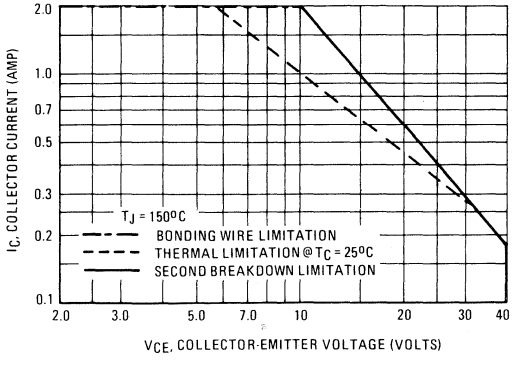


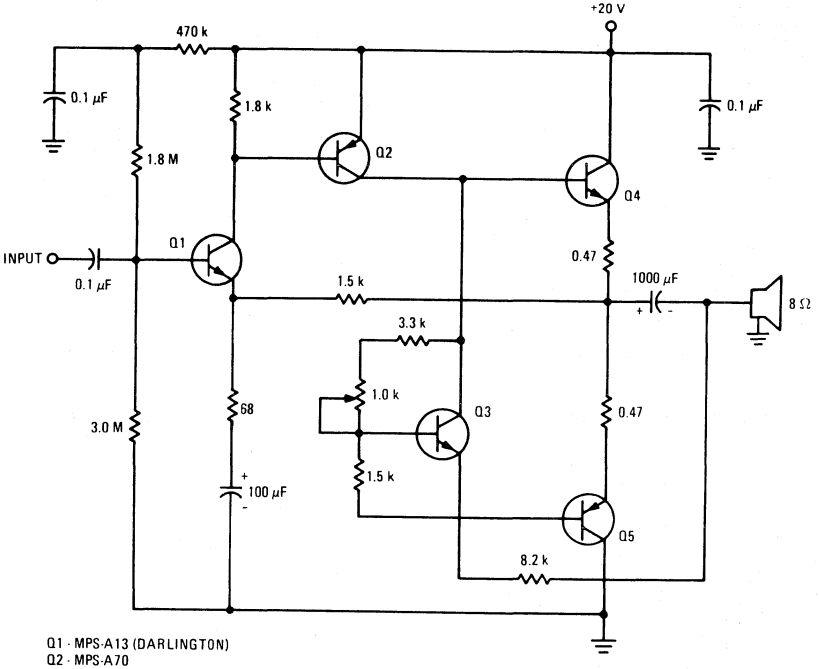
FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

5-WATT AUDIO AMPLIFIER



Q1 - MPS-A13 (DARLINGTON)
Q2 - MPS-A70
Q3 - MPS-A20
Q4 - MPS-U45 } COMPLEMENTARY
Q5 - MPS-U95 } DARLINGTONS

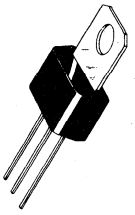
MPS-U95

PNP SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

PNP SILICON DARLINGTON TRANSISTOR

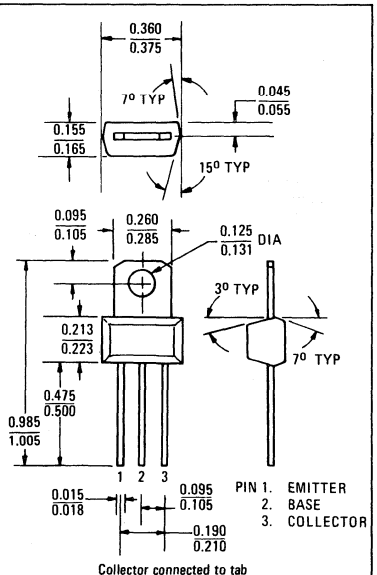


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W



Collector connected to tab

To convert inches to millimeters multiply by 25.4

CASE 152

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	10	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	65,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	35,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	0.5	3.2	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	12	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

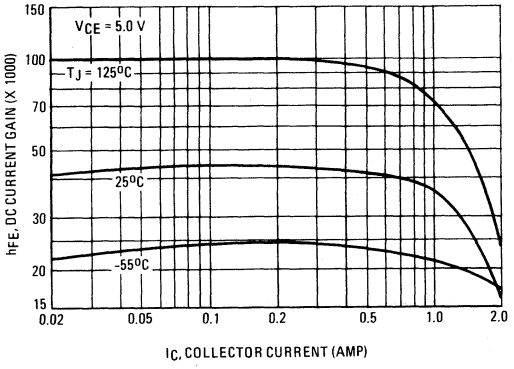


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

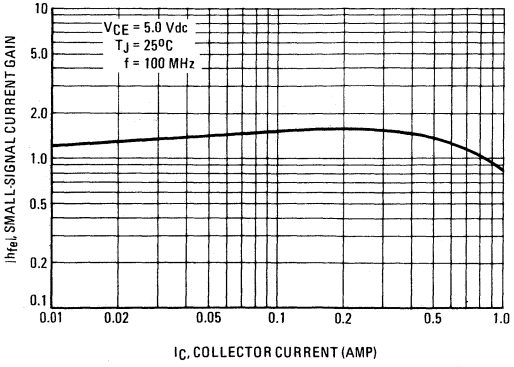


FIGURE 3 – "ON" VOLTAGES

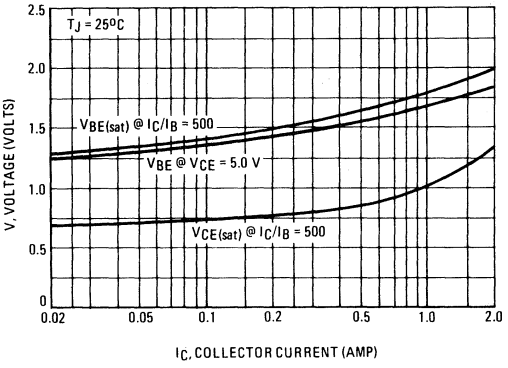


FIGURE 4 – TEMPERATURE COEFFICIENT

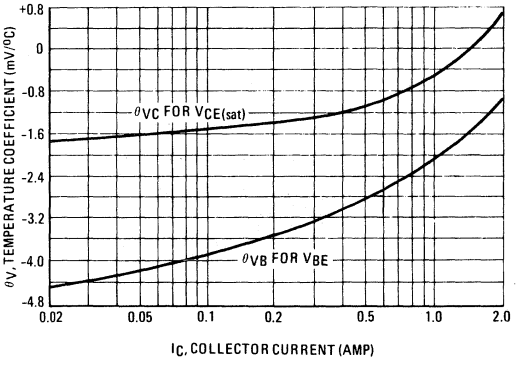
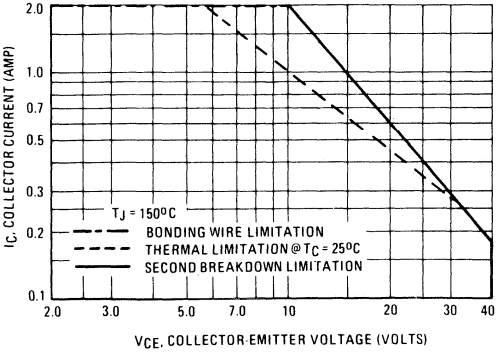


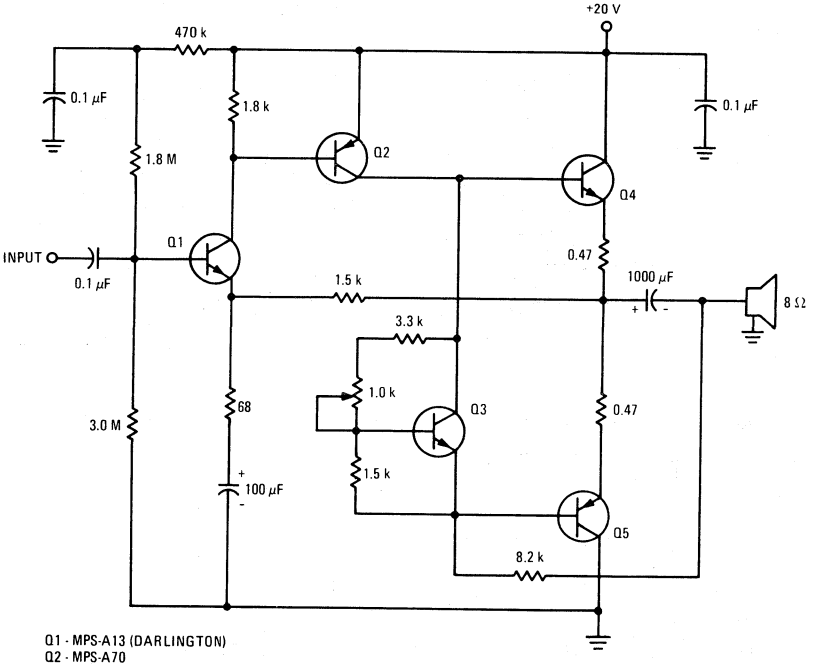
FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

5-WATT AUDIO AMPLIFIER



Q1 - MPS-A13 (DARLINGTON)
Q2 - MPS-A70
Q3 - MPS-A20
Q4 - MPS-U45 } COMPLEMENTARY
Q5 - MPS-U95 } DARLINGTONS

TIP29, 29A, 29B, 29C
TIP30, 30A, 30B, 30C

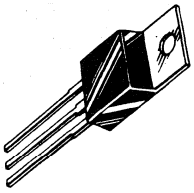
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available.

1 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
30 WATTS



MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	◄ 5.0 ►				Vdc
Collector Current — Continuous	I_C	◄ 1.0 ►				Adc
Peak		◄ 3.0 ►				
Base Current	I_B	◄ 0.4 ►				Adc
Total Device Dissipation @ T_C = 25°C	P_D	◄ 30 ►				Watts
Derate above 25°C		◄ 0.24 ►				W/°C
Total Device Dissipation @ T_A = 25°C	P_D	◄ 2.0 ►				Watts
Derate above 25°C		◄ 0.016 ►				W/°C
Unclamped Inductive Load Energy (See Note 3)	E	◄ 32 ►				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	◄ -65 to +150 ►				°C

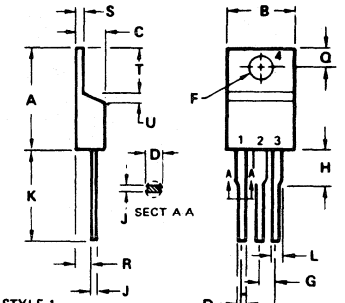
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)	TIP29, TIP30	$V_{CEO(sus)}$	40	–	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP29A, TIP30A		60	–	
	TIP29B, TIP30B		80	–	
	TIP29C, TIP30C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP29, TIP29A, TIP30, TIP30A		–	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	TIP29B, TIP29C, TIP30B, TIP30C		–	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP29, TIP30		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP29A, TIP30A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP29B, TIP30B		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP29C, TIP30C		–	200	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.2 Adc, V_{CE} = 4.0 Vdc)			40	–	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	0.7	Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.3	Vdc
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T	3.0	–	MHz
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Small-Signal Current Gain		h_{fe}	20	–	–
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, R_E = 0.1 Ω, I_C = 1.8 A.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

FIGURE 1 – DC CURRENT GAIN

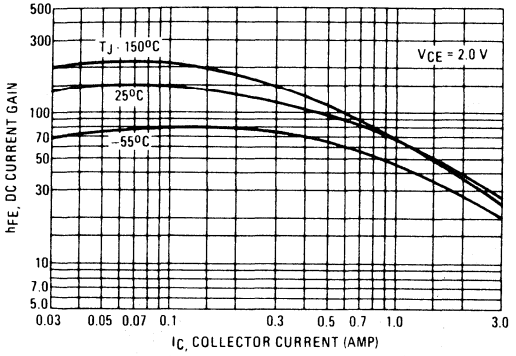


FIGURE 2 – TURN-OFF TIME

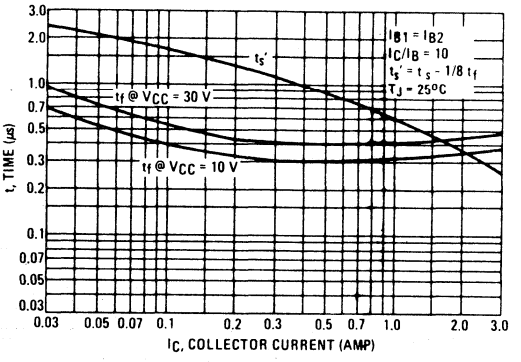


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT

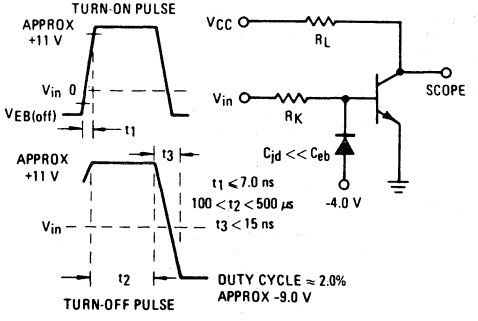


FIGURE 4 – TURN-ON TIME

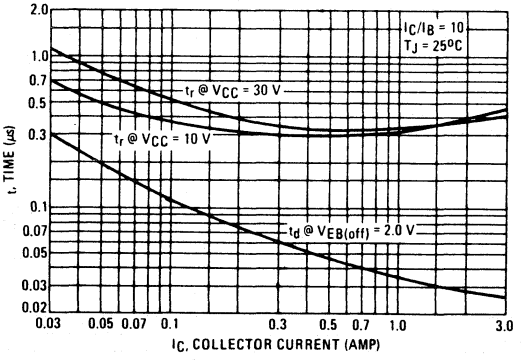
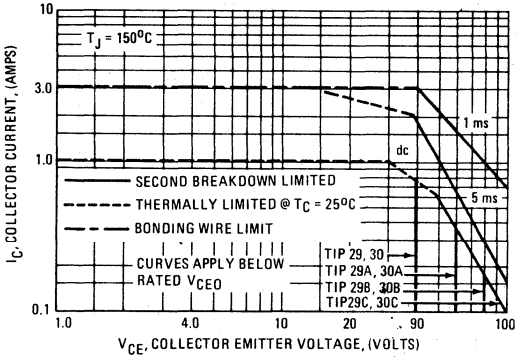


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

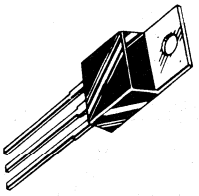
TIP31, 31A, 31B, 31C
TIP32, 32A, 32B, 32C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – TIP31, TIP 32
  = 60 Vdc (Min) – TIP31A, TIP32A
  = 80 Vdc (Min) – TIP31B, TIP32B
  = 100 Vdc (Min) – TIP31C, TIP32C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80-100 VOLTS
40 WATTS



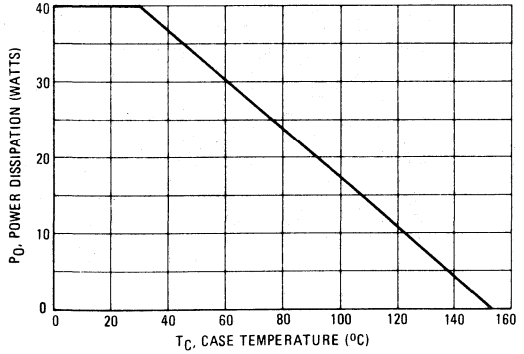
MAXIMUM RATINGS

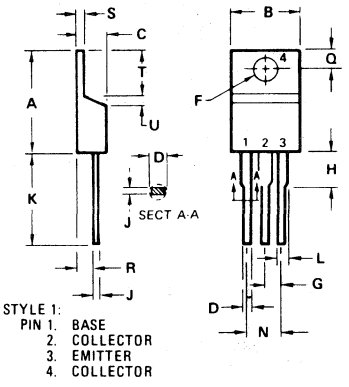
Rating	Symbol	TIP31 TIP32	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	3.0				Adc
Peak		5.0				
Base Current	I_B	1.0				Adc
Total Device Dissipation @ T_C = 25°C	P_D	40				Watts
Derate above 25°C		0.32				W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP31, TIP32	$V_{CEO(sus)}$	40	–	Vdc
	TIP31A, TIP32A		60	–	
	TIP31B, TIP32B		80	–	
	TIP31C, TIP32C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP31, TIP31A, TIP32, TIP32A		–	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C, TIP32B, TIP32C		–	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP31, TIP32		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		–	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			25	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	–	1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

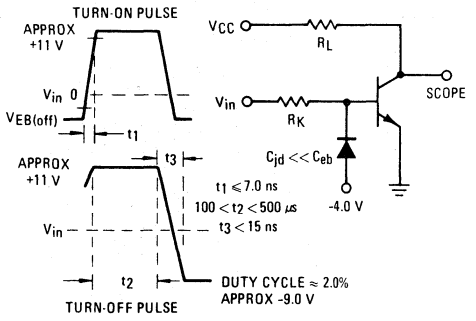


FIGURE 3 – TURN-ON TIME

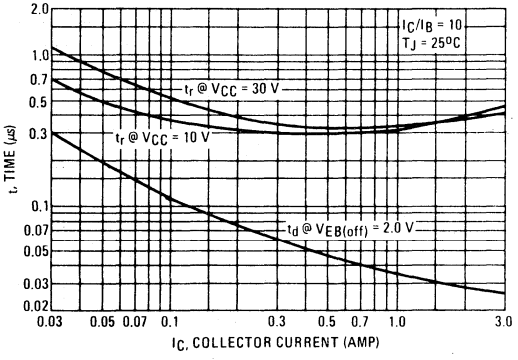


FIGURE 4 – THERMAL RESPONSE

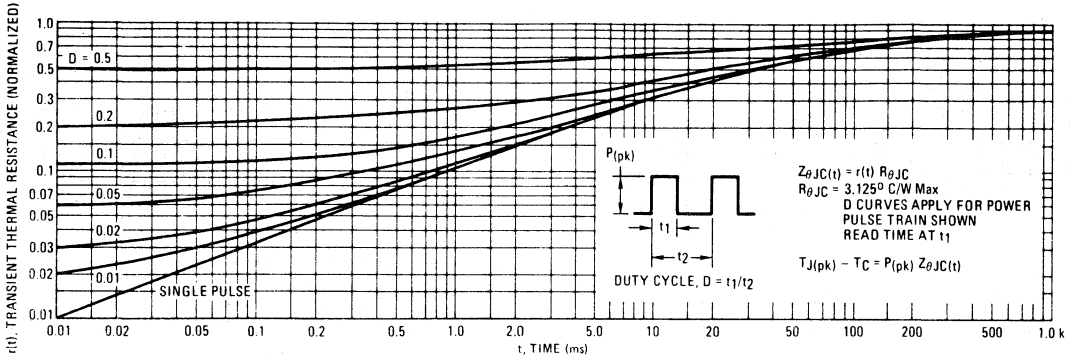
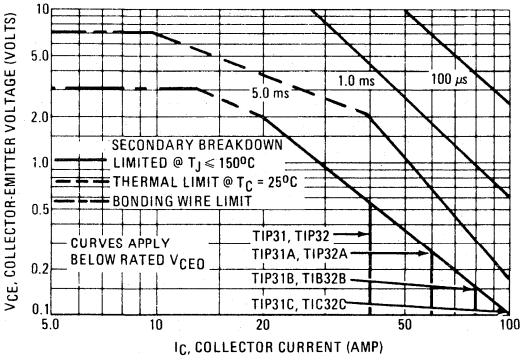


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

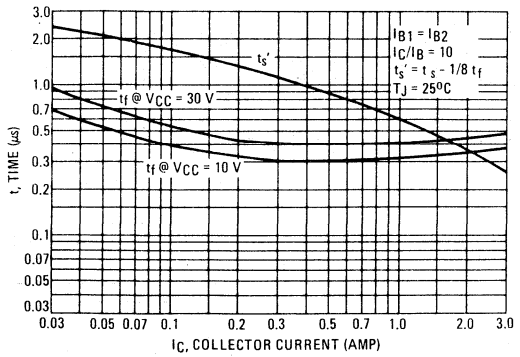


FIGURE 7 – CAPACITANCE

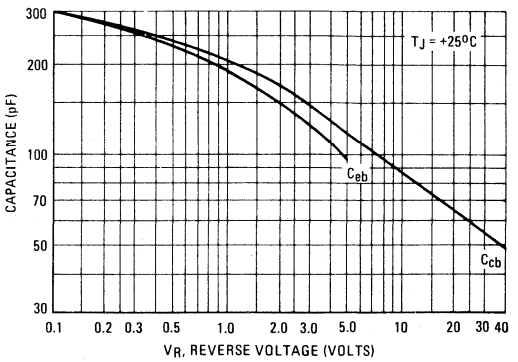


FIGURE 8 – DC CURRENT GAIN

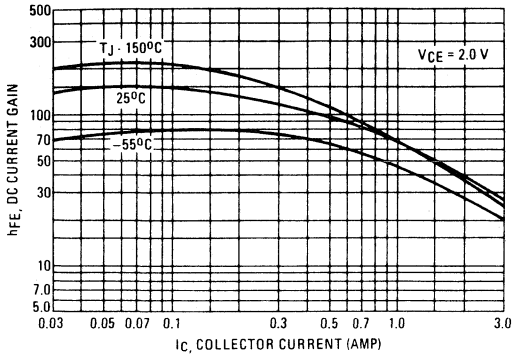


FIGURE 9 – COLLECTOR SATURATION REGION

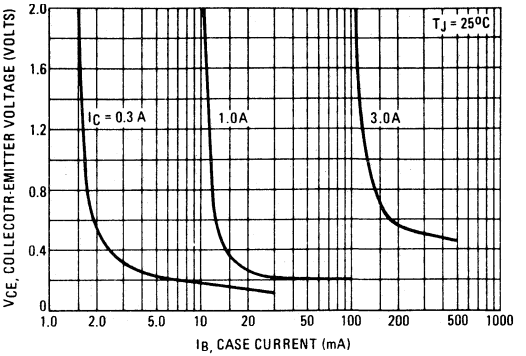


FIGURE 10 – "ON" VOLTAGES

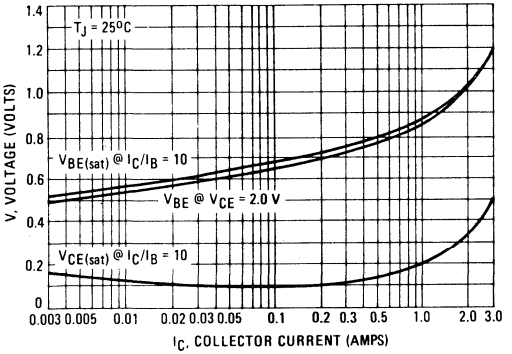


FIGURE 11 – TEMPERATURE COEFFICIENTS

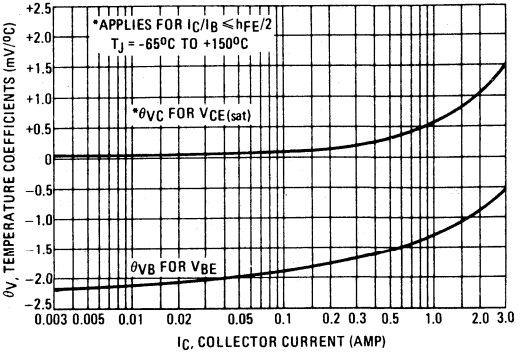


FIGURE 12 – COLLECTOR CUT-OFF REGION

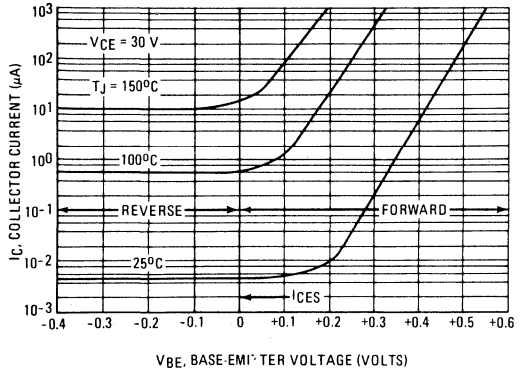
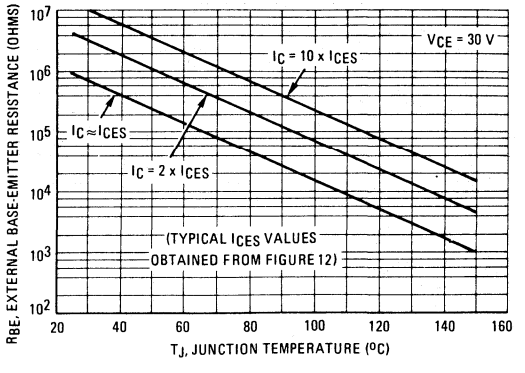


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



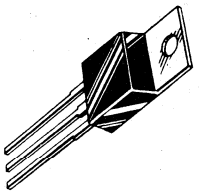
TIP41, 41A, 41B, 41C
TIP42, 42A, 42B, 42C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – TIP41, TIP42
  = 60 Vdc (Min) – TIP41A, TIP42A
  = 80 Vdc (Min) – TIP41B, TIP42B
  = 100 Vdc (Min) – TIP41C, TIP42C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80-100 VOLTS
65 WATTS



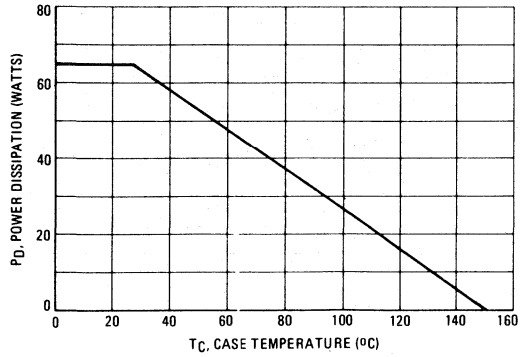
***MAXIMUM RATINGS**

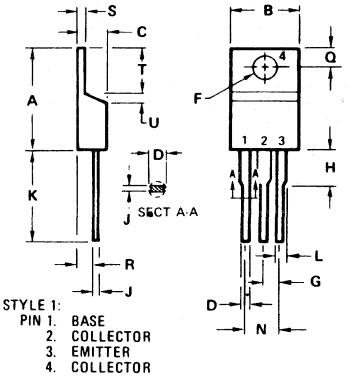
Rating	Symbol	TIP41 TIP42	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	6				Adc
Peak		10				
Base Current	I_B	2.0				Adc
Total Device Dissipation @ T_C = 25°C	P_D	65				Watts
Derate above 25°C		0.52				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

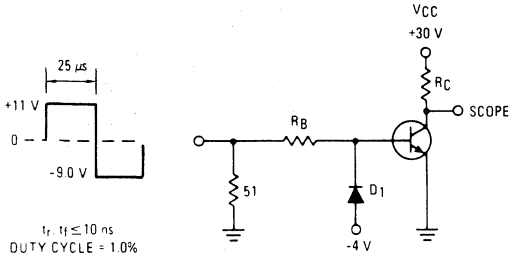
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41, TIP42	$V_{CEO(sus)}$	40	–	Vdc
	TIP41A, TIP42A		60	–	
	TIP41B, TIP42B		80	–	
	TIP41C, TIP42C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A		–	0.7	
(V_{CE} = 60 Vdc, I_B = 0)	TIP41B, TIP41C, TIP42B, TIP42C		–	0.7	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP41, TIP42		–	400	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP41A, TIP42A		–	400	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP41B, TIP42B		–	400	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41C, TIP42C		–	400	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)			30	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = h_{fe} \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FIGURE 3 – TURN-ON TIME

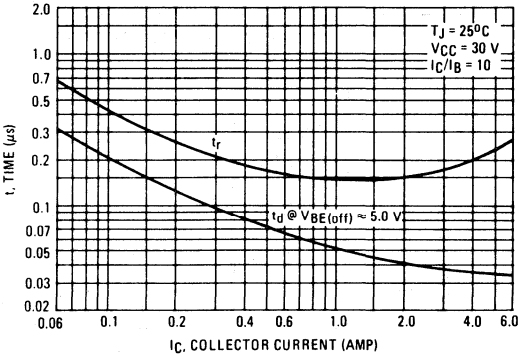


FIGURE 4 – THERMAL RESPONSE

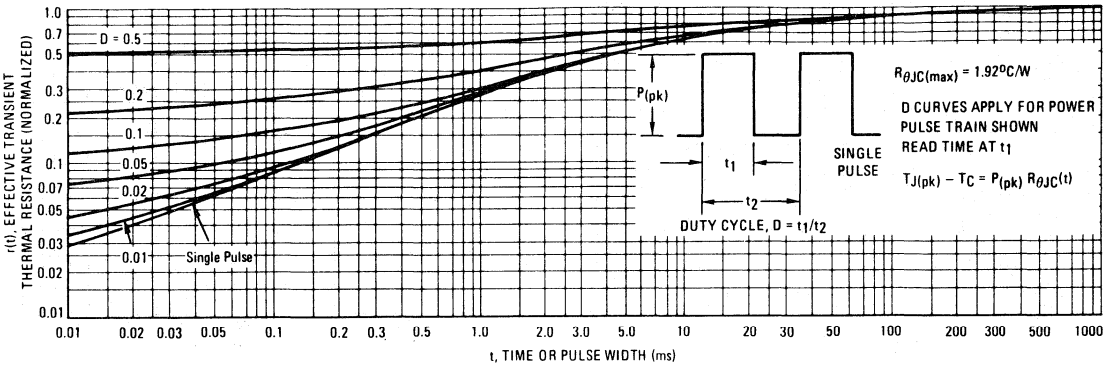
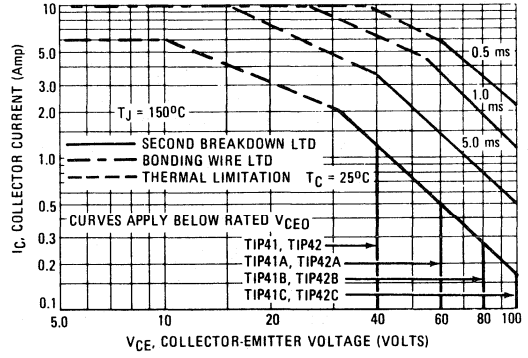


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

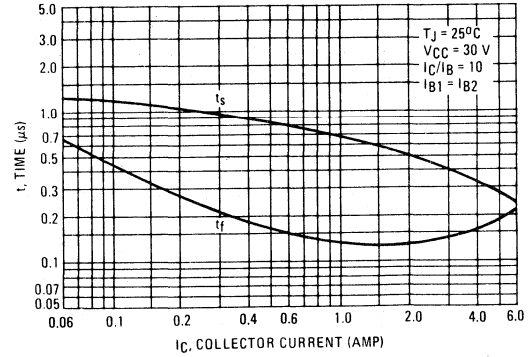


FIGURE 7 – CAPACITANCE

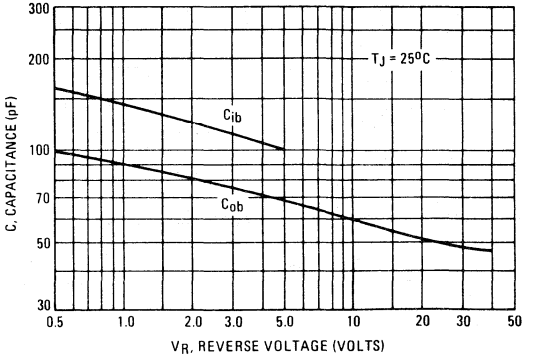


FIGURE 8 – DC CURRENT GAIN

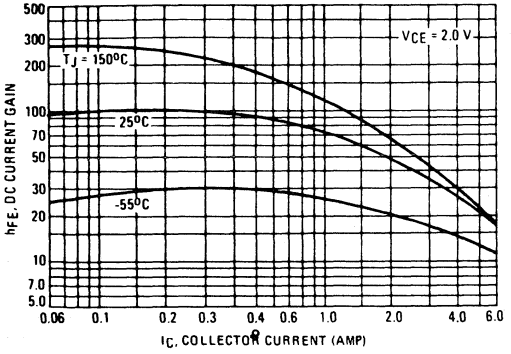


FIGURE 9 – COLLECTOR SATURATION REGION

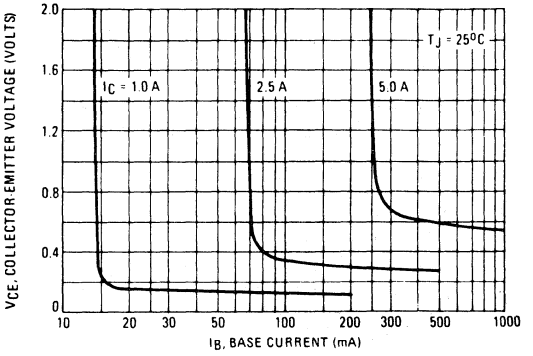


FIGURE 10 – "ON" VOLTAGES

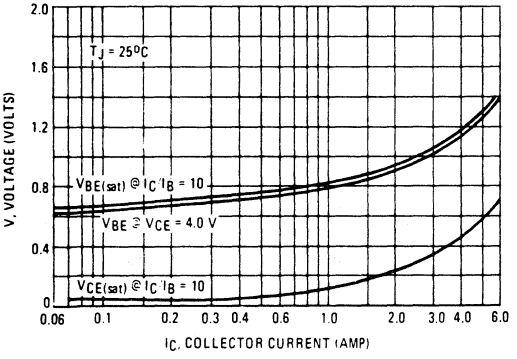


FIGURE 11 – TEMPERATURE COEFFICIENTS

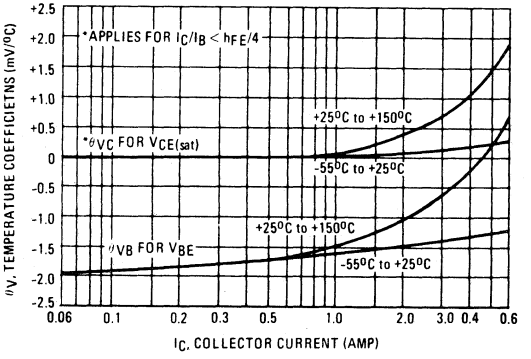


FIGURE 12 – COLLECTOR CUT-OFF REGION

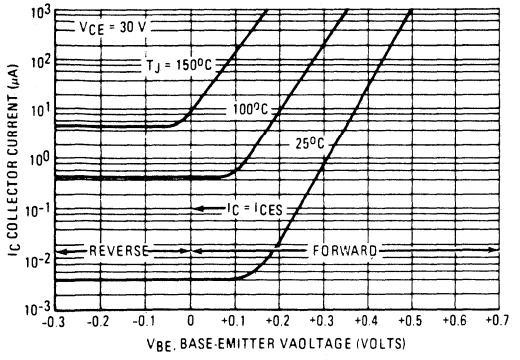
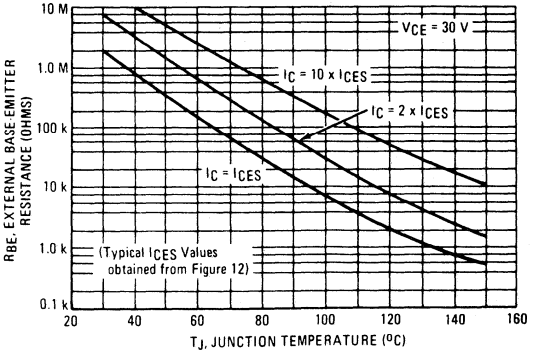


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



TIP47 • TIP48
TIP49 • TIP50

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

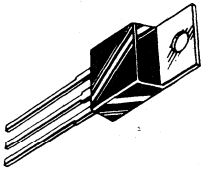
. . . designed for line operated audio output amplifier, Switchmode[1] power supply drivers and other switching applications.

- 250 V to 400 V (Min) – $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS
NPN SILICON

250-300-350-400 VOLTS
40 WATTS



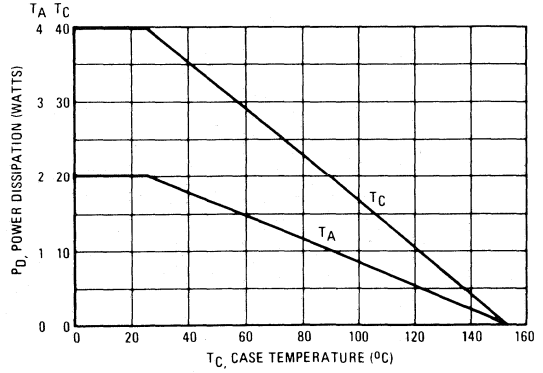
MAXIMUM RATINGS

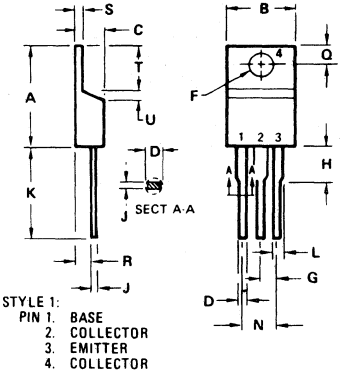
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	◄ 5.0 ►				Vdc
Collector Current – Continuous Peak	I_C	◄ 1.0 ► ◄ 2.0 ►				Adc
Base Current	I_B	◄ 0.6 ►				Adc
Total Device Dissipation @ T_C = 25° C Derate above 25° C	P_D	◄ 40 ► ◄ 0.32 ►				Watts W/°C
Total Device Dissipation @ T_A = 25° C Derate above 25° C	P_D	◄ 40 ► ◄ 0.016 ►				Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	◄ 20 ►				mJ
Operating and Storage Junction Temperature Range	T_J,T_{stg}	◄ -65 to +150 ►				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

[1] Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP47	$V_{CEO(sus)}$	250	–	Vdc
	TIP48		300	–	
	TIP49		350	–	
	TIP50		400	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	TIP47		–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	TIP48		–	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	TIP49		–	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	TIP50		–	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	TIP47		–	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	TIP48		–	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	TIP49		–	1.0	
(V_{CE} = 500 Vdc, V_{BE} = 0)	TIP50		–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 mAdc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

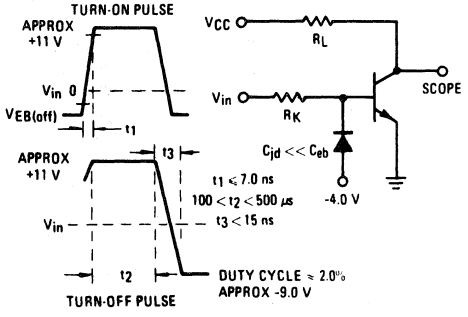


FIGURE 3 – TURN-ON TIME

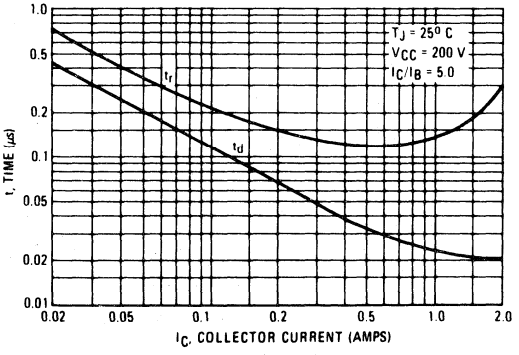


FIGURE 4 – THERMAL RESPONSE

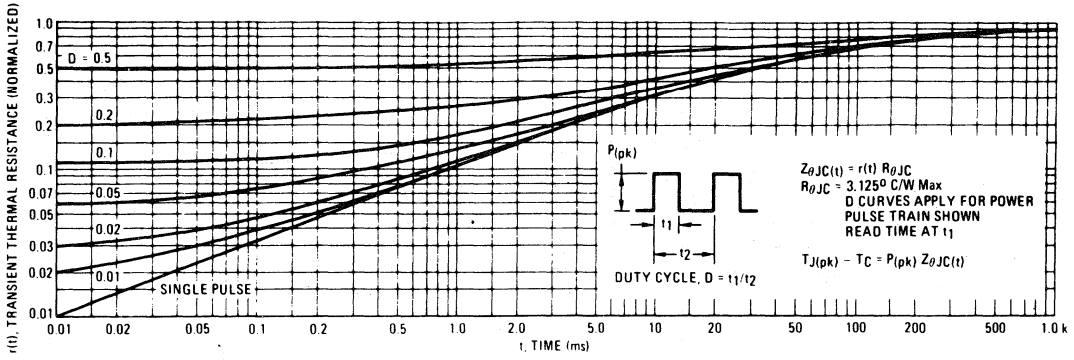
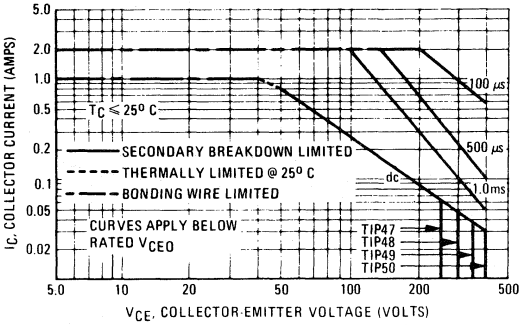


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

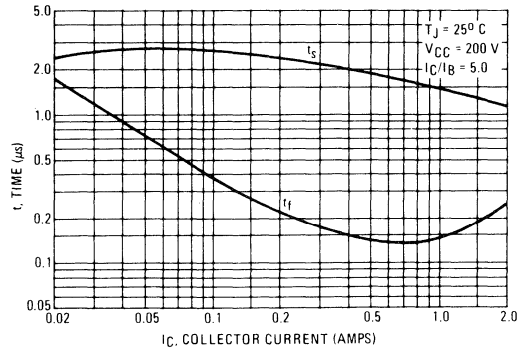


FIGURE 7 – TEMPERATURE COEFFICIENTS

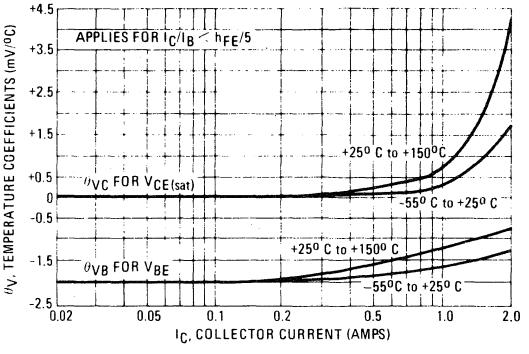
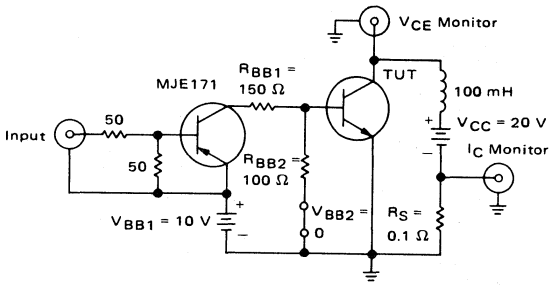


FIGURE 8 – INDUCTIVE LOAD SWITCHING

Test Circuit



Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Voltage and Current Waveforms

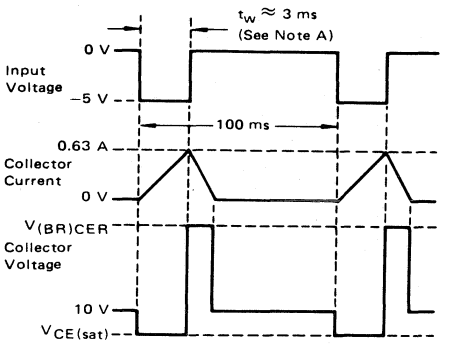


FIGURE 9 – DC CURRENT GAIN

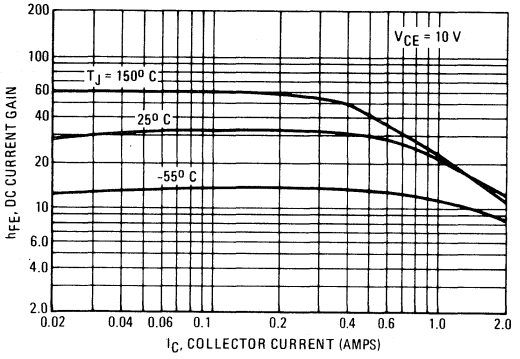
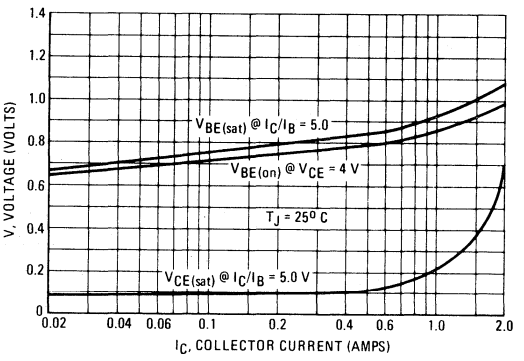


FIGURE 10 – "ON" VOLTAGES



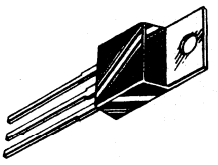
TIP110, TIP111, TIP112 (NPN)
TIP115, TIP116, TIP117 (PNP)

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage – @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP110, TIP115
  = 80 Vdc (Min) – TIP111, TIP116
  = 100 Vdc (Min) – TIP112, TIP117
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 2.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
50 WATTS



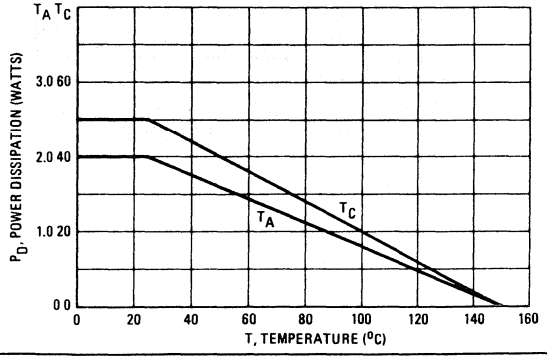
MAXIMUM RATINGS

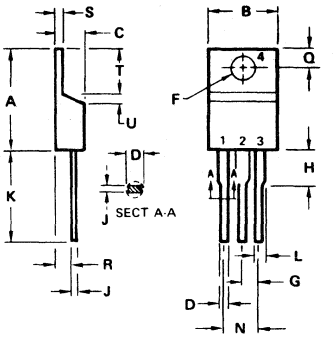
Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	2.0 4.0			Adc
Base Current	I_B	50			mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4			Watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy – Figure 13	E	25			mJ
Operating and Storage Junction,	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	–	
	TIP111, TIP116		80	–	
	TIP112, TIP117		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		–	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112, TIP117		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		–	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		–	1.0	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	–	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			–	2.8	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$			–
(I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			25	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		–	200	
	TIP110, TIP111, TIP112		–	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

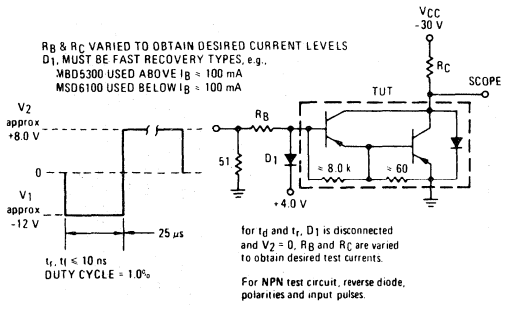


FIGURE 3 – SWITCHING TIMES

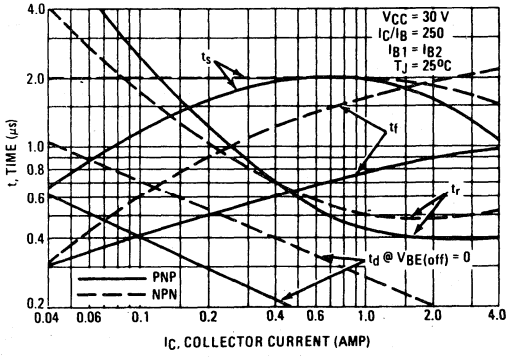
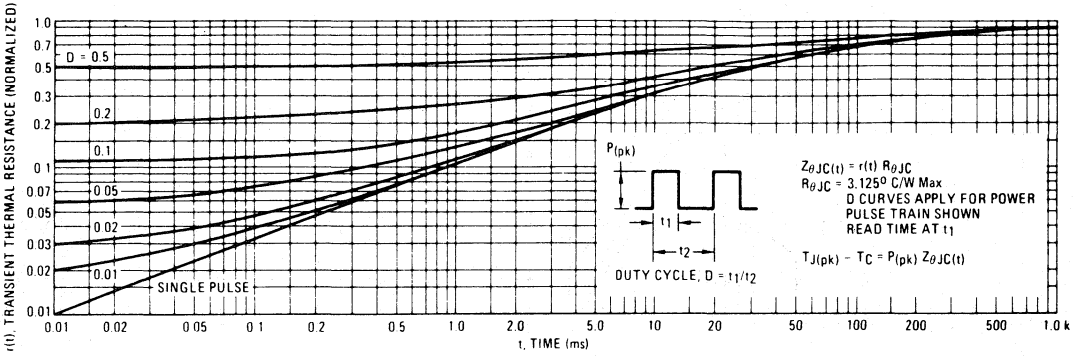


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – TIP115, 116, 117

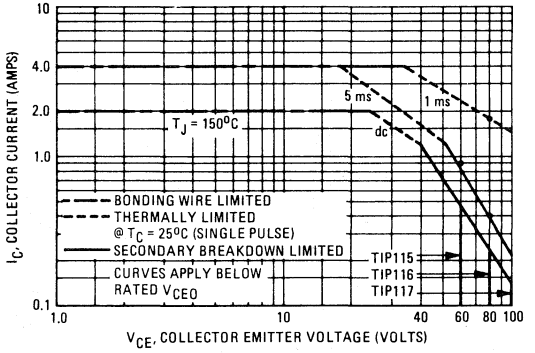
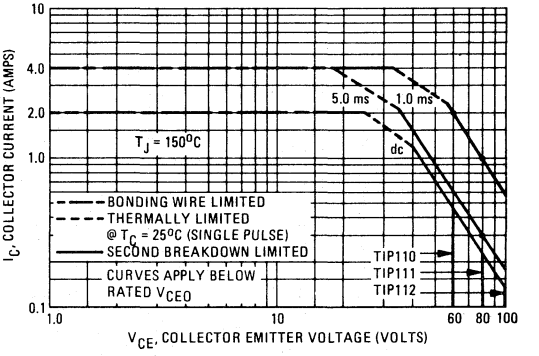


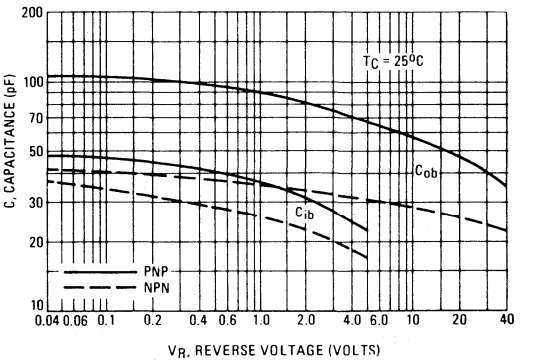
FIGURE 6 – TIP110, 111, 112



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

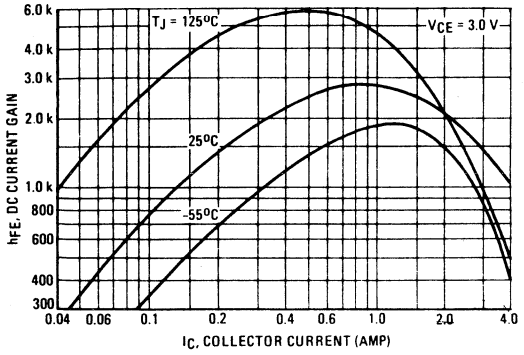
FIGURE 7 – CAPACITANCE



NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

FIGURE 8 – DC CURRENT GAIN



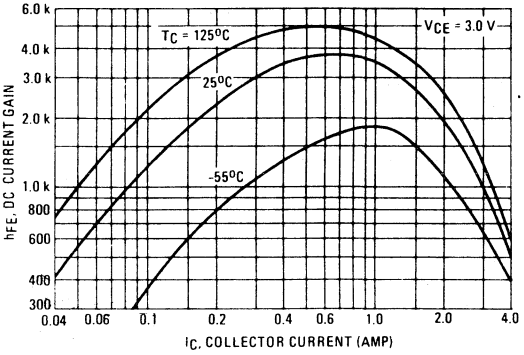
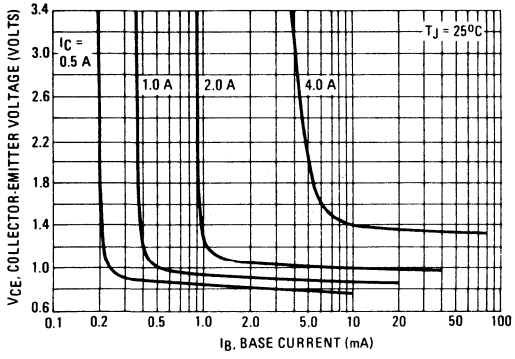


FIGURE 9 – COLLECTOR SATURATION REGION



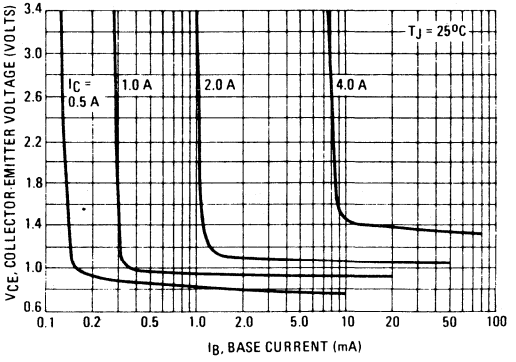
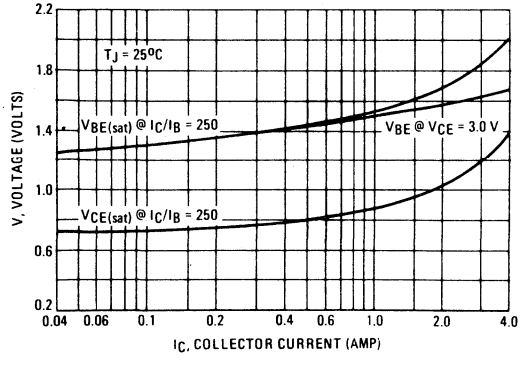
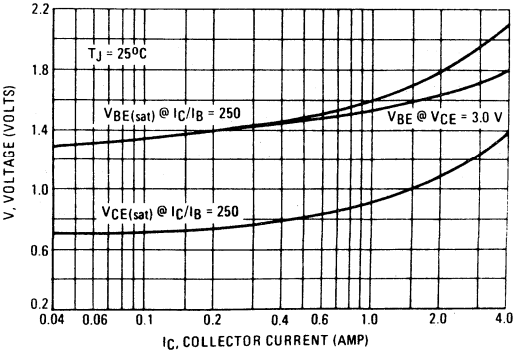


FIGURE 10 – "ON" VOLTAGES

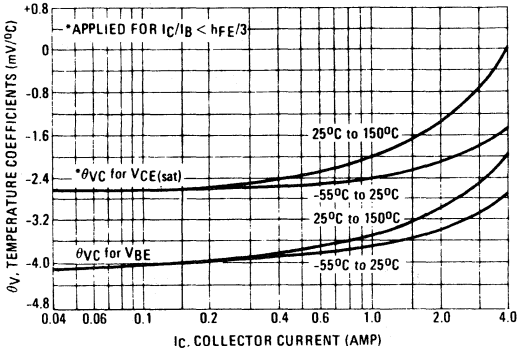




NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

FIGURE 11 – TEMPERATURE COEFFICIENTS



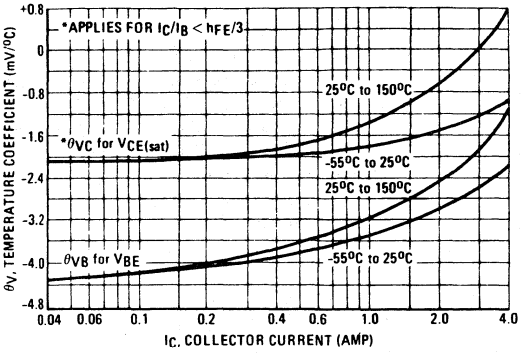
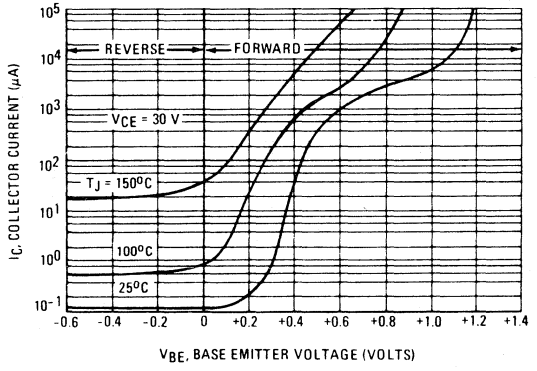


FIGURE 12 – COLLECTOR CUT-OFF REGION



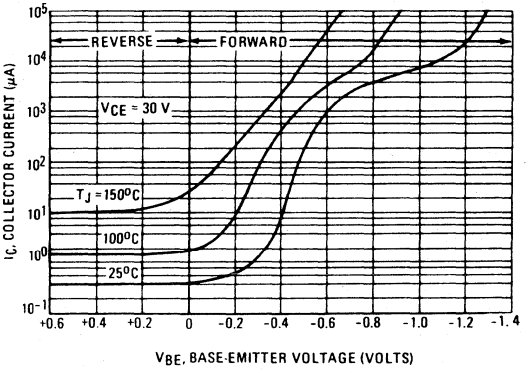
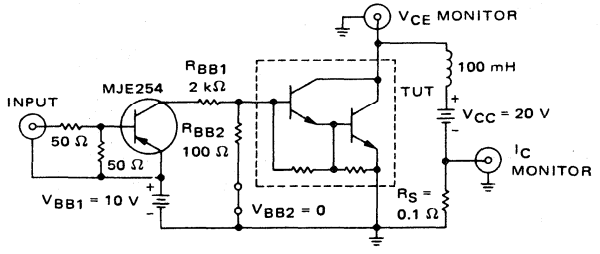
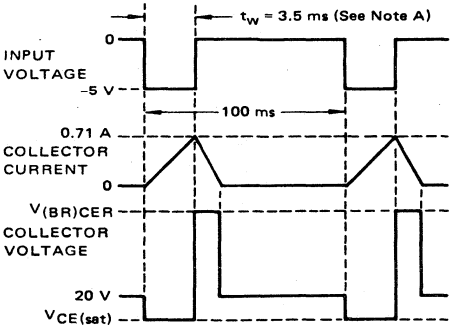


FIGURE 13 – INDUCTIVE LOAD SWITCHING

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTE A: Input pulse width is increased until I_{CM} = 0.71 A, NPN test shown; for PNP test reverse all polarity and use MJE224 driver.

TIP120, TIP121, TIP122 (NPN)
TIP125, TIP126, TIP127 (PNP)

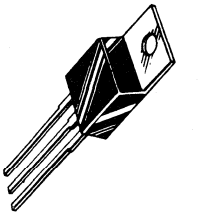
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP120, TIP125
  = 80 Vdc (Min) – TIP121, TIP126
  = 100 Vdc (Min) – TIP122, TIP127
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
65 WATTS



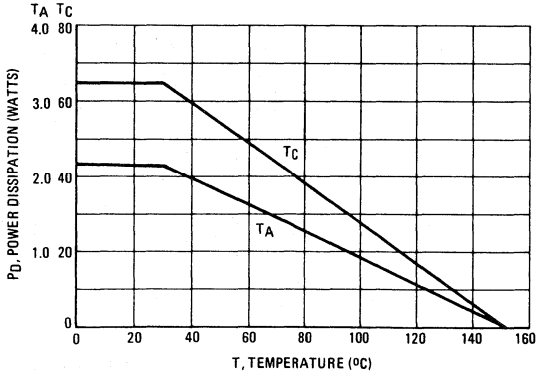
***MAXIMUM RATINGS**

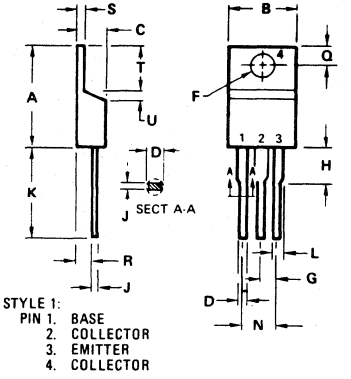
Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	8.0			Adc
Peak		16			
Base Current	I_B	120			mAdc
Total Device Dissipation @T_C = 25°C	P_D	65			Watts
Derate above 25°C		0.52			W/°C
Total Device Dissipation @T_A = 25°C	P_D	2.2			Watts
Derate above 25°C		0.0175			W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	57	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	–	
	TIP121, TIP126		80	–	
	TIP122, TIP127		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		–	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		–	0.2	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)			4.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP125, TIP126, TIP127		–	300	
	TIP120, TIP121, TIP122		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

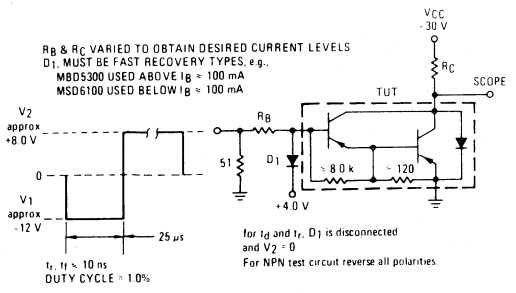


FIGURE 3 – SWITCHING TIMES

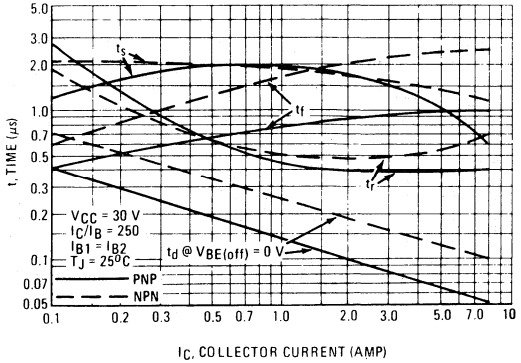


FIGURE 4 – THERMAL RESPONSE

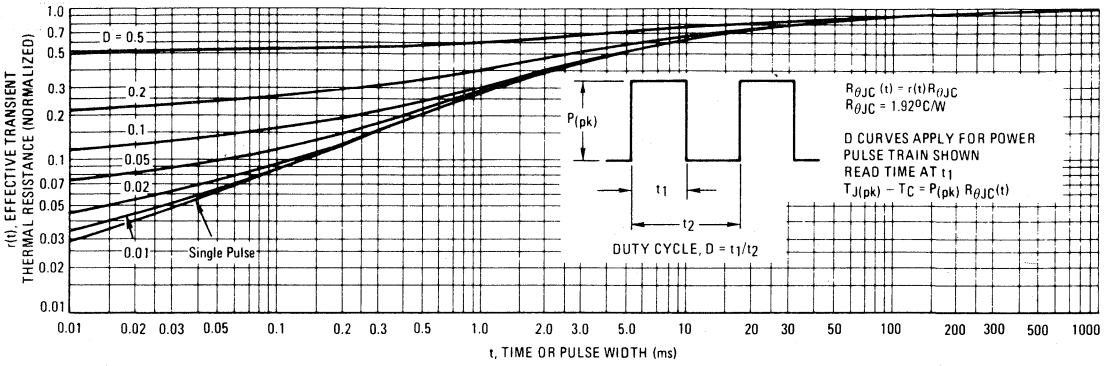
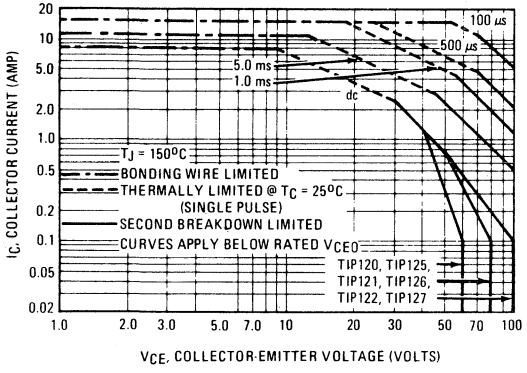


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

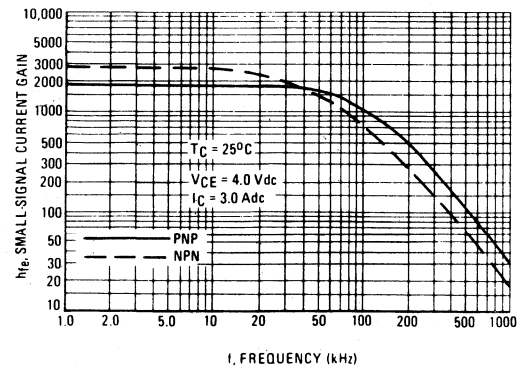
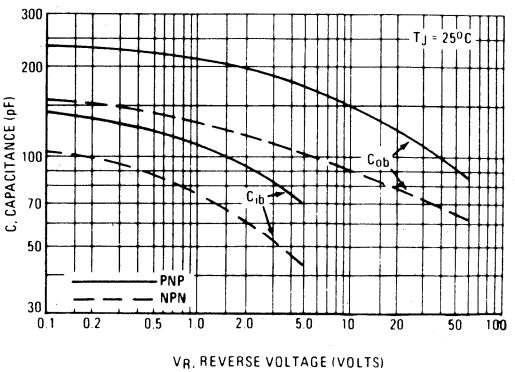


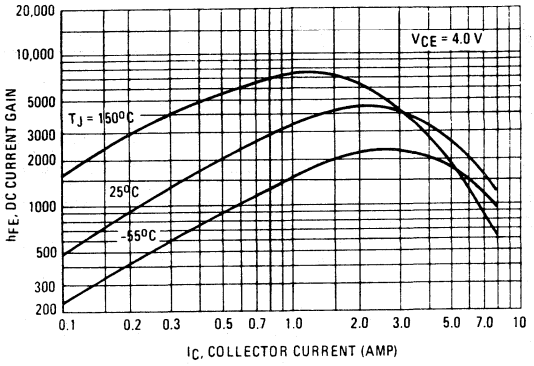
FIGURE 7 – CAPACITANCE



NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 8 – DC CURRENT GAIN



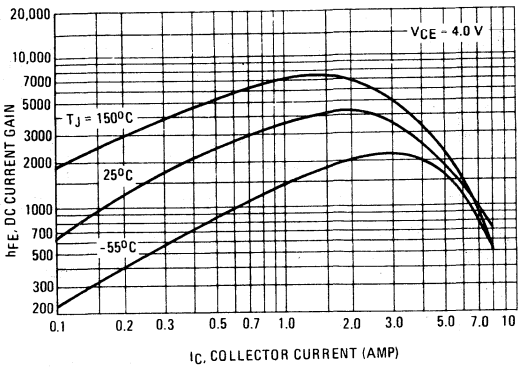
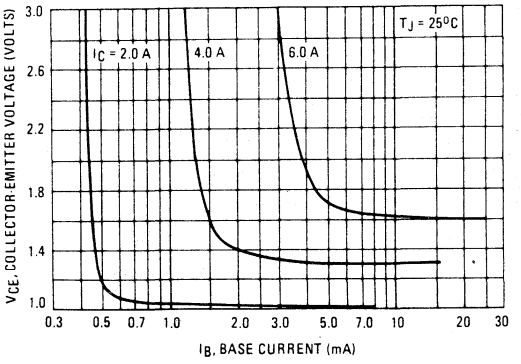


FIGURE 9 – COLLECTOR SATURATION REGION



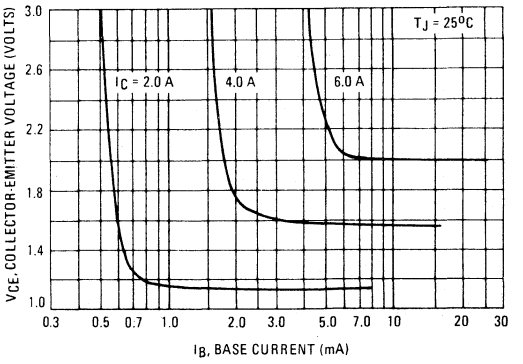
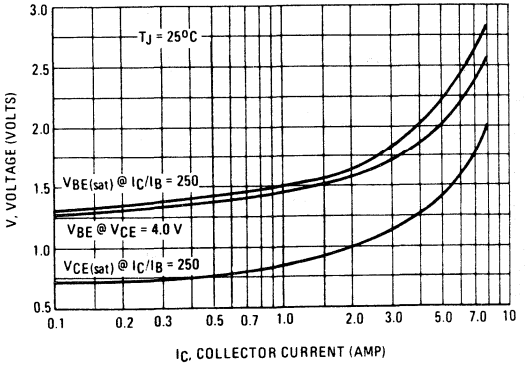
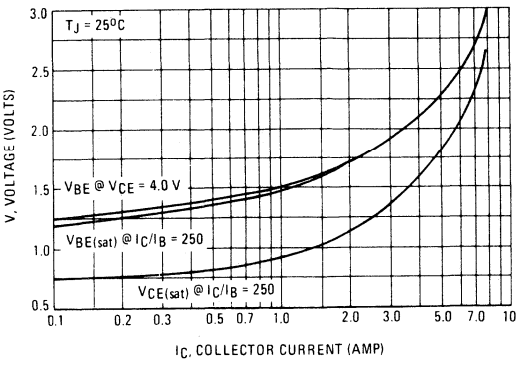


FIGURE 10 – "ON" VOLTAGES

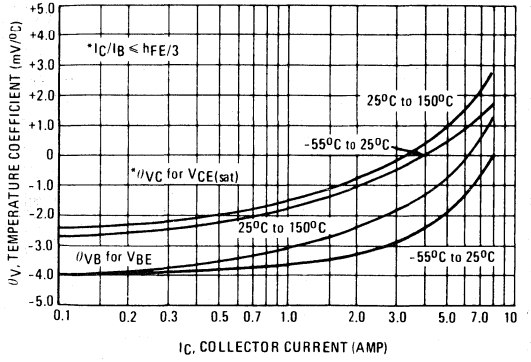




NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 11 – TEMPERATURE COEFFICIENTS



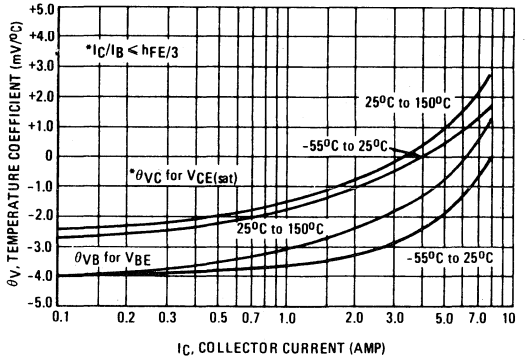
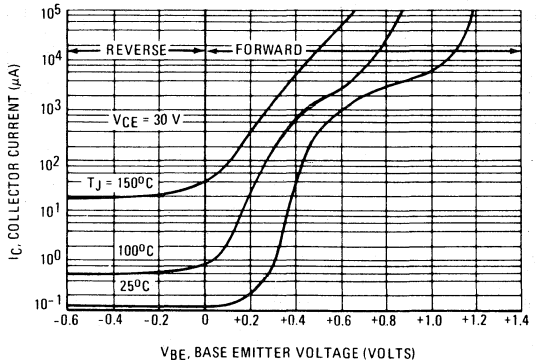


FIGURE 12 – COLLECTOR CUT-OFF REGION



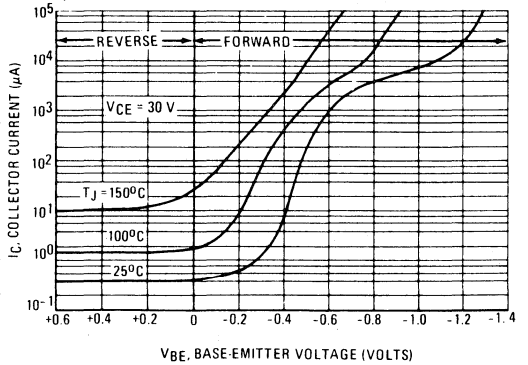
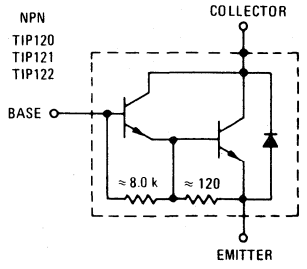
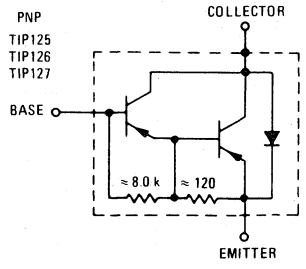


FIGURE 13 – DARLINGTON SCHEMATIC





HIGH-POWER NPN SILICON POWER TRANSISTOR

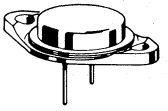
. . . EIP-BASE▲ power transistor designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- Current-Gain – Bandwidth Product – f_T = 2.5 MHz (Min) @ I_C = 1 Adc
- Safe Operating Area – Full Power Rating to 40 V

15 AMPERE

POWER TRANSISTOR NPN SILICON

60 VOLTS
115 WATTS



*MAXIMUM RATINGS

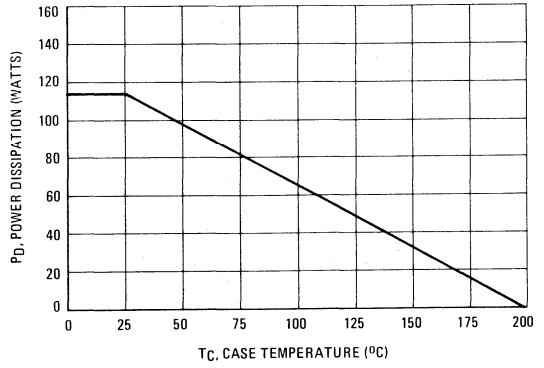
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CEX}	90	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

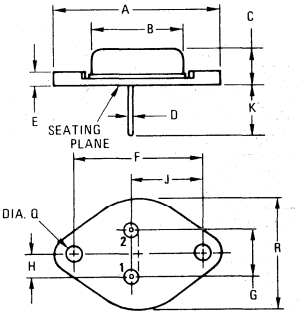
*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

▲Trademark of Motorola Inc.

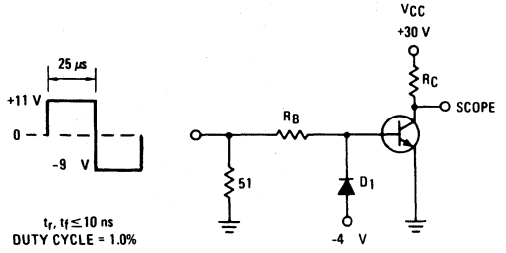
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
* Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	70	–	Vdc
* Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	5 30	mAdc
* Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
* DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	70 –	–
Collector-Emitter Saturation Voltage * (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
Second Breakdown Collector Current With Base Forward-Biased	$I_{S/b}$	(See Figure 4)		Adc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 1 Adc, V_{CE} = 4 Vdc, f_{test} = 1 MHz)	f_T	2.5	–	MHz
*Small Signal Current Gain Cutoff Frequency (I_C = 1 Adc, V_{CE} = 4 Vdc)	f_{hfe}	10	–	kHz
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	15	120	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FIGURE 3 – TURN-ON TIME

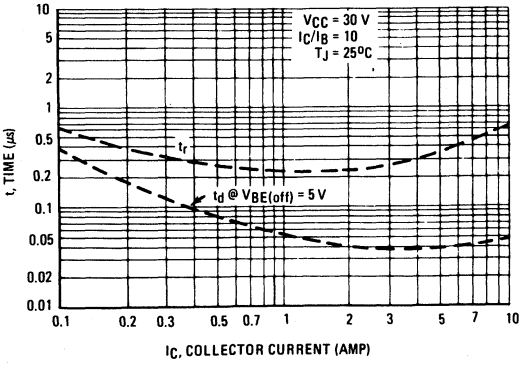
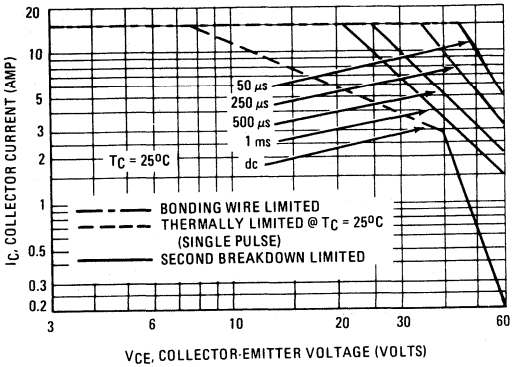


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A.)

FIGURE 5 – COLLECTOR CUT-OFF REGION

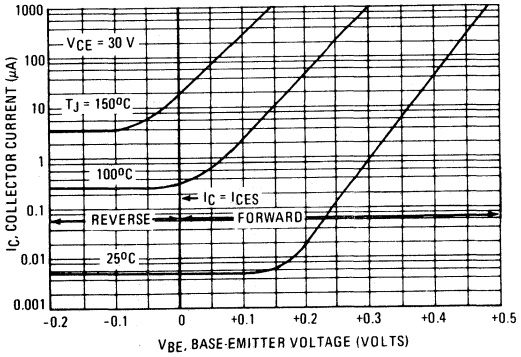


FIGURE 6 – TURN-OFF TIME

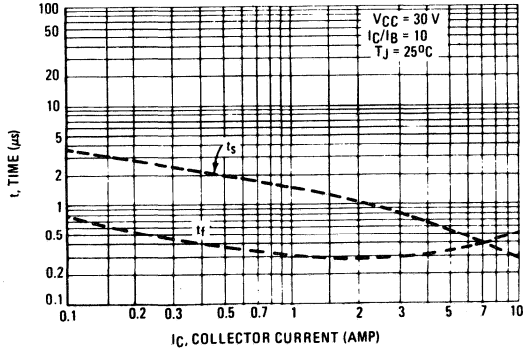


FIGURE 7 – CAPACITANCE

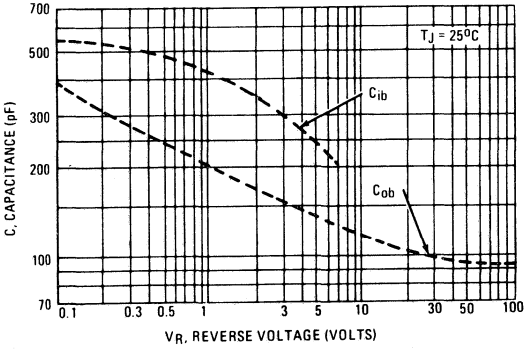


FIGURE 8 – DC CURRENT GAIN

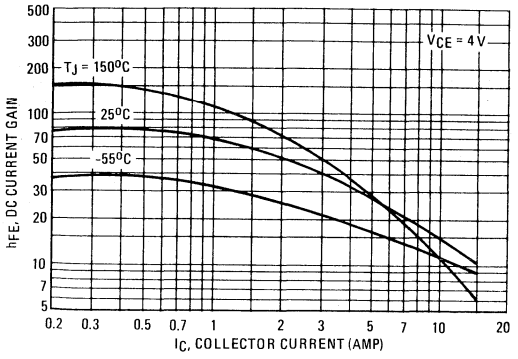


FIGURE 9 – COLLECTOR SATURATION REGION

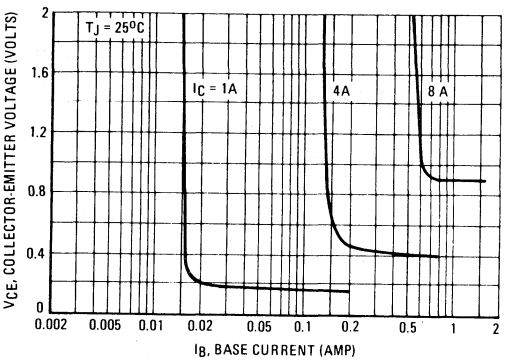
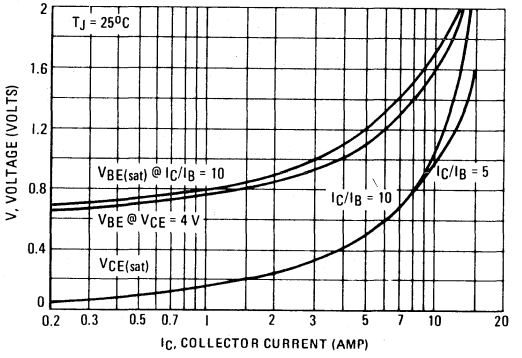


FIGURE 10 – "ON" VOLTAGES



2N3773 (NPN)
2N6609 (PNP)

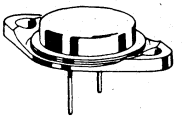
COMPLEMENTARY SILICON POWER TRANSISTORS

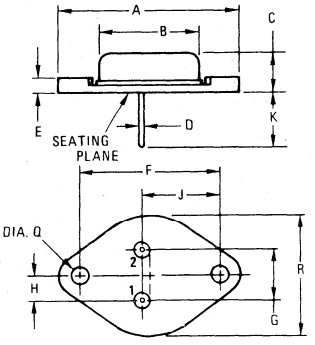
The 2N3773 and 2N6609 are EPI-BASE▲ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
  150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{fe} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE
COMPLEMENTARY
POWER TRANSISTORS

140 VOLTS
150 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	–	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	–	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	–	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	15 5	60	–
Collector-Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	– –	1.4 4	Vdc
*Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	–	–
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	–	–
SWITCHING CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	–	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

NPN

FIGURE 1 – DC CURRENT GAIN

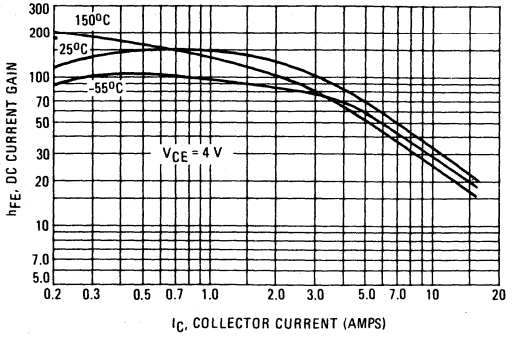


FIGURE 3 – COLLECTOR SATURATION REGION

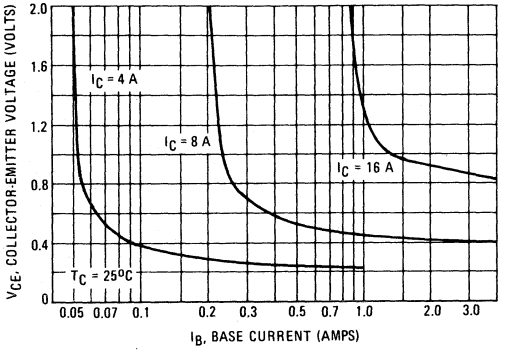
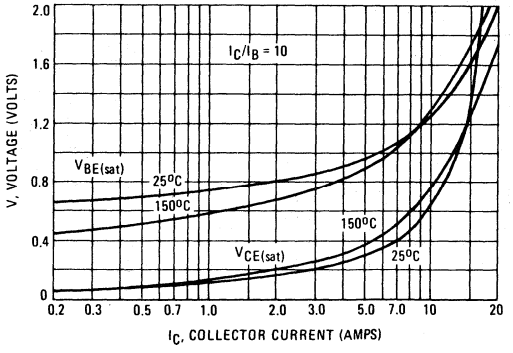


FIGURE 5 – "ON" VOLTAGE



PNP

FIGURE 2 – DC CURRENT GAIN

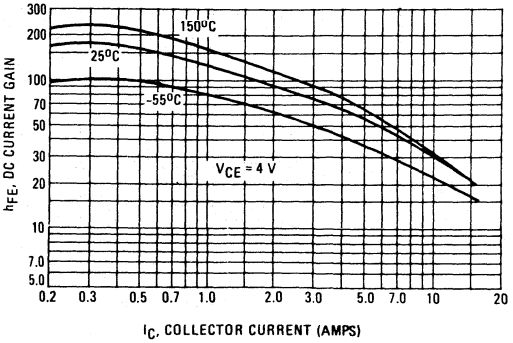


FIGURE 4 – COLLECTOR SATURATION REGION

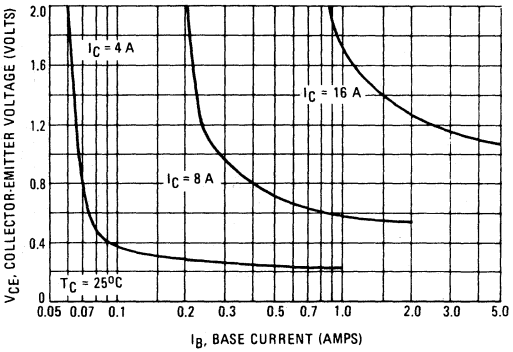


FIGURE 6 – "ON" VOLTAGE

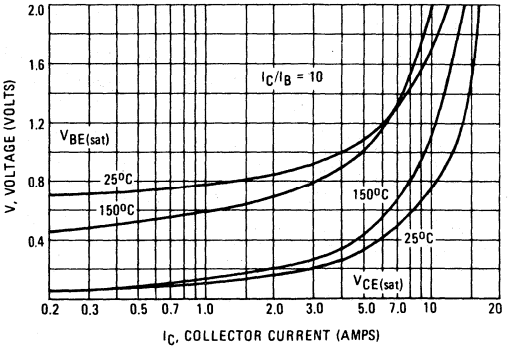


FIGURE 7 – TURN-ON SWITCHING TIMES – 2N3773, 2N6609

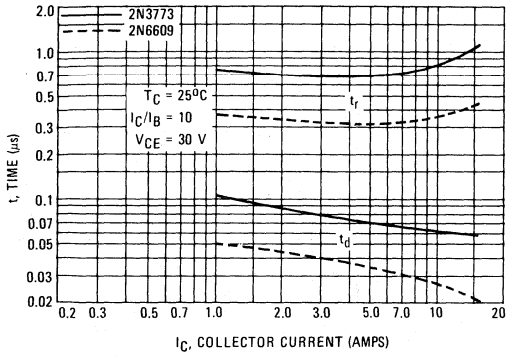


FIGURE 8 – TURN-OFF SWITCHING TIMES – 2N3773, 2N6609

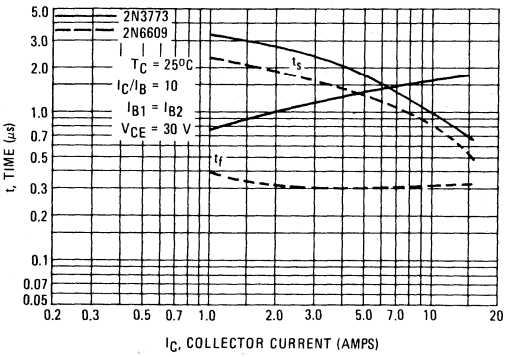


FIGURE 9 – CURRENT-GAIN – BANDWIDTH PRODUCT – 2N3773, 2N6609

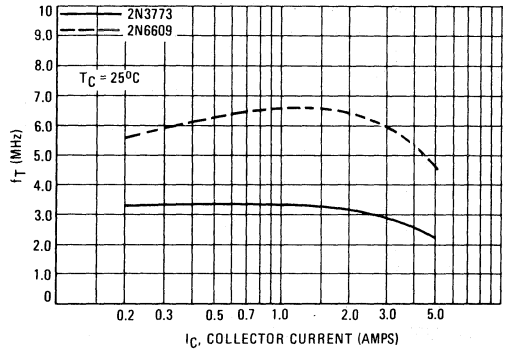


FIGURE 10 – CAPACITANCES – 2N3773, 2N6609

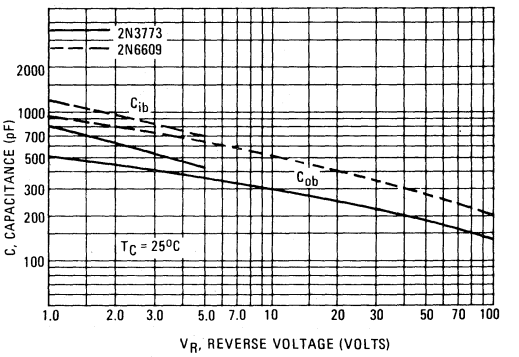


FIGURE 11 – THERMAL RESPONSE – 2N3773, 2N6609

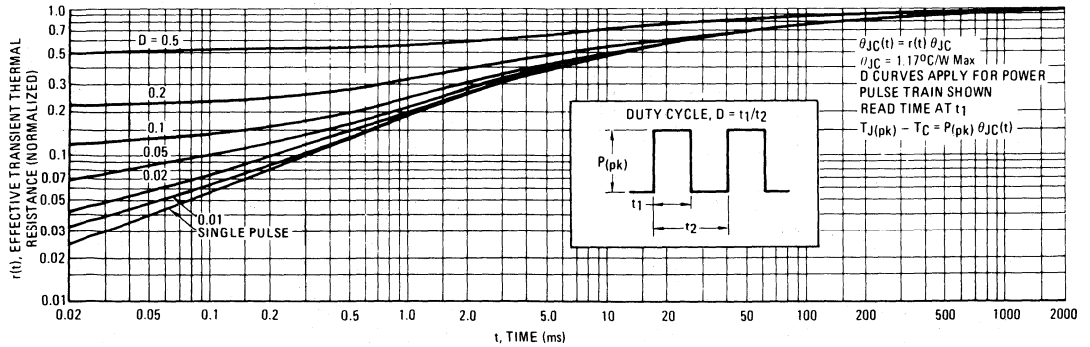
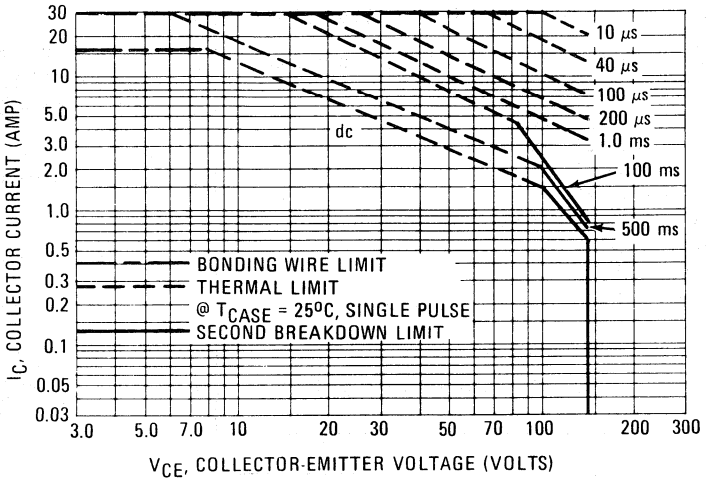


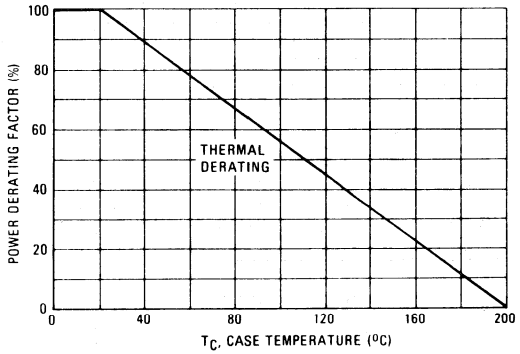
FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 13 – POWER DERATING



2N5629
2N5630 • 2N5631

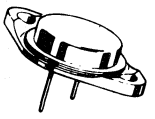
HIGH-VOLTAGE – HIGH POWER NPN TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N5629
  = 120 Vdc – 2N5630
  = 140 Vdc – 2N5631
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N5629
  = 20 (Min) – 2N5630
  = 15 (Min) – 2N5631
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Complement to PNP Transistor Series 2N6029, 2N6030, 2N6031

16 AMPERE
POWER TRANSISTORS
NPN SILICON

100-120-140 VOLTS
200 WATTS



*MAXIMUM RATINGS

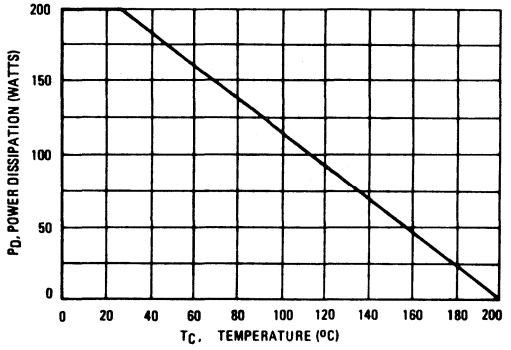
Rating	Symbol	2N5629	2N5630	2N5631	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 16 → ← 20 →			Adc
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

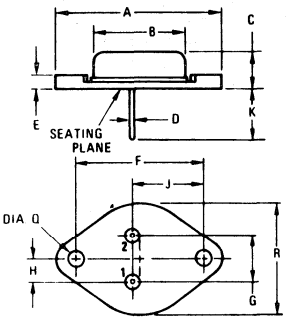
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

Collector connected to case

CASE 11 (TO-3)

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

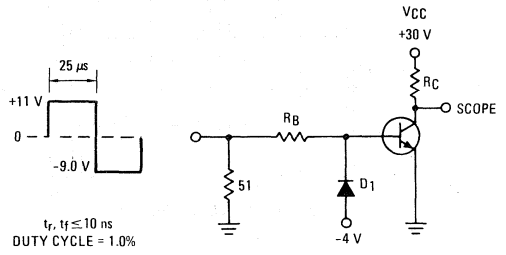
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5629	$V_{CEO(sus)}$	100	–	Vdc
	2N5630		120	–	
	2N5631		140	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N5629		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5630		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N5631		–	1.0	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	2N5629		25	100	
	2N5630		20	80	
	2N5631		15	60	
(I_C = 16 Adc, V_{CE} = 2.0 Vdc)	All Types		4.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	All Types		–	1.0	
(I_C = 16 Adc, I_B = 4.0 Adc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	500	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

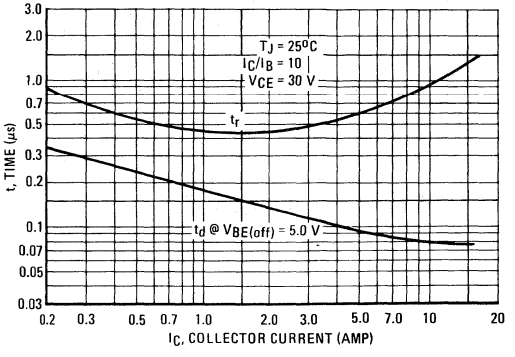


FIGURE 4 – THERMAL RESPONSE

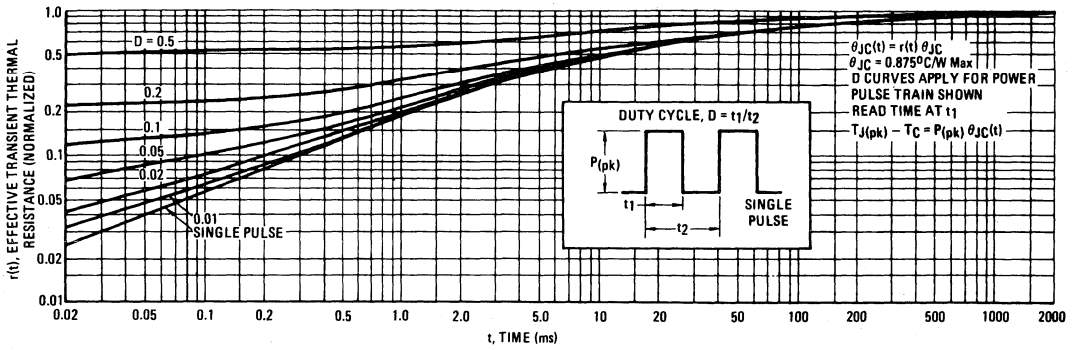
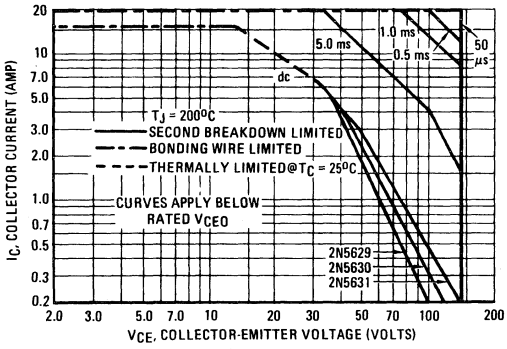


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

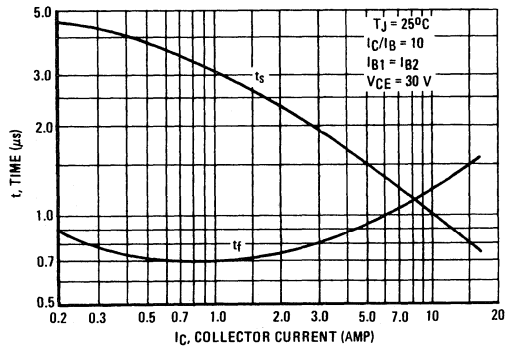


FIGURE 7 – CAPACITANCE

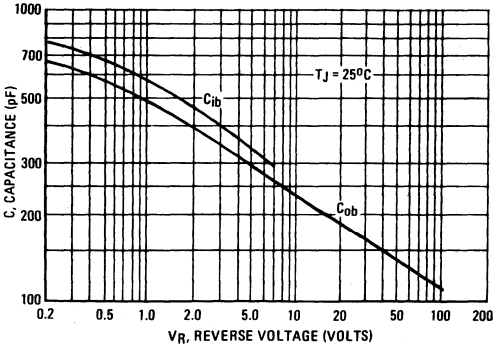


FIGURE 8 – DC CURRENT GAIN

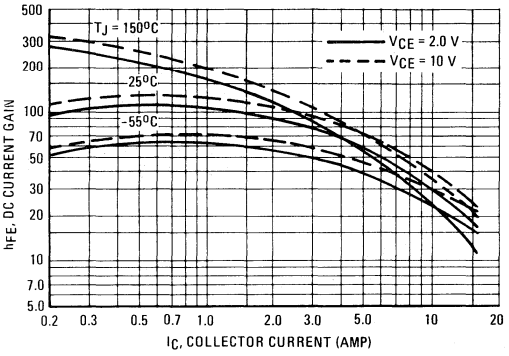


FIGURE 9 – COLLECTOR SATURATION REGION

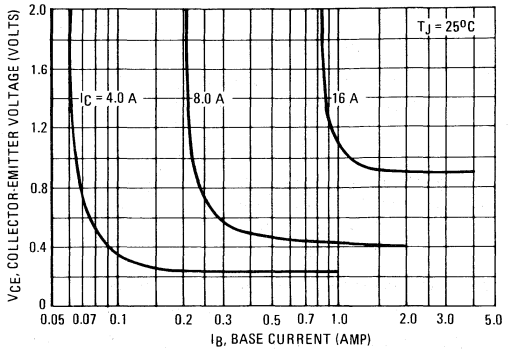


FIGURE 10 – ON VOLTAGES

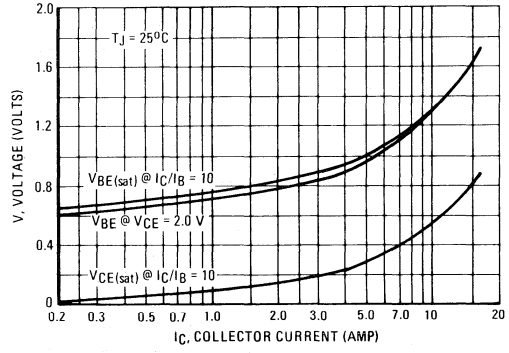


FIGURE 11 – TEMPERATURE COEFFICIENTS

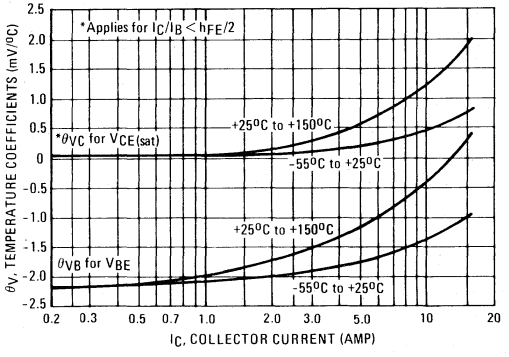


FIGURE 12 – COLLECTOR CUTOFF REGION

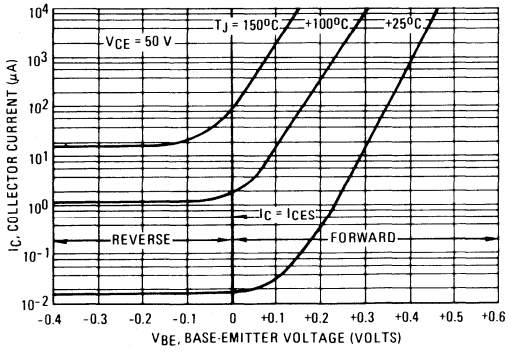
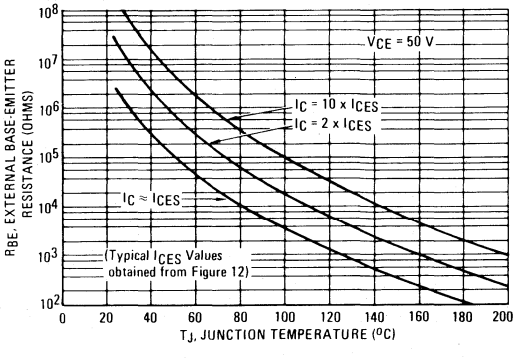


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6029
2N6030 • 2N6031

HIGH-VOLTAGE – HIGH POWER PNP TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N6029
  = 120 Vdc – 2N6030
  = 140 Vdc – 2N6031
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N6029
  = 20 (Min) – 2N6030
  = 15 (Min) – 2N6031
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Complement to NPN Transistor Series – 2N5629, 2N5630, 2N5631

16 AMPERE
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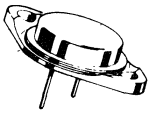
100-120-140 VOLTS
200 WATTS



*MAXIMUM RATINGS

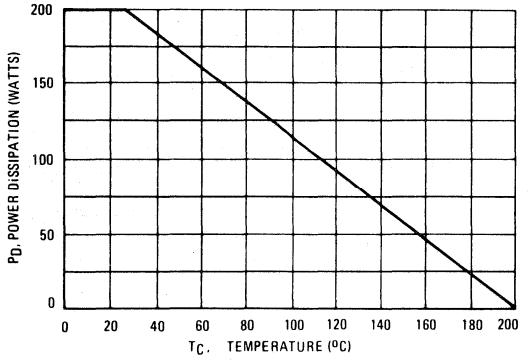
Rating	Symbol	2N6029	2N6030	2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous	I_C	← 16 →			Adc
Peak		← 20 →			
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 200 →			Watts
Derate above 25°C		← 1.14 →			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

*THERMAL CHARACTERISTICS

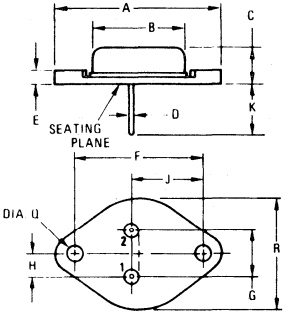
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37	–	1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

Collector connected to case

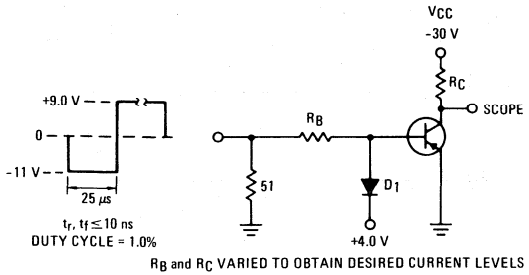
CASE 11 (TO-3)

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6029	$V_{CEO(sus)}$	100	–	Vdc
	2N6030		120	–	
	2N6031		140	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6029		–	2.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6030		–	2.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N6031		–	2.0	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	2.0	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	7.0	
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	2.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	2N6029		25	100	
	2N6030		20	80	
	2N6031		15	60	
(I_C = 16 Adc, V_{CE} = 2.0 Vdc)	All Types		4.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 16 Adc, I_B = 4.0 Adc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	1000	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data. (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

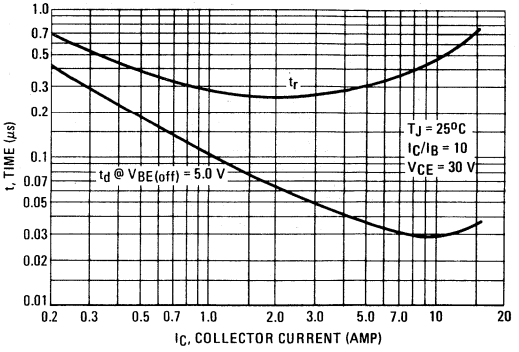


FIGURE 4 – THERMAL RESPONSE

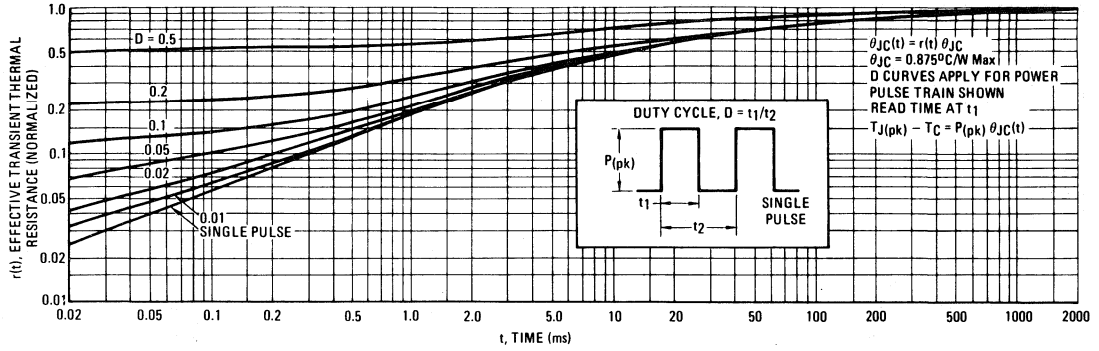
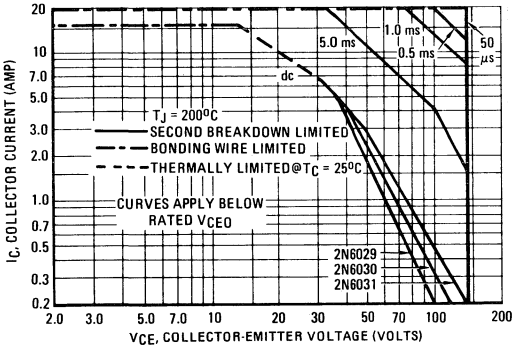


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 6 – TURN-OFF TIME

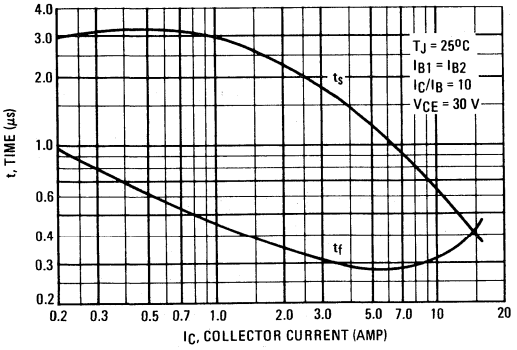


FIGURE 7 – CAPACITANCE

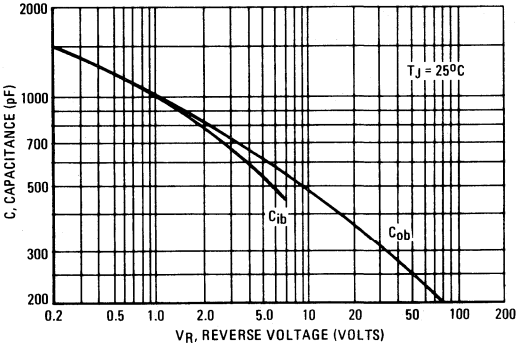


FIGURE 8 – DC CURRENT GAIN

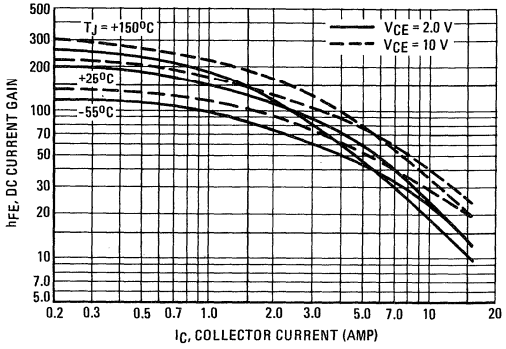


FIGURE 9 – COLLECTOR SATURATION REGION

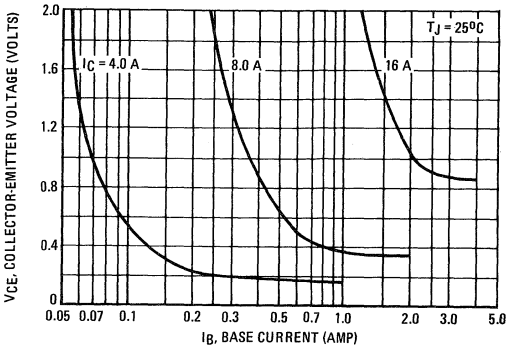


FIGURE 10 – "ON" VOLTAGES

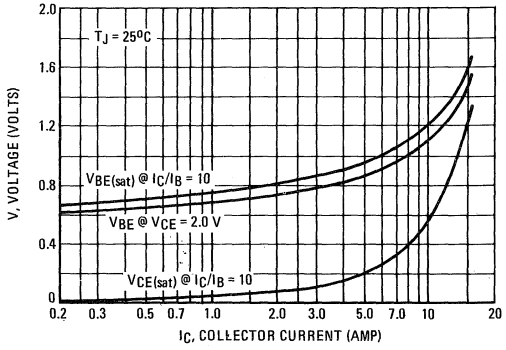


FIGURE 11 – TEMPERATURE COEFFICIENTS

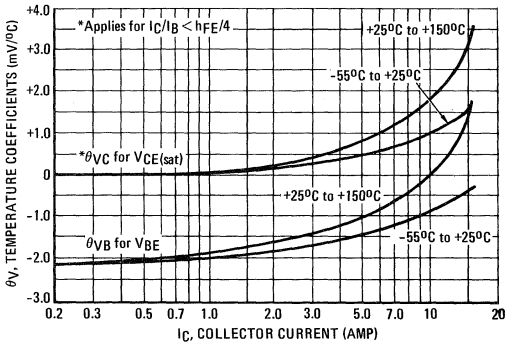


FIGURE 12 – COLLECTOR CUTOFF REGION

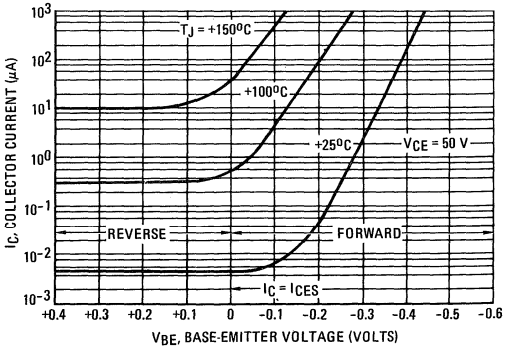
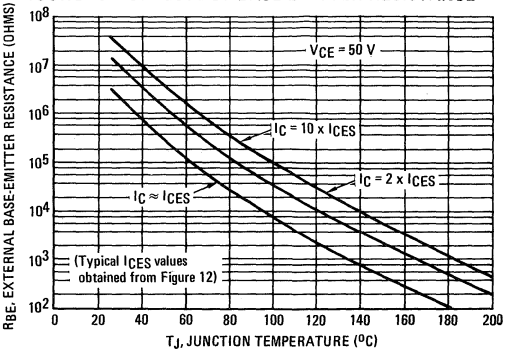


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



SMALL SIGNAL BIPOLAR TRANSISTORS

General Purpose Transistors		H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC237, 238, 239	Complementary Transistors	120-380	2	5	100	20-45	NPN	TO-92	4-1
BC307, 308, 309			2	5	100	20-45	PNP	TO-92	4-5
BC546, 547, 548	Complimentary Transistors	120-420	2	5	100	30-65	NPN	TO-92	4-46
BC556, 557, 558			2	5	100	30-65	PNP	TO-92	4-61
BF257, 258, 259	Video O/P Transistors	25	30	10	100	160-300	NPN	TO-39	4-93
MPS A13, A14	Darlington Transistors	10K-20K	100	5	300	30	NPN	TO-92	4-138
MPS A16, A17	Switching Transistors	200	5	10	100	40	NPN	TO-92	4-141
MPS A62, A63, A64	Darlington Transistors	10K-20K	100	5	300	20-30	PNP	TO-92	4-143
MPS L01	High Voltage Transistor	50	10	5	150	120	NPN	TO-92	4-147

Low Noise/Good H_{FE} Linearity Transistors		H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC413, 414	Amplifier Transistors	180-380	2	5	100	30-45	NPN	TO-92	4-18
BC415, 416	Amplifier Transistors	180-380	2	5	100	30-45	PNP	TO-92	4-25
BC549, 550	Amplifier Transistors	180-380	2	5	100	30-45	NPN	TO-92	4-54
BC559, 560	Amplifier Transistors	100-380	2	5	100	30-45	PNP	TO-92	4-67
BC650,S – 651,S	Amplifier Transistors	380-680	2	5	200	30-45	NPN	TO-92	4-74

High Frequency Transistors		H_{FE} @ (min.)	I_C mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BF198	TV/IF Amplifier Transistor	27	4	10	25	30	NPN	TO-92	4-80
BF199	TV/IF Amplifier Transistor	40	7	10	100	25	NPN	TO-92	4-83
BF240, 241	AM/FM Amplifier Transistors	36-67	1	10	25	40	NPN	TO-92	4-86
BF254, 255	AM/FM Amplifier Transistors	35-100	1	10	100	20	NPN	TO-92	4-90
BF371, 373	TV/IF Amplifier Transistors	40	7	10	100	30-45	NPN	TO-92	4-95
BF374, 375	VHF/TV Amplifier Oscillator Transistor	35-70	1	10	100	25	NPN	TO-92	4-99
BF391, 392, 393	High Voltage Video Transistors	40	10	10	500	200-300	NPN	TO-92	4-103
BF394, 395	AM/FM Amplifier Transistors	35-100	1	10	100	30	NPN	TO-92	4-106
BF479	UHF Amplifier Transistor	20	10	10	–	30	PNP	317A	4-110
BF491, 492, 493	High Voltage Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-114
BF506	VHF Oscillator/Mixer Transistor	20	3	10	50	35	PNP	TO-92	4-117
BF509	VHF Amplifier Transistor	20	3	10	50	35	PNP	TO-92	4-120
BF679	UHF Amplifier Transistor	35	3	10	–	35	PNP	317A	4-124
BF680	UHF Oscillator/Mixer Transistor	35	3	10	–	35	PNP	317A	4-128

High Voltage Transistors		H_{FE} @ → (min.)	I_C → mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC372, 373	Darlington Transistors	10K-25K	100	5	1000	80-100	NPN	TO-92	4-15
BC445, 447, 449	Driver/Output Transistors	50-180	2	5	300	60-100	NPN	TO-92	4-32
BC446, 448, 450	Driver/Output Transistors	50-180	2	5	300	60-100	PNP	TO-92	4-36
BC485, 487, 489	Driver/Output Transistors	60-160	100	2	1000	45-80	NPN	TO-92	4-40
BC486, 488, 490	Driver/Output Transistors	60-160	100	2	1000	45-80	PNP	TO-92	4-44
BF257, 258, 259	Video O/P Transistors	25	30	10	100	160-300	NPN	TO-39	4-93
BF391, 392, 393	Video Transistors	40	10	10	500	200-300	NPN	TO-92	4-103
BF491, 492, 493	Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-114
MPS A05, A06	Comp. Driver Transistors	50	10	1	500	60-80	NPN	TO-92	4-132
MPS A55, A56		50	10	1	500	60-80	PNP	TO-92	4-132
MPS L01	Amplifier Transistor	50	10	5	150	120	NPN	TO-92	4-147

4

High Current Transistors		H_{FE} @ → (min.)	I_C → mA	V_{CE} V	I_C (cont.) mA	BV_{CEO} V	Polarity	Package	Page
BC327, 328	Compl. Driver/OP Transistors	100-160	100	1	800	25-45	PNP	TO-92	4-9
BC337, 338		100-160	100	1	800	25-45	NPN	TO-92	4-12
BC372, 373	Darlington Transistors	10K-25K	100	5	1000	80-100	NPN	TO-92	4-15
BC485, 487, 489	Driver/Output Transistors	60-160	100	2	1000	45-80	NPN	TO-92	4-40
BC486, 488, 490	Driver/Output Transistors	60-160	100	2	1000	45-80	PNP	TO-92	4-44
BF391, 392, 393	Video Transistors	40	10	10	500	200-300	NPN	TO-92	4-103
BF491, 492, 493	Video Transistors	40	10	10	500	200-300	PNP	TO-92	4-114
MPS A05, A06	Compl. Driver Transistors	50	10	1	500	60-80	NPN	TO-92	4-132
MPS A55, A56		50	10	1	500	60-80	PNP	TO-92	4-132

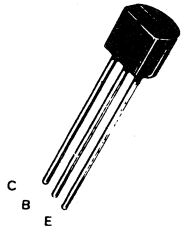
BC238

NPN SILICON ANNULAR TRANSISTORS

. . . designed for general-purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 45, 20, 45 Vdc (Min) @ I_C = 2.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 100 mAdc
- Low Collector-Base capacitance
  C_{cbo} = 4.5 pf (Max) @ V_{CB} = 10 Vdc
- Complementary to PNP BC 307, BC 308, BC 309
- One-Piece, Injection-Molded Unibloc † Package

NPN SILICON AMPLIFIER TRANSISTORS



For standard package order BC 237 / 238 / 239
For TO - 18 configuration order BC 237 - 18 / 238 - 18 / 239 - 18
For TO - 5 configuration order BC 237 - 5 / 238 - 5 / 239 - 5

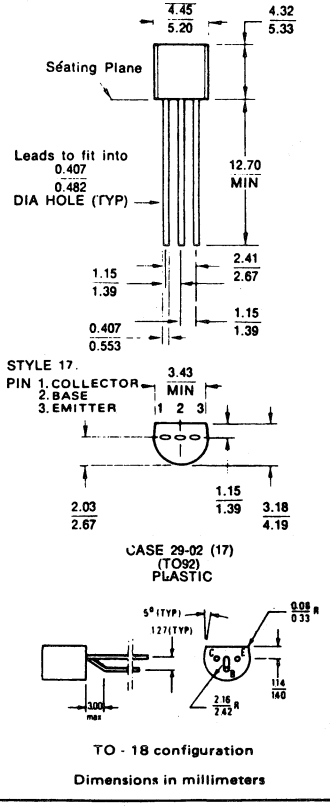
4

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BC 237 BC 238 BC 239	45 20 45	Vdc
Collector-Emitter Voltage	V_{CES}	BC 237 BC 238 BC 239	50 30 50	Vdc
Emitter-Base Voltage	V_{EB}		5.0	Vdc
Collector Current—Continuous Peak	I_C		0.10 0.20	Adc
Base Current—Continuous	I_B		0.05	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		350 2.81	mW mW/°C
Operating and Storage Junction Temperature range	T_J, T_{stg}		−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}		0.357	°C/mW



* Annular Semiconductors Patented by Motorola Inc.
† Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A 25° C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 237 BC 238 BC 239	BV_{CEO}	45 20 45			Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BC 237 BC 238 BC 239	BV_{EBO}	6 5 5			Vdc
Collector Cutoff Current						
(V_{CE} = 30Vdc, V_{BE} = 0)	BC 238	I_{CES}		0.20	15	
(V_{CE} = 50 Vdc, V_{BE} = 0)	BC 239 BC 237			0.20 0.20	15 15	ηAdc
(V_{CE} = 30 Vdc, V_{BE} = 0) T_A = 125 C	BC 238			0.20	4	
(V_{CE} = 50 Vdc, V_{BE} = 0) T_A = 125 C	BC 239 BC 237			0.20 0.20	4 4	μAdc
ON CHARACTERISTICS						
DC Current Gain						
(I_C = 10 μAdc, V_{CE} = 5 Vdc)		h_{FE}				
	BC 237A/238A			90		
	BC 237B/238B/239B			150		
	BC 237C/238C/239C			270		
(I_C = 2mAdc, V_{CE} = 5Vdc)						
	BC 237		120		800	
	BC 238		120		800	
	BC 239		180		800	
	BC 237A/238A		120	170	220	
	BC 237B/238B/239B		180	290	460	
	BC 237C/238C/239C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)						
	BC 237A/238A			120		
	BC 237B/238B/239B			180		
	BC 237C/238C/239C			300		
Collector-Emitter On Voltage						
(I_C = 100 μAdc, I_B = 5 μAdc)	BC 237/BC 238/BC 239	$V_{CE(sat)}$		0.07	0.20	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)	BC 237/BC 239			0.20	0.60	
	BC 238			0.20	–	
Base-Emitter Saturation Voltage						
(I_C = 100 μAdc, I_B = 5 μAdc)		$V_{BE(sat)}$		0.60	0.83	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)				1.05		
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 100 μAdc, V_{CE} = 5 Vdc)				0.50		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55	0.62	0.70	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)				0.83		

DYNAMIC CHARACTERISTICS, SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain-Bandwidth Product		f_T				MHz
(I_C = 0.5 mAdc, V_{CE} = 3 Vdc, f = 100 MHz)						
	BC 237			100		
	BC 238			120		
	BC 239			140		
(I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)						
	BC 237		150	200		
	BC 238		150	240		
	BC 239		150	280		
Collector-Base Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, I_C = 0, f = 1 MHz)					4.50	
Emitter-Base Capacitance		C_{eb}				pF
(V_{BE} = 0.5 Vdc, I_C = 0, f = 1 MHz)				8.0		
Input Impedance		h_{ie}(h11e)				K ohm
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A		1.6	2.2	4.5	
	BC 237B/238B/239B		3.2	6.0	8.5	
	BC 237C/238C/239C		6.0	8.7	15.0	
Voltage Feedback Ratio		h_{re}(h12e)				X10 $^{-4}$
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A			1.5		
	BC 237B/238B/239B			2.0		
	BC 237C/238C/239C			3.0		
Small-Signal Current Gain		h_{fe}(h21e)				
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A		125	220	260	
	BC 237B/238B/239B		240	330	500	
	BC 237C/238C/239C		450	600	900	
Output Admittance		h_{oe}(h22e)				μ mhos
(I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)						
	BC 237A/238A			8	25	
	BC 237B/238B/239B			10	35	
	BC 237C/238C/239C			12	50	
Noise Figure		NF				dB
(I_C = 0.2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 30 Hz to 15 KHz)	BC 239			2	4	
(I_C = 0.2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 1 KHz, Δf = 200 Hz)	BC 237			2	10	
	BC 238			2	10	
	BC 239			2	4	

4

FIGURE 1 - NORMALIZED DC CURRENT GAIN

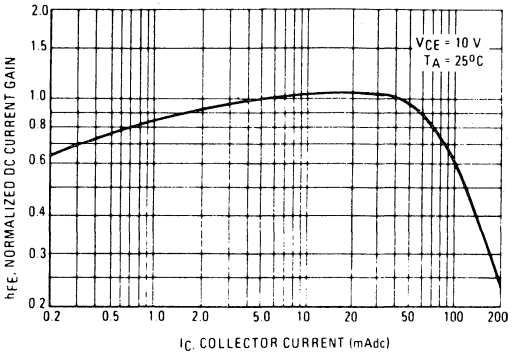


FIGURE 2 - "SATURATION" AND "ON" VOLTAGES

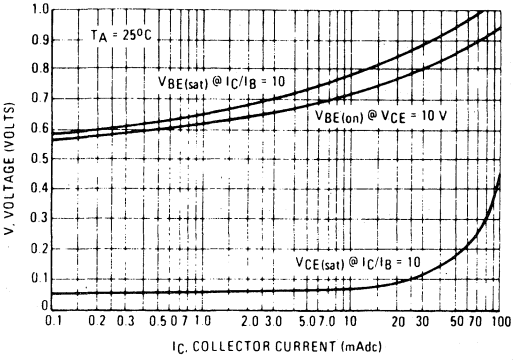


FIGURE 3 - CURRENT-GAIN-BANDWIDTH PRODUCT

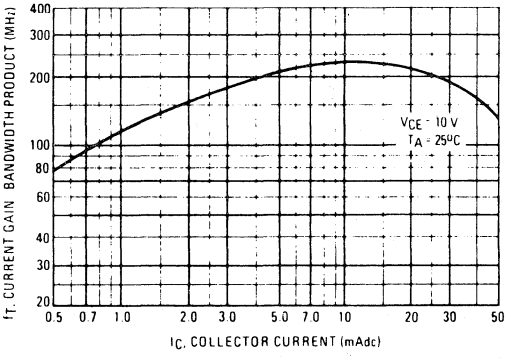


FIGURE 4 - CAPACITANCES

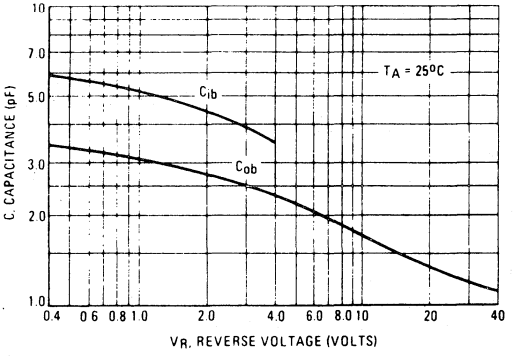


FIGURE 5 - OUTPUT ADMITTANCE

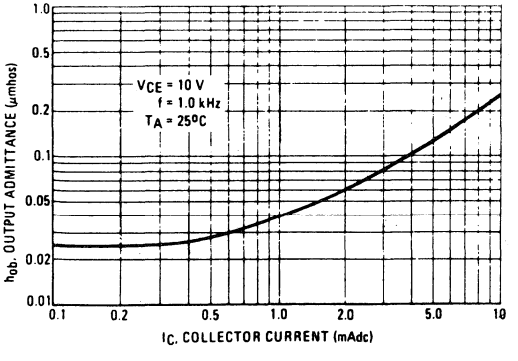
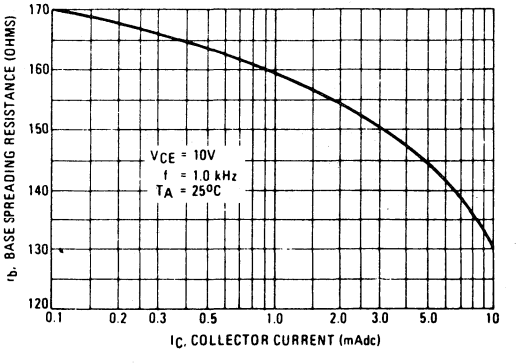


FIGURE 6 - BASE SPREADING RESISTANCE



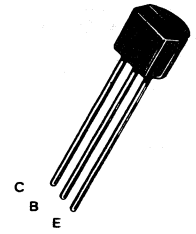
BC307
BC308 • BC309

PNP SILICON ANNULAR* TRANSISTORS

. . . designed for general purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 20, 25, 45 Vdc (Min) @ I_C = 2.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE\ (sat)}$ = 0.35 Vdc (Typ) @ I_C = 100 mAdc
- Low Collector - Base capacitance
  C_{cbo} = 6.0 pF (Max) @ V_{CB} = 10 Vdc
- Complementary to NPN BC 237, BC 238, BC 239
- One-Piece, Injection-Molded Unibloc† Package

PNP SILICON AMPLIFIER TRANSISTORS



For standard package order BC 307 / 308 / 309
For TO - 18 configuration order BC 307 - 18 / 308 - 18 / 309 - 18
For TO - 5 configuration order BC 307 - 5 / 308 - 5 / 309 - 5

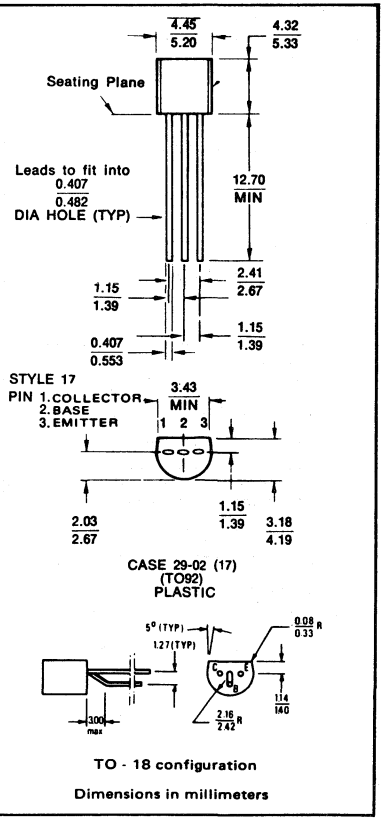
4

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BC 307 BC 308 BC 309	45 25 45	Vdc
Collector-Emitter Voltage	V_{CES}	BC 307 BC 308 BC 309	50 30 50	Vdc
Emitter-Base Voltage	V_{EB}	all	5.0	Vdc
Collector Current - Continuous Peak	I_C I_{CM}	all	0.10 0.20	A
Base Current - Continuous	I_B	all	0.05	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	all	0.30 2.40	Watts mW/°C
Operating and Storage Junction Temperature range	T_J,T_{stg}	all	-55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol		Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}		0.416	°C/mW



TO - 18 configuration

Dimensions in millimeters

* Annular Semiconductors Patented by Motorola Inc.
† Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 307	BV_{CEO}	45	–	–	Vdc
	BC 308		25	–	–	
	BC 309		45	–	–	
Emitter-Base Breakdown Voltage (I_E = 100μAdc, I_C = 0)	BC 307	BV_{EBO}	5	–	–	Vdc
	BC 308		5	–	–	
	BC 309		5	–	–	
Collector-Emitter Leakage Current (V_{CES} = 20 V)	BC 307	I_{CES}	–	2	100	nA
	BC 308		–	2	100	
	BC 309		–	2	100	
(V_{CES} = 20 V, T_A = 125°C)	BC 307		–	–	4	μA
	BC 308		–	–	4	
	BC 309		–	–	4	
ON CHARACTERISTICS						
DC Current Gain (I_C = 10 μ Adc, V_{CE} = 5 Vdc)		h_{FE}				
	BC 307A/308A/309A		–	90	–	
	BC 307B/308B/309B		–	150	–	
	BC 307C/308C/309C		–	270	–	
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 307		120	–	800	
	BC 308		120	–	800	
	BC 309		120	–	800	
	BC 307A/308A/309A		120	170	220	
	BC 307B/308B/309B		180	290	460	
	BC 307C/308C/309C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 307A/308A/309A		–	120	–	
	BC 307B/308B/309B		–	180	–	
	BC 307C/308C/309C		–	300	–	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0,5 mAdc)		V_{CE} (sat)	–	0.10	–	Vdc
(I_C = 10 mAdc, I_B = see Note 1)			–	0.30	0.60	
(I_C = 100 mAdc, I_B = 5 mAdc)			–	0.25	–	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc)		V_{BE} (sat)	–	0.70	–	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)			–	1.00	–	
Base-Emitter on Voltage (I_C = 2 mAdc, V_{CE} = 5 Vdc)		V_{BE} (on)	0.55	0.62	0.70	Vdc

Note 1 : I_C = 10 mAdc on the constant base current characteristic, which yields the point I_C = 11 mAdc, V_{CE} = 1 V

DYNAMIC CHARACTERISTICS / SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain – Bandwidth Product (I_C= 10 mAdc, V_{CE}= 5 Vdc, f = 50 MHz)		f_T				MHz
	BC 307		–	280	–	
	BC 308		–	320	–	
	BC 309		–	360	–	
Collector-Base Capacitance (V_{CB}= 10 Vdc, I_C= 0, f = 1 MHz)		C_{cbo}	–	–	6.0	pF
Noise Figure		NF				dB
(I_C= 0.2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 30 Hz to 15 KHz)	BC 309		–	2	4	
(I_C= 0,2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 1 KHz, f = 200 Hz)	BC 307		–	2	10	
	BC 308		–	2	10	
	BC 309		–	2	4	
Input Impedance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{ie}(h_{11e})$				kΩ
	BC 307A/308A/309A		1.2	2.7	4.5	
	BC 307B/308B/309B		3.0	4.5	8.0	
	BC 307C/308C/309C		5.0	8.0	14.0	
Voltage Feedback Ratio (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{re}(h_{12e})$				10^{-4}
	BC 307A/308A/309A		–	3.0	–	
	BC 307B/308B/309B		–	3.5	–	
	BC 307C/308C/309C		–	4.0	–	
Small Signal Current Gain (I_C= 2 mAdc, V_{CE}= 5 Vdc f = 1 KHz)		$h_{fe}(h_{21e})$				–
	BC 307A/308A/309A		125	220	260	
	BC 307B/308B/309B		240	330	500	
	BC 307C/308C/309C		450	600	900	
Output Admittance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f= 1 KHz)		$h_{oe}(h_{22e})$				μmhos
	BC 307A/308A/309A		–	25	50	
	BC 307B/308B/309B		–	30	70	
	BC 307C/308C/309C		–	60	110	

FIGURE 1 – NORMALIZED DC CURRENT GAIN

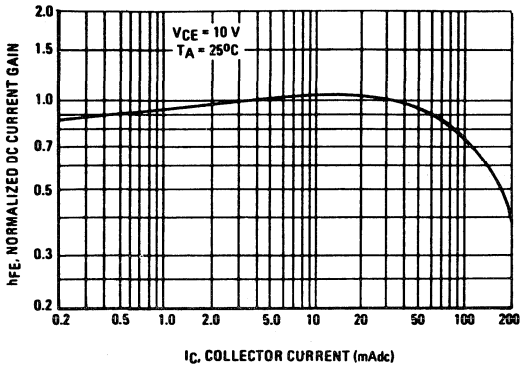


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

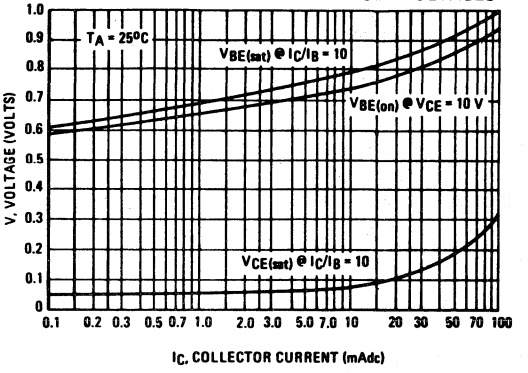


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

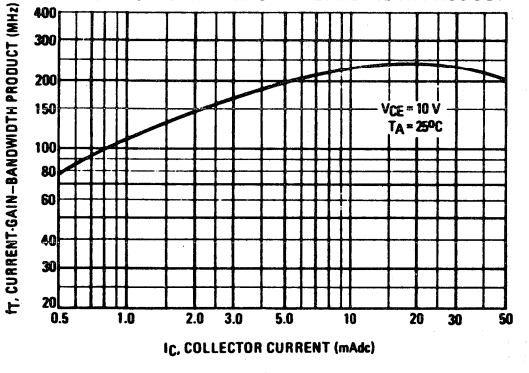


FIGURE 4 – CAPACITANCES

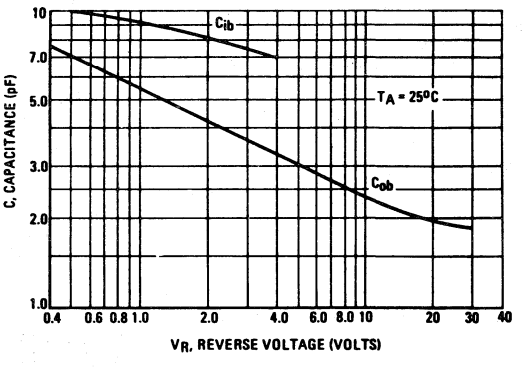


FIGURE 5 – OUTPUT ADMITTANCE

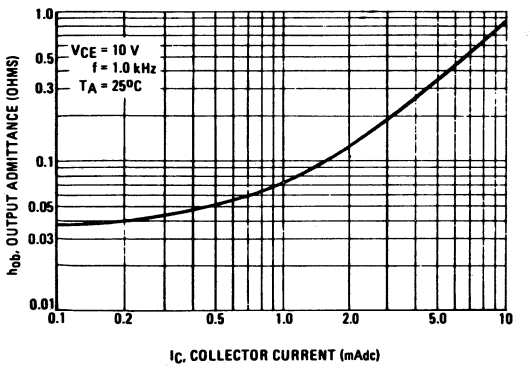
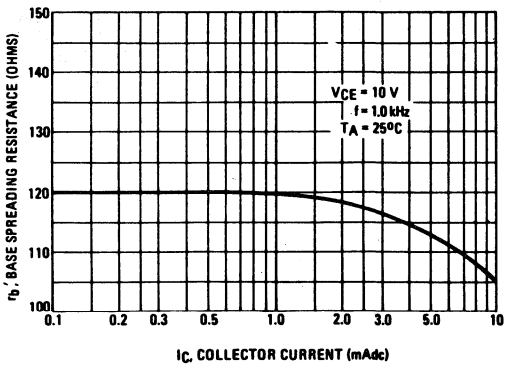


FIGURE 6 – BASE SPREADING RESISTANCE



BC327
BC328

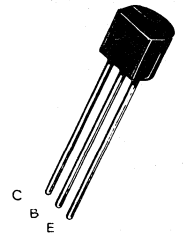
PNP SILICON ANNULAR♦ TRANSISTORS

... designed for complementary driver and output stages where the following features are important.

- High Peak Current of 1 Amp
- High Gain, h_{FE} – 40 min at I_C – 300 mA
- Low Saturation Voltage, $V_{CE\ sat}$ – 0.7 Volts max. at I_C – 500 mA
- High Power Dissipation[1], P_D – 1.5 Watt
- One-Piece, Injection-Molded Unibloc Package
- Complementary to NPN BC337, BC338
- Available in -16 and -25 gain groups

[1] T Case ≤ 25 °C.

PNP SILICON AMPLIFIER TRANSISTORS



For standard package order BC327/BC328
For TO - 18 configuration order BC327 - 18/328 - 18
For TO - 5 configuration order BC327 - 5/328 - 5

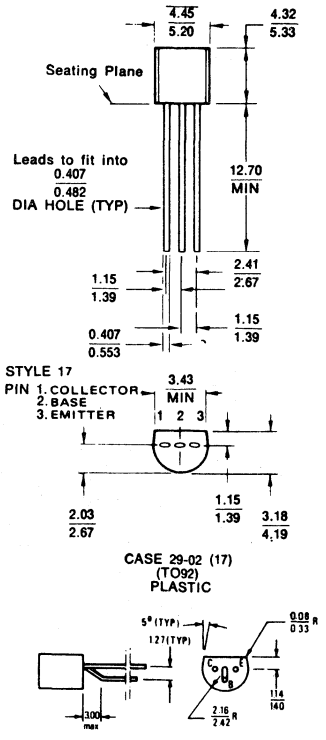
MAXIMUM RATINGS

Rating	Symbol	BC327	BC328	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	Vdc
Collector-Base Voltage	V_{CB}	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25° C	P_D	625 5.0		mW mW/° C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25° C	P_D	1.5 12.0		Watt mW/° C
DC Collector Current	I_C	800		mA
Collector Current (10 μsec pulse)	I_C	1.0		A
DC Base Current	I_B	100		mA
Base Current (10 μsec pulse)	I_B	200		mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors patented by Motorola Inc.



TO-18 configuration
Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics & Conditions	Symbol	Type	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10mA, I_B = 0	BV_{CEO}	BC327 BC328	45 25			Vdc
Collector-Base Breakdown Voltage I_C = 10μA, I_E = 0	BV_{CBO}	BC327 BC328	50 30			Vdc
Emitter-Base Breakdown Voltage I_E = 10μA, I_C = 0	BV_{EBO}		5			Vdc
Collector Cutoff Current BC327 — V_{CB} = 30V I_E = 0 BC328 — V_{CB} = 20V I_E = 0	I_{CBO}				100	nAdc
Emitter Cutoff Current V_{EB} = 4V, I_C = 0	I_{EBO}				100	nAdc
DC Current Gain I_C = 100mA, V_{CE} = 1V BC327/BC328 BC327-16/BC328-16 BC327-25/BC328-25 I_C = 300mA, V_{CE} = 1V	h_{FE}		 100 100 160 40		 600 250 400	
Base-Emitter On Voltage I_C = 300mA, V_{CE} = 1V	$V_{BE(on)}$				1.2	Vdc
Collector-Emitter Saturation Voltage I_C = 500mA, I_B = 50mA	$V_{CE(sat)}$				0.7	Vdc
Output Capacitance V_{CB} = 10V, I_E = 0 f = 1MHz	C_{ob}			5		pF
Current-Gain-Bandwidth Product I_C = 10mA, V_{CE} = 5V	f_T			260		MHz

FIGURE 1 – THERMAL RESPONSE

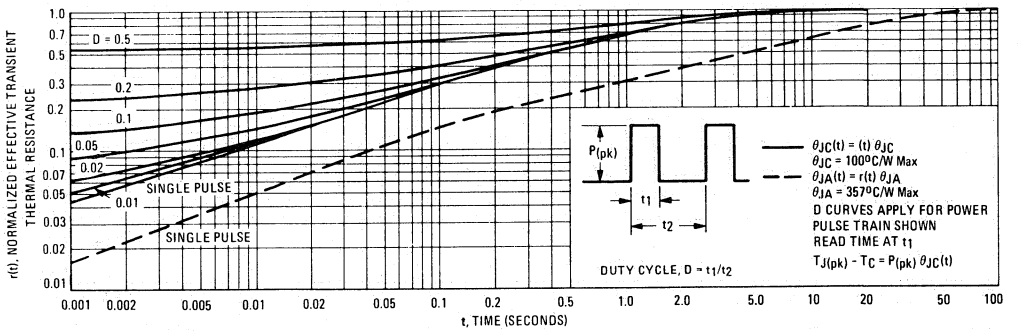


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

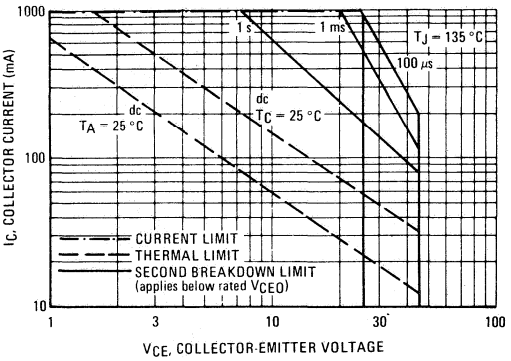


FIGURE 3 – DC CURRENT GAIN

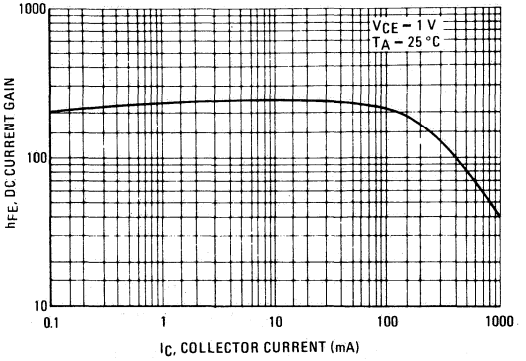


FIGURE 4 – SATURATION REGION

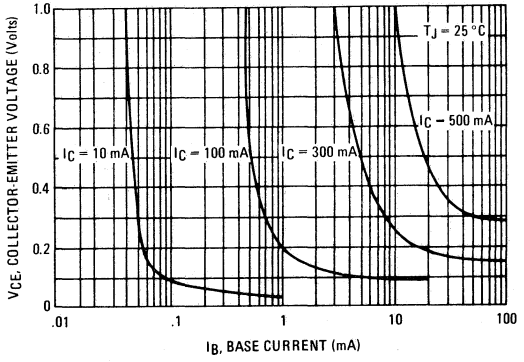


FIGURE 5 – "ON" VOLTAGES

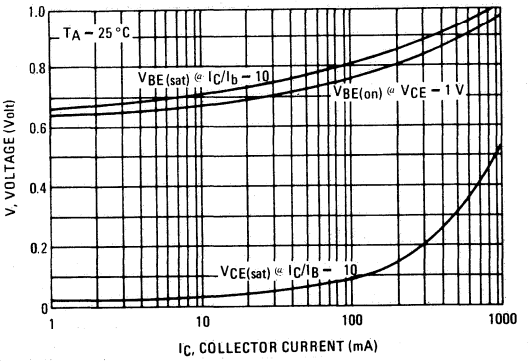


FIGURE 6 – TEMPERATURE COEFFICIENTS

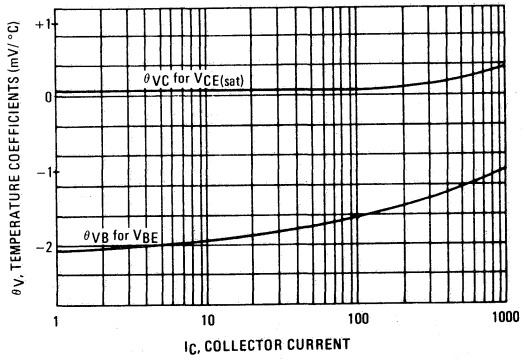
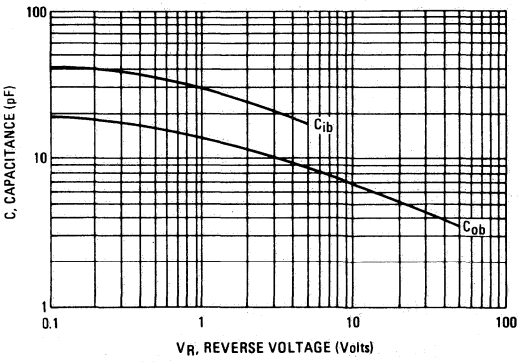


FIGURE 7 – CAPACITANCES



BC337
BC338

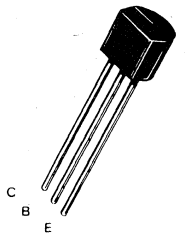
NPN SILICON ANNULAR♦ TRANSISTORS

... designed for complementary driver and output stages where the following features are important.

- High Peak Current of 1 Amp
- High Gain, h_{FE} = 60 min at I_C = 300 mA
- Low Saturation Voltage, V_{CEsat} = 0.7 Volts max. at I_C = 500 mA
- High Power Dissipation[1], P_D = 1.5 Watt
- One-Piece, Injection-Molded Unibloc Package
- Complementary to PNP BC327, BC328
- Available in -16, -25 and -40 gain groups

[1] T Case ≦ 25 °C.

NPN SILICON AMPLIFIER TRANSISTORS



For standard package order BC 337 / BC 338
For TO - 18 configuration order BC 337 - 18 / 338 - 18
For TO - 5 configuration order BC 337 - 5 / 338 - 5

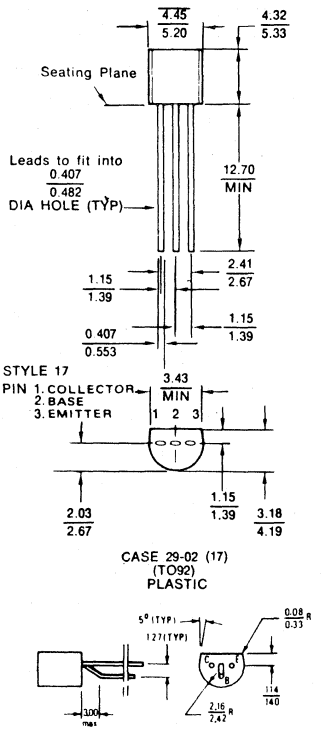
MAXIMUM RATINGS

Rating	Symbol	BC337	BC338	Unit
Collector-Emitter Voltage	V_{CEO}	45	25	Vdc
Collector-Base Voltage	V_{CB}	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Total Device Dissipation @ T_A = 25° C Derate above 25° C	P_D	625 5.0		mW mW/° C
Total Device Dissipation @ T_C = 25° C Derate above 25° C	P_D	1.5 12.0		Watt mW/° C
DC Collector Current	I_C	800		mA
Collector Current (10 μsec pulse)	I_C	1.0		A
DC Base Current	I_B	100		mA
Base Current (10 μsec pulse)	I_B	200		mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors patented by Motorola Inc.



TO-18 configuration
Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics & Conditions	Symbol	Type	Min.	Typ.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 10mA, I_B = 0	BV_{CEO}	BC337 BC338	45 25			Vdc
Collector-Base Breakdown Voltage I_C = 10μA, I_E = 0	BV_{CBO}	BC337 BC338	50 30			Vdc
Emitter-Base Breakdown Voltage I_E = 10μA, I_C = 0	BV_{EBO}		5			Vdc
Collector Cutoff Current BC337 — V_{CB} = 30V I_E = 0 BC338 — V_{CB} = 20V I_E = 0	I_{CBO}				100	nAdc
Emitter Cutoff Current V_{EB} = 4V, I_C = 0	I_{EBO}				100	nAdc
DC Current Gain I_C = 100mA, V_{CE} = 1V BC337/BC338 BC337-16/BC338-16 BC337-25/BC338-25 BC337-40/BC338-40 I_C = 300mA, V_{CE} = 1V	h_{FE}		 100 100 160 250 60		 600 250 400 600	
Base-Emitter On Voltage I_C = 300mA, V_{CE} = 1V	$V_{BE(on)}$				1.2	Vdc
Collector-Emitter Saturation Voltage I_C = 500mA, I_B = 50mA	$V_{CE(sat)}$				0.7	Vdc
Output Capacitance V_{CB} = 10V, I_E = 0 f = 1MHz	C_{ob}			4		pF
Current-Gain-Bandwidth Product I_C = 10mA, V_{CE} = 5V	f_T			210		MHz

FIGURE 1 – THERMAL RESPONSE

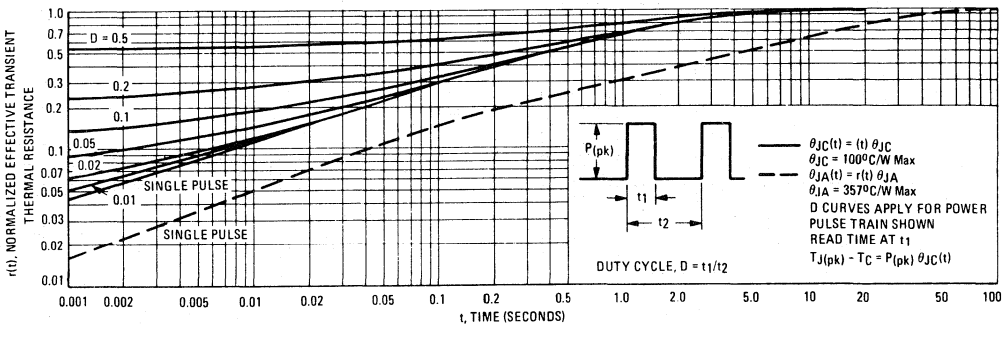


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

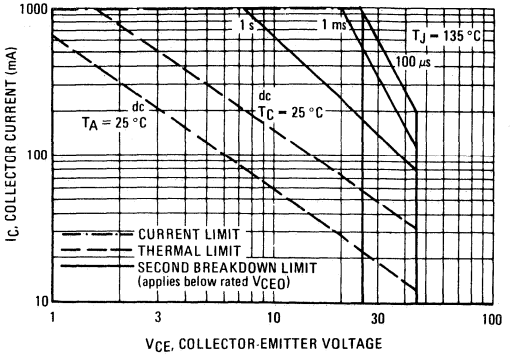


FIGURE 3 – DC CURRENT GAIN

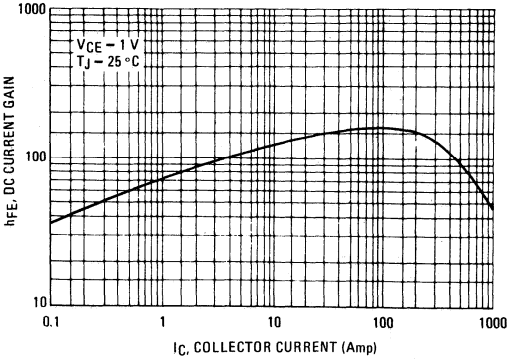


FIGURE 4 – SATURATION REGION

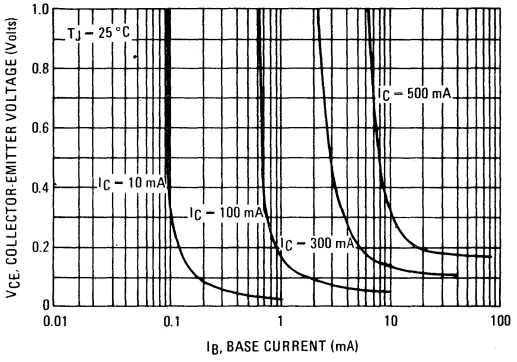


FIGURE 5 – "ON" VOLTAGES

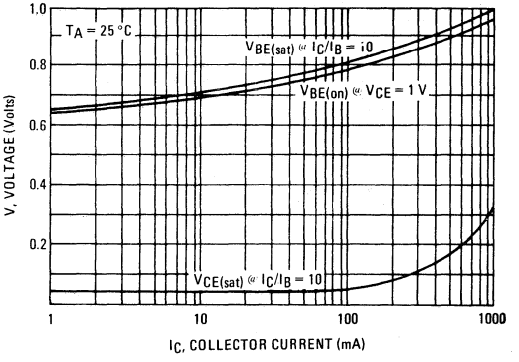


FIGURE 6 – TEMPERATURE COEFFICIENTS

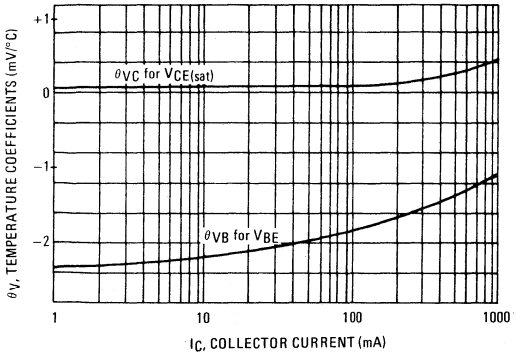
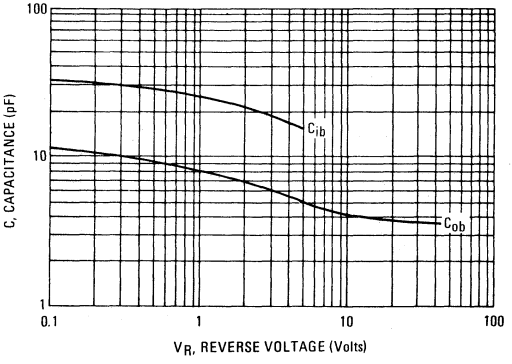


FIGURE 7 – CAPACITANCES



BC372
BC373

NPN SILICON HIGH VOLTAGE DARLINGTON

. . . designed for use relay driver and all inductive load applications.

- High Collector-Emitter Breakdown Voltage
  BV_{CES} – 100 V at 100 μA for BC372
  – 80 V at 100 μA for BC373
- High Current gain
  I_C – 100/mAdc, V_{CE} – 5 Vdc (min, 10000, max. 600000).
- Available in standardized gain groups (–16, –25, –40).

MAXIMUM RATINGS

Rating	Symbol	BC372	BC373	Unit
Collector-Emitter Voltage	V_{CEO}	100	80	Vdc
Collector-Base Voltage	V_{CB}	100	80	Vdc
Emitter-Base Voltage	V_{EB}	12		Vdc
Collector-Current-Continuous	I_C	1.0		Adc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0		W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

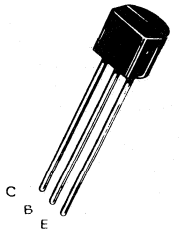
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

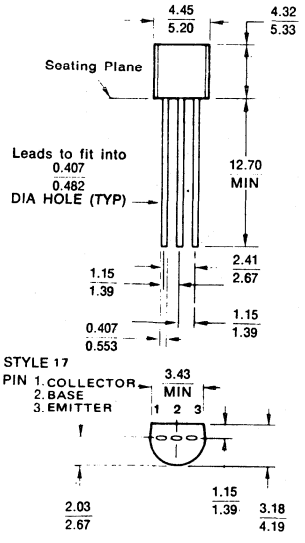
* Annular Semiconductors patented by Motorola Inc

[1] Due to the monolithic construction of this device breakdown voltages of both transistors are identical BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by boise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.

NPN SILICON DARLINGTON TRANSISTORS



For standard package order BC372, BC373
For TO - 18 configuration order
BC372-18, BC373-18
For TO - 5 configuration order
BC372-5, BC373-5.



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unlessotherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 100 μAdc, I_B = 0) BC372 BC373	BV_{CES}	100 80			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC372 BC373	BV_{CBO}	100 80			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	12			Vdc
Collector cutoff current V_{CB} = 80 Vdc – I_E = 0 BC372 V_{CB} = 60 Vdc – I_E = 0 BC373	I_{CBO}			100 100	nAdc
Emitter cutoff current V_{BE} = 10 V, I_C = 0	I_{EBO}			100	nAdc
ON CHARACTERISTICS*					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) plein range –16 –25 –40 (I_C = 250 mAdc, V_{CE} = 5 Vdc) plein range –16 –25 –40	h_{FE}	10 K 10 K 25 K 60 K 8 K 8 K 20 K 40 K		600 K 60 K 160 K 600 K	
Collector Emitter Saturation Voltage (I_C = 250 mAdc – I_B = 0,25 mAdc	$V_{CE\ (sat)}$		0.8	1	Vdc
Base Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 0,25 mAdc)	$V_{BE\ (sat)}$		1.4	2	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	f_T	100	200		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}		10	25	pF
Noise Figure (I_C = 1 mAdc, V_{CE} = 5 Vdc, R_g = 100 Kohm, F = 1 KHz	N_F		2.0		dB

*Pulse test – Pulse width = 300 μs – Duty cycle 2%.

FIGURE 1 – DC CURRENT GAIN

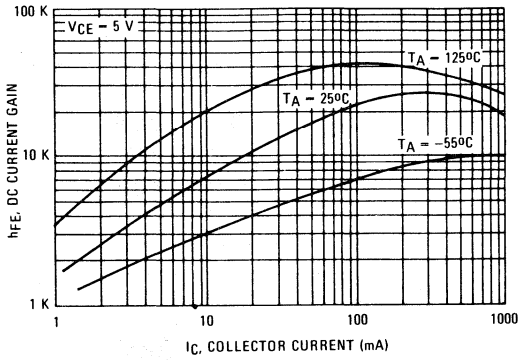


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

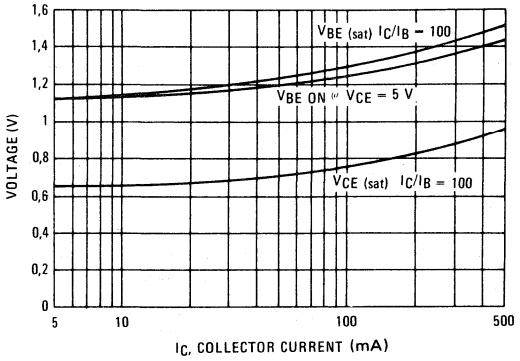


FIGURE 3 – CURRENT GAIN BANDWIDTH PRODUCT

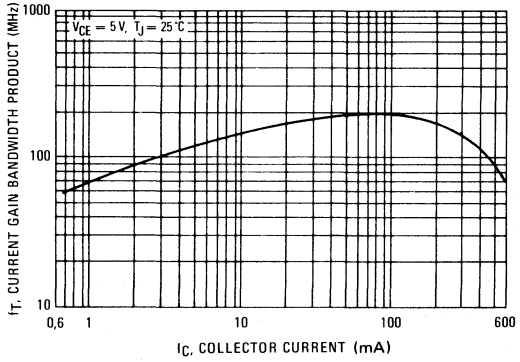
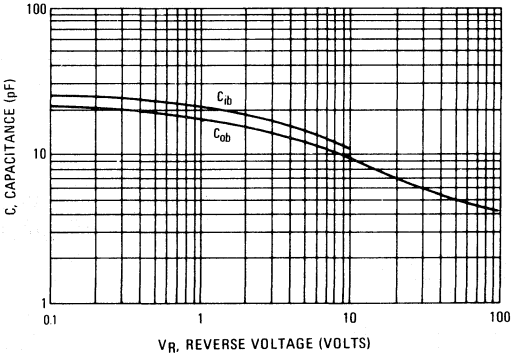


FIGURE 4 – CAPACITANCES

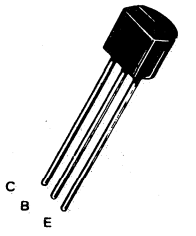


BC413
BC414

NPN SILICON ANNULAR♦
LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  NF = 2.5dB max (30Hz-15KHz)
- Low Noise At Low Frequency
  $V_T = 12nV/\sqrt{Hz}$ max (120Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  } (2mA/5V)
- Full Applications Information

NPN SILICON
LOW NOISE
TRANSISTOR



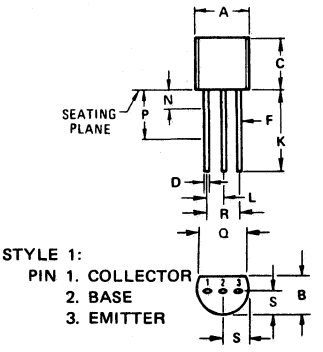
MAXIMUM RATINGS

Rating	Symbol	Value BC413	Value BC414	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at $T_A = 25\ ^oC$ Derate above 25 ^oC	P_D	350 2.81		mW mW/^{o}C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to + 150		^{o}C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	^{o}C/W

♦ Annular Semiconductors Patented by Motorola Inc.



STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

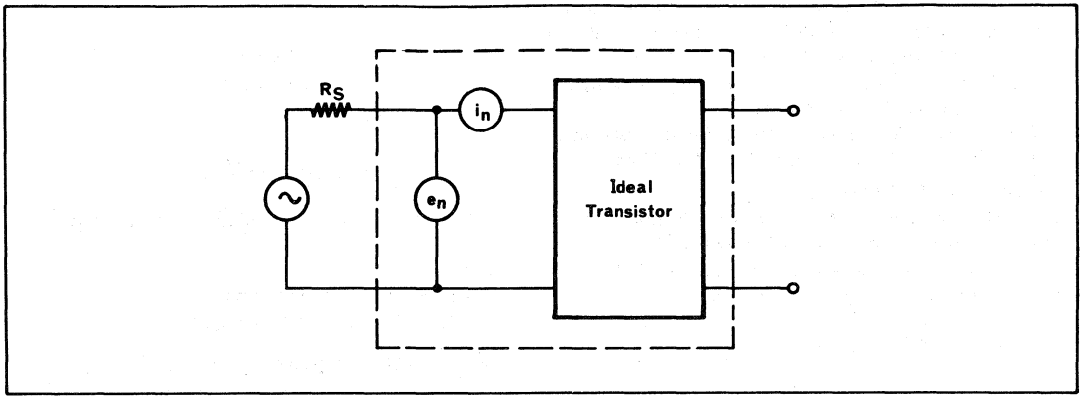
ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (I_C = 10mAdc, I_B = 0) BC413	BV_{CEO}	30			Vdc
BC414		45			
Collector-Base Breakdown Voltage (I_C = 10μAdc, I_E = 0) BC413	BV_{CBO}	45			Vdc
BC414		50			
Emitter-Base Breakdown Voltage (I_C = 10μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4Vdc, I_C = 0)	I_{EBO}			15	nAdc
On Characteristics					
DC Current Gain	h_{FE}				
(I_C = 10μAdc, V_{CE} = 5Vdc) BC413B/BC414B		100	150		
BC413C/BC414C		100	270		
(I_C = 2mAdc, V_{CE} = 5Vdc) BC413B/BC414B		180	290	460	
BC413C/BC414C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10mAdc, I_B = 0.5mAdc)			0.075	0.25	
(I_C = 10mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100mAdc, I_B = 5mAdc, see note 2)			0.25	0.6	
Base-Emitter Saturation Voltage (I_C = 100mAdc, I_B = 5mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100μAdc, V_{CE} = 5Vdc)			0.55		
(I_C = 2mAdc, V_{CE} = 5Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11mA at V_{CE} = 1V
Note 2: Pulse test = 300μs —— Duty Cycle = 2%

Characteristic	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Current-Gain-Bandwidth Product (I_C = 10mAdc, V_{CE} = 5Vdc, f = 100MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10Vdc, I_E = 0, f = 1MHz)	Ccbo		2.5		pF
h-Parameters (I_C = 2mAdc, V_{CE} = 5Vdc, f = 1KHz)					
Input Impedance BC413B/BC414B BC413C/BC414C	h_{ie} (h_{11e})	 3.2 6.0	 6.0 8.7	 8.5 15.0	KΩ
Voltage Feedback Ratio BC413B/BC414B BC413C/BC414C	h_{re} (h_{12e})		 2. 3.		10^{-4}
Small Signal Current Gain BC413B/BC414B BC413C/BC414C	h_{fe} (h_{21e})	 240 450	 330 600	 500 900	
Output Admittance BC413B/BC414B BC413C/BC414C	h_{oe} (h_{22e})		 10 12	 60 110	μ mhos
Noise Performance					
Noise Figure (I_C = 200μAdc, V_{CE} = 5Vdc, R_S = 2KΩ, f = 30Hz – 15KHz)	NF		0.6	2.5	dB
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 120Hz) See Application note, Section I	V_T		8.0	12	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 10Hz – 50Hz) See Application note, Section II	V_T		74	135	$nV/\sqrt{Hz}$

FIGURE 1. – TRANSISTOR NOISE MODEL.



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2 R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23} j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC414 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n = 4.5nV/$\sqrt{Hz}$ from figure 2 or figure 3 (Note that this is for a one cycle bandwidth)
Read i_n = 5.8pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})^2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})^2.(1 \times 10^3)^2]^{1/2}$$

Thus: $\boxed{V_T = 8.2nV}$

This checks with the value of 8nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})^2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7;

To minimize noise in a transistor stage, one might use figure 7 and deduce that noise is minimized when Noise Figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T \cdot f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\Delta f = 1Hz$), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 = 10Hz$, $f_2 = 50Hz$ at $I_C = 200\mu A$ and $R_S = 2K\Omega$

This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)]^2 \, df$$

$(f_1 - f_2)$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4KT\,R_S + i_{n(f)}^2\,R_S^2$$

$e_{n(f)}$ and 4 KT R_S are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f}$$ (1/f noise spectrum density)

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$

$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\,KT\,R_S) \times (f_2-f_1) + R_S^2\, i_{n(f1)}^2 \times f1 \times i_n\,(f1)\,\frac{f2}{f1}$$

Now:

$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)

$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\,(10Hz-50Hz) = [(25 + 33.1)40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus:

$$V_T(10Hz-50Hz) = 74\ nV$$

FIGURE 2 – NOISE VOLTAGE vs FREQUENCY.

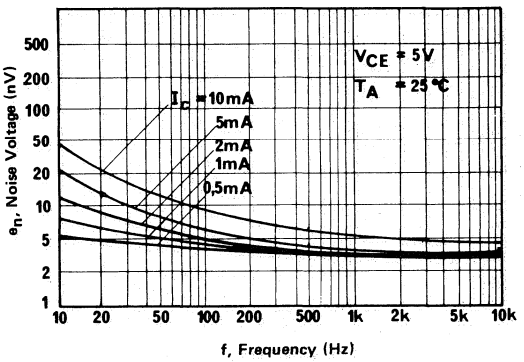


FIGURE 3. – NOISE VOLTAGE vs COLLECTOR CURRENT.

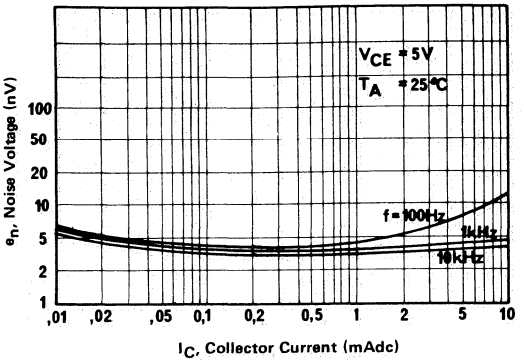


FIGURE 4. – NOISE CURRENT.

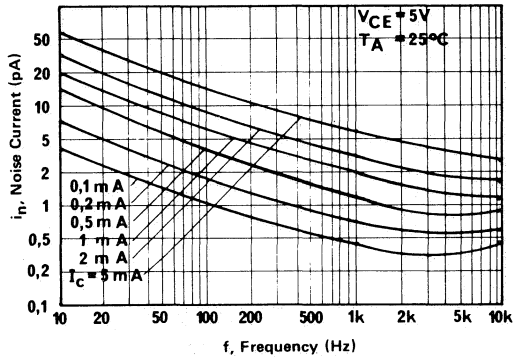


FIGURE 5. – WIDEBAND NOISE FIGURE.

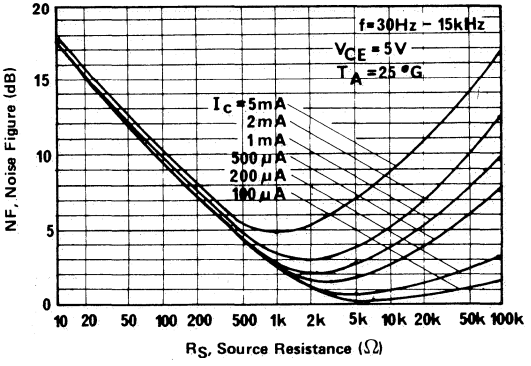


FIGURE 6. – TOTAL NOISE VOLTAGE (120 Hz).

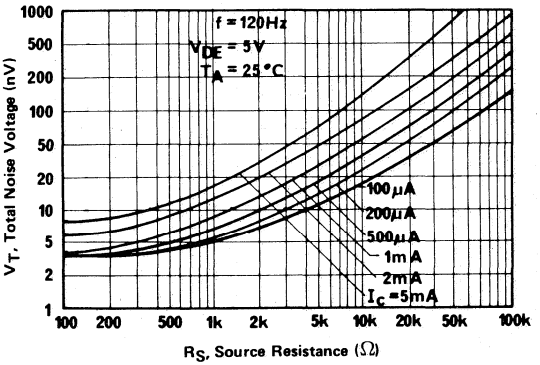


FIGURE 7. – NOISE FIGURE (120 Hz).

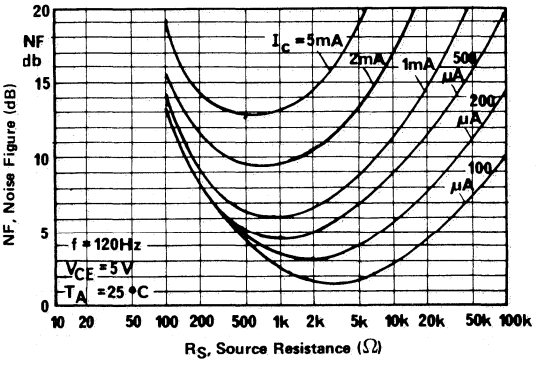


FIGURE 8. – NORMALIZED DC CURRENT GAIN.

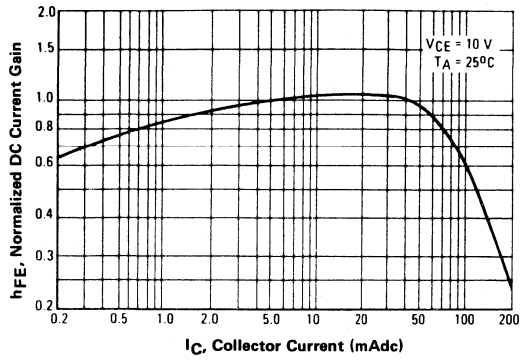


FIGURE 9. – "SATURATION" AND "ON" VOLTAGES.

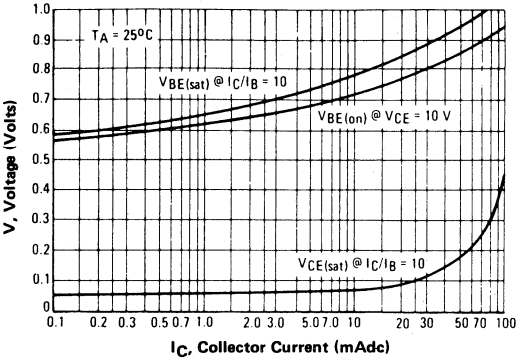


FIGURE 10. – CURRENT GAIN–BANDWIDTH PRODUCT.

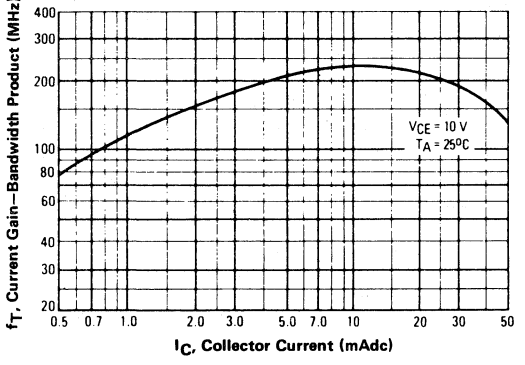


FIGURE 11. – CAPACITANCES.

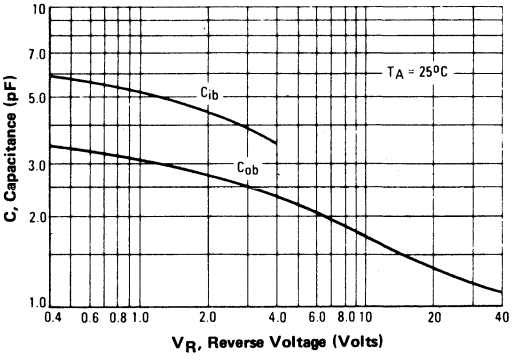


FIGURE 12. – OUTPUT ADMITTANCE.

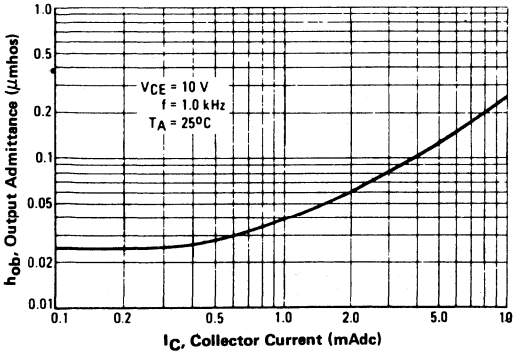
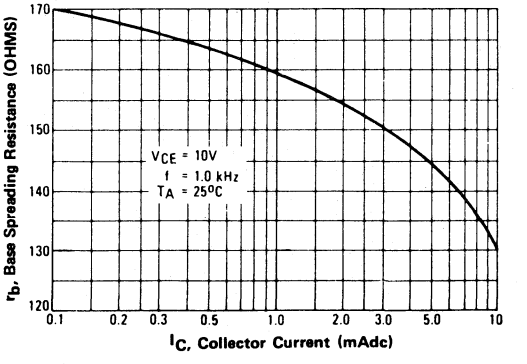


FIGURE 13. – BASE SPREADING RESISTANCE.

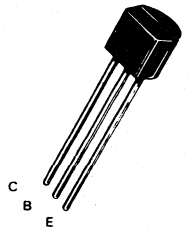


BC415
BC416

PNP SILICON ANNULAR♦
LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  NF = 2.5dB max (30Hz-15KHz)
- Low Noise At Low Frequency
  $V_T = 10nV/\sqrt{Hz}$ max (120Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  (2mA/5V)
- Full Applications Information

PNP SILICON
LOW NOISE
TRANSISTOR



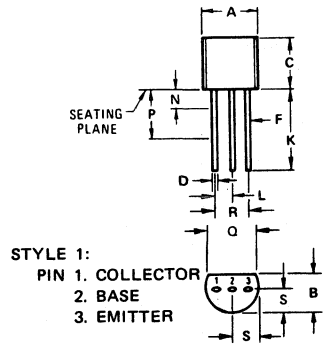
MAXIMUM RATINGS

Rating	Symbol	Value BC415	Value BC416	Unit
Collector-Emitter Voltage	V_{CEO}	35	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at $T_A = 25\ ^oC$ Derate above 25 ^oC	P_D	350 2.81		mW mW/^oC
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to + 150		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	$^oC/W$

♦ Annular Semiconductors Patented by Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (I_C = 10mAdc, I_B = 0) BC415	BV_{CEO}	35			Vdc
BC416		45			
Collector-Base Breakdown Voltage (I_C = 10μAdc, I_E = 0) BC415	BV_{CBO}	45			Vdc
BC416		50			
Emitter-Base Breakdown Voltage (I_C = 10μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4Vdc, I_C = 0)	I_{EBO}			15	nAdc
On Characteristics					
DC Current Gain	h_{FE}				
(I_C = 10μAdc, V_{CE} = 5Vdc) BC415B/BC416B		100	150		
BC415C/BC416C		100	270		
(I_C = 2mAdc, V_{CE} = 5Vdc) BC415B/BC416B		180	290	460	
BC415C/BC416C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10mAdc, I_B = 0.5mAdc)			0.075	0.25	
(I_C = 10mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100mAdc, I_B = 5mAdc, see note 2)			0.25		
Base-Emitter Saturation Voltage (I_C = 100mAdc, I_B = 5mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100μAdc, V_{CE} = 5Vdc)			0.55		
(I_C = 2mAdc, V_{CE} = 5Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11mA at V_{CE} = 1V
Note 2: Pulse test = 300μs —— Duty Cycle = 2%

Characteristic	Symbol	Min	Typ	Max	Unit

Dynamic Characteristics

Current-Gain-Bandwidth Product (I_C = 10mAdc, V_{CE} = 5Vdc, f = 100MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10Vdc, I_E = 0, f = 1MHz)	Ccbo		2.5		pF

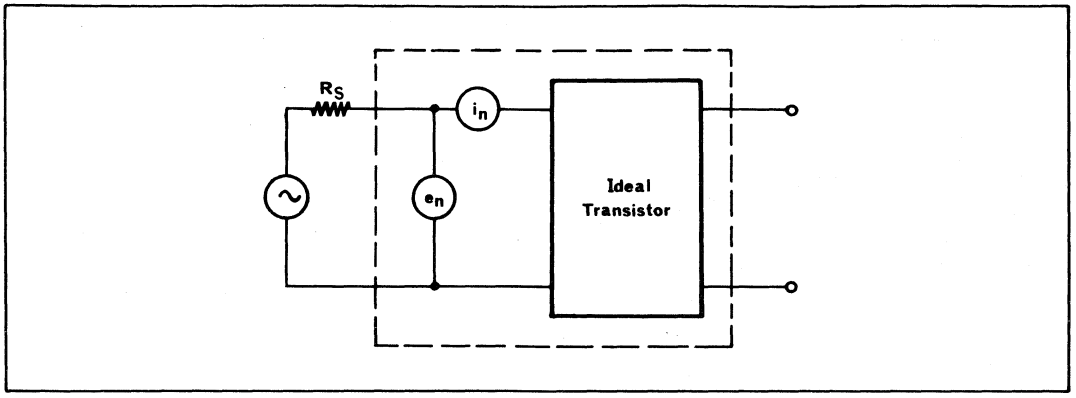
h-Parameters (I_C = 2mAdc, V_{CE} = 5Vdc, f = 1KHz)

Input Impedance	h_{ie}				KΩ
BC415B/BC416B	(h_{11e})	3.2	6.0	8.5	
BC415C/BC416C		5.0	8.0	14.0	
Voltage Feedback Ratio	h_{re}				10^{-4}
BC415B/BC416B	(h_{12e})		3.5		
BC415C/BC416C			4.0		
Small Signal Current Gain	h_{fe}				
BC415B/BC416B	(h_{21e})	240	330	500	
BC415C/BC416C		450	600	900	
Output Admittance	h_{oe}				μ mhos
BC415B/BC416B	(h_{22e})		10	60	
BC415C/BC416C			12	110	

Noise Performance

Noise Figure (I_C = 200μAdc, V_{CE} = 5Vdc, R_S = 2KΩ, f = 30Hz – 15KHz)	NF		0.5	2.0	dB
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 120Hz) See Application note, Section I	V_T		8	10	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200μAdc, V_{CE} = 5V, R_S = 2KΩ, f = 10Hz – 50Hz) See Application note, Section II	V_T		74	110	$nV/\sqrt{Hz}$

FIGURE 1. – TRANSISTOR NOISE MODEL.



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23}j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC414 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read $e_n = 4.5nV/\sqrt{Hz}$ from figure 2 or figure 3 (Note that this is for a one cycle bandwidth)
Read $i_n = 5.8pA/\sqrt{Hz}$ from figure 4

$$V_T = [(4.5 \times 10^{-9})2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})2.(1 \times 10^3)2]^{1/2}$$

Thus: $\boxed{V_T = 8.2nV}$

This checks with the value of 8nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7;

To minimize noise in a transistor stage, one might use figure 7 and deduce that noise is minimized when Noise Figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\Delta f = 1Hz$), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 = 10Hz$, $f_2 = 50Hz$ at $I_C = 200\mu A$ and $R_S = 2K\Omega$

This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)]^2 \, df$$
$$(f_1 - f_2)$$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4KT\,R_S + i_{n(f)}^2 R_S^2$$

$e_{n(f)}$ and 4 KT R_S are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f}$$ (1/f noise spectrum density)

G(f) bandpass filter
$= 1$ for $f \in (f_1, f_2)$
$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\,KT\,R_S) \times (f_2-f_1) + R_S^2\, i_{n(f1)}^2 \times f1 \times i_n\,(f1)\,\frac{f2}{f1}$$

Now:
$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)
$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\,(10Hz-50Hz) = [(25 + 33.1)40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10Hz-50Hz) = 74\ nV}$

FIGURE 2. – NOISE VOLTAGE vs FREQUENCY.

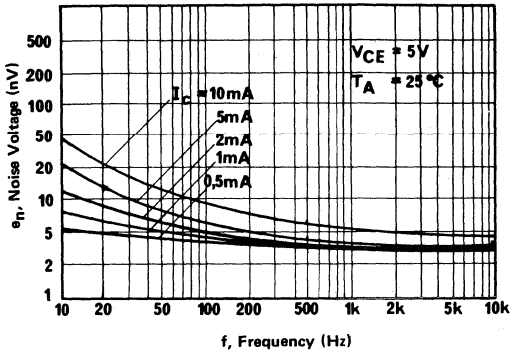


FIGURE 3. – NOISE VOLTAGE vs COLLECTOR CURRENT.

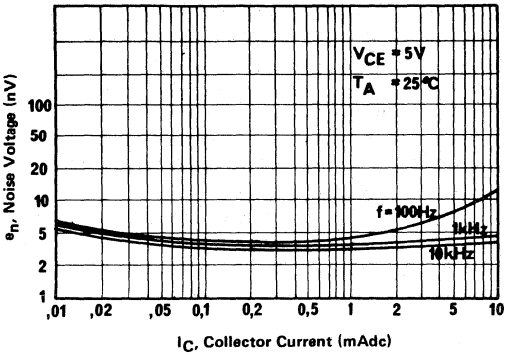


FIGURE 4. – NOISE CURRENT.

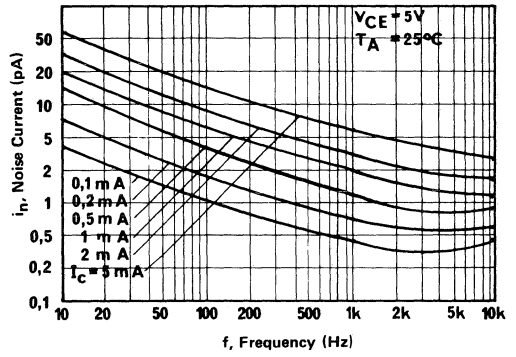


FIGURE 5. – WIDEBAND NOISE FIGURE.

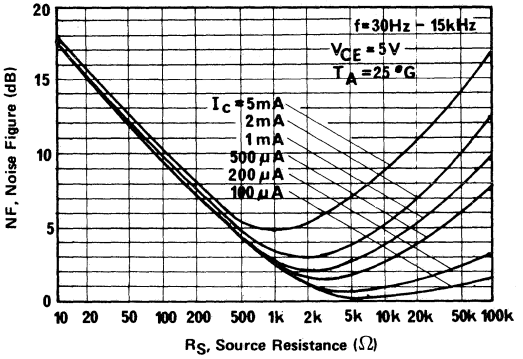


FIGURE 6. – TOTAL NOISE VOLTAGE (120 Hz).

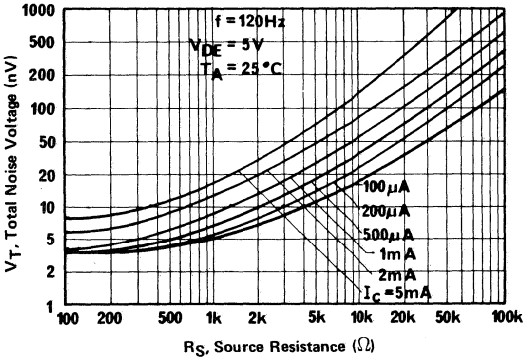


FIGURE 7. – NOISE FIGURE (120 Hz).

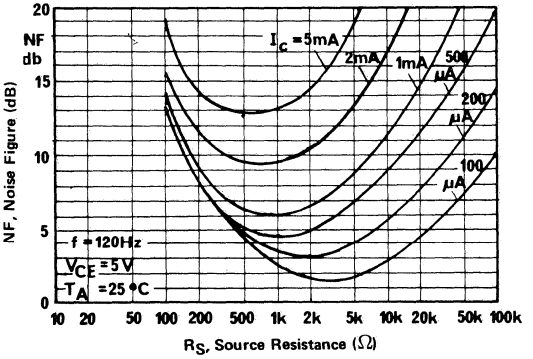


FIGURE 8. – NORMALIZED DC CURRENT GAIN.

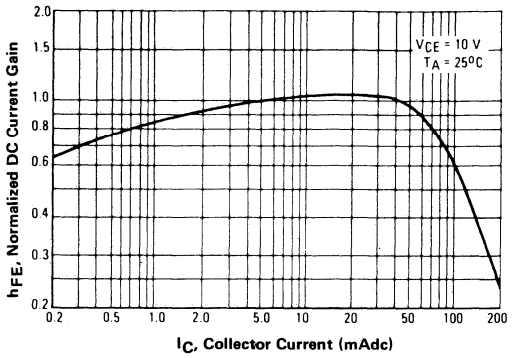


FIGURE 9. – "SATURATION" AND "ON" VOLTAGES.

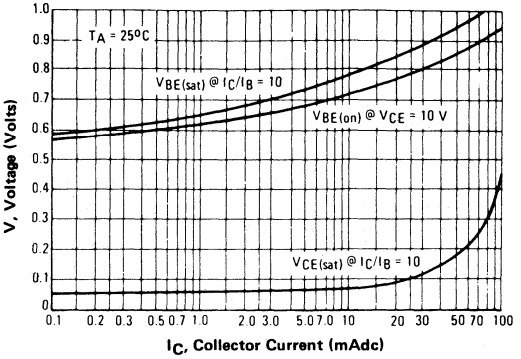


FIGURE 10. – CURRENT GAIN–BANDWIDTH PRODUCT.

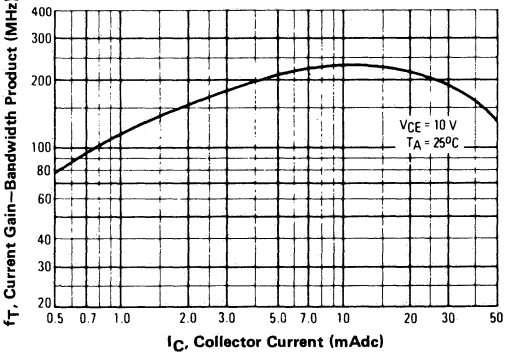


FIGURE 11. – CAPACITANCES.

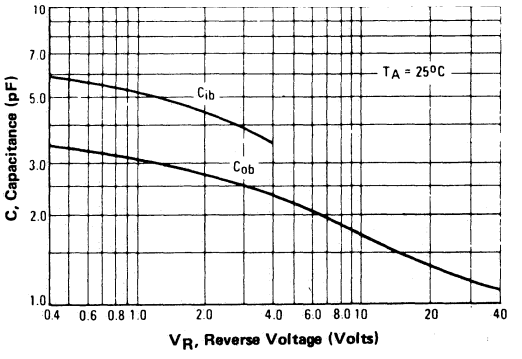


FIGURE 12. – OUTPUT ADMITTANCE.

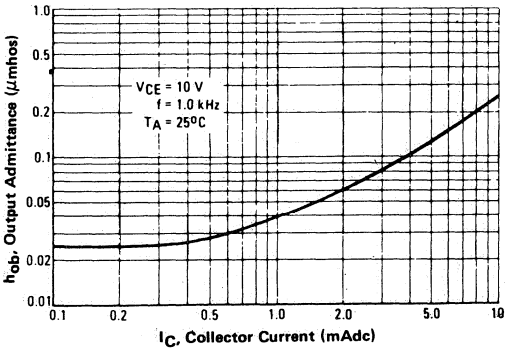
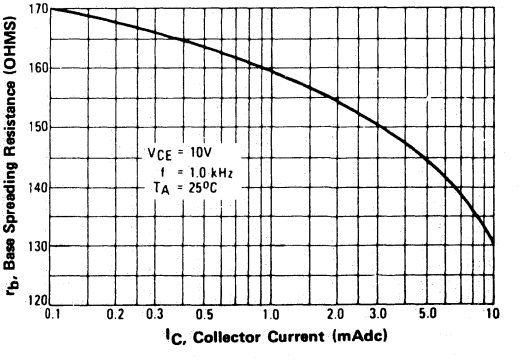


FIGURE 13. – BASE SPREADING RESISTANCE.



BC445
BC447 • BC449

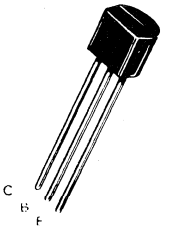
PNP SILICON ANNULAR* TRANSISTORS

... designed for use as high voltage driver and output transistors, particularly suitable as Power Darlington drivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) I_C = 1.0 mAdc — BC445
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC447
  = 100 Vdc (Min) I_C = 1.0 mAdc — BC449
- Excellent Current Gain Linearity — 1.0 mAdc to 100 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.25 Vdc (Max) I_C = 100 mAdc
- Available in standardized gain groups (A/B)

NPN SILICON

HIGH VOLTAGE TRANSISTORS



For standard package order BC445/447/449

For TO - 18 configuration order
BC445-18 BC447-18 BC449-18

For TO - 5 configuration order
BC445-5 BC447-5 BC449-5

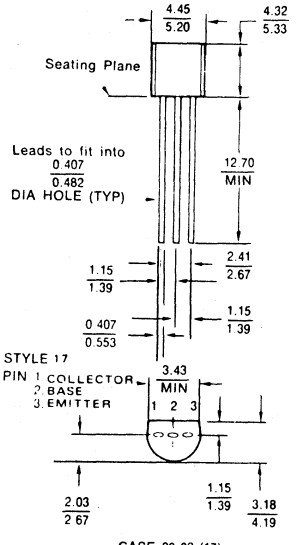
MAXIMUM RATINGS

Rating	Symbol	BC445	BC447	BC449	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector-Current-Continuous	I_C	300			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	83.3	°C/W
Thermal resistance, Junction to Ambient	Θ_{JA}	200	°C/W

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 1.0 mAdc, I_B = 0) BC445	BV_{CEO}	60	—	—	Vdc
BC447		80	—	—	
BC449		100	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0) BC445	BV_{CBO}	60	—	—	Vdc
BC447		80	—	—	
BC449		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC445		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC447		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC449		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain — I_C = 2mA, V_{CE} = 5V full range	h_{FE}	50		460	
A		120		220	
BC445/447 only B		180		460	
I_C = 10mA, V_{CE} = 5V full range		50			
A		100			
BC445/447 only B		160			
I_C = 100mA, V_{CE} = 5V full range		50			
A		60			
BC445/447 only B		90			
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	—	0.1	0.25	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	0.85	—	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	0.8	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	100	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.0	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	16	—	pF

* Pulse test - Pulse width ≤ 300 μs - Duty cycle 2%

FIG. 1 — DC CURRENT GAIN

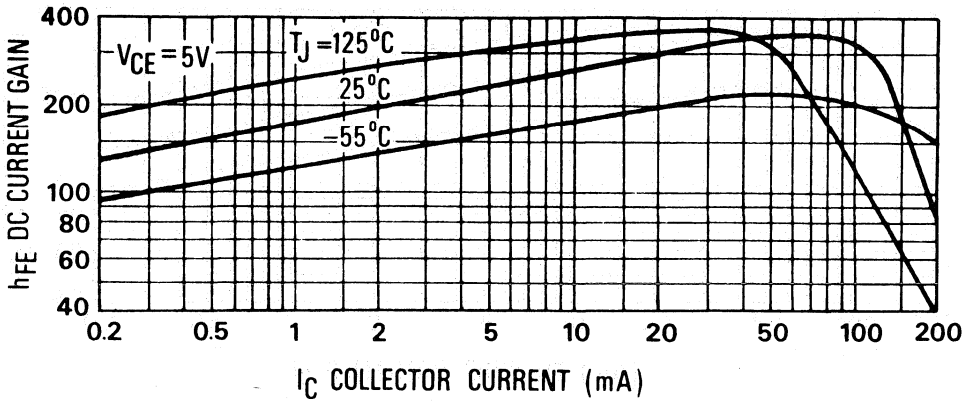


FIG. 2 — "ON" VOLTAGES

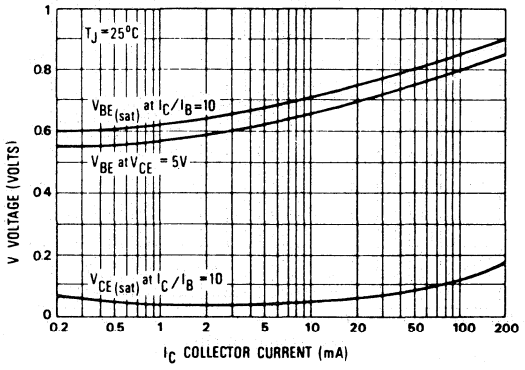


FIG. 3 — COLLECTOR SATURATION REGION

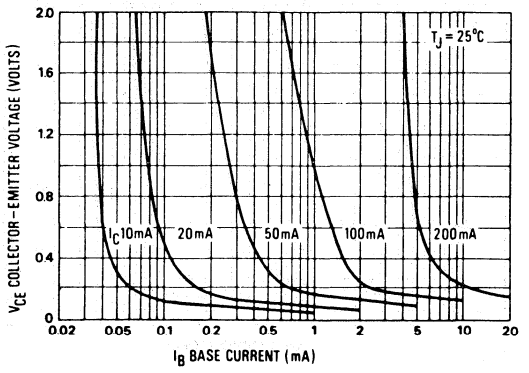


FIG. 4 — BASE-EMITTER TEMPERATURE COEFFICIENT

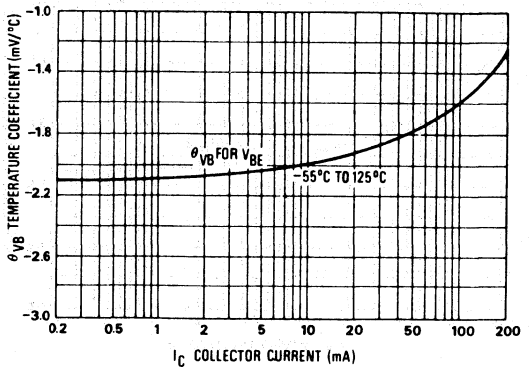


FIG. 5 — CURRENT GAIN — BANDWIDTH PRODUCT

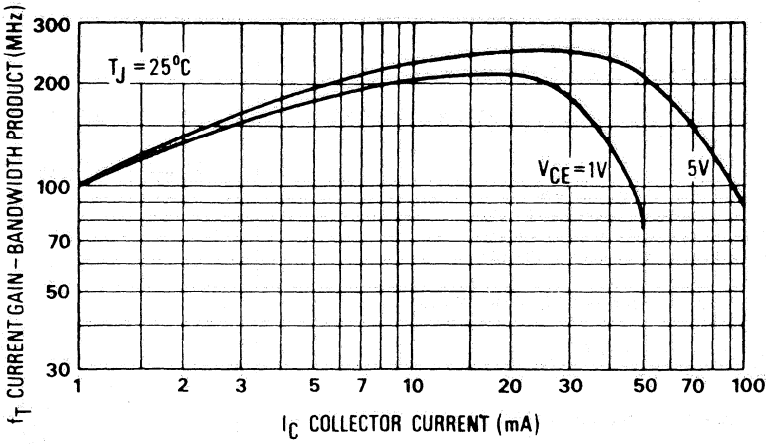
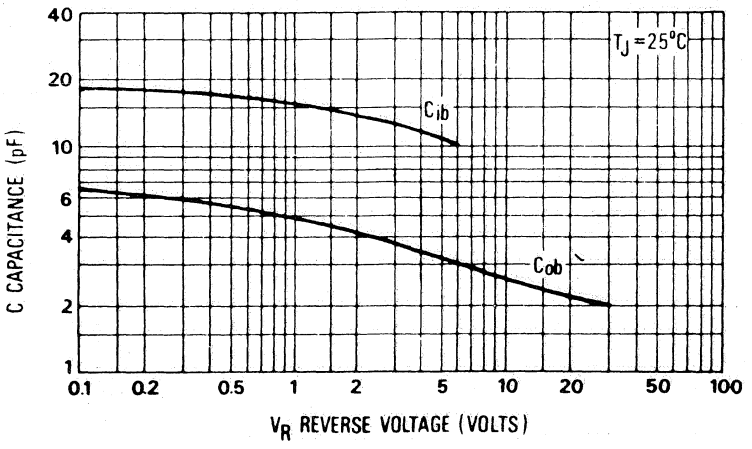


FIG. 6 — CAPACITANCE



BC446
BC448 • BC450

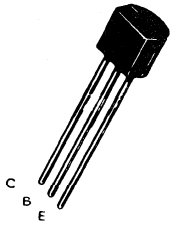
PNP SILICON ANNULAR* TRANSISTORS

... designed for use as high voltage driver and output transistors, particularly suitable as Power Darlington drivers.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 60 Vdc (Min) I_C = 1.0 mAdc — BC446
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC448
  = 100 Vdc (Min) I_C = 1.0 mAdc — BC450
- Excellent Current Gain Linearity — 1.0 mAdc to 100 mAdc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.25 Vdc (Max) I_C = 100 mAdc
- Available in standardized gain groups (A/B)

PNP SILICON

HIGH VOLTAGE TRANSISTORS



For standard package order BC446/BC448/BC450

For TO - 18 configuration order
BC446-18/BC448-18/BC450-18

For TO - 5 configuration order
BC446-5/BC448-5/BC450-5

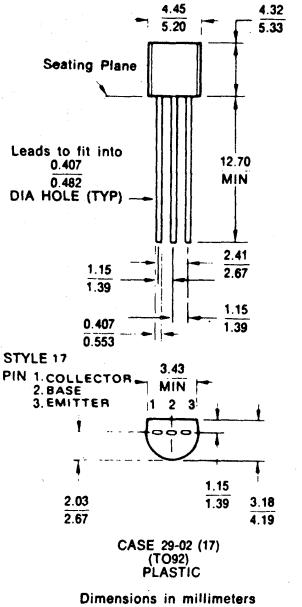
MAXIMUM RATINGS

Rating	Symbol	BC446	BC448	BC450	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector-Current-Continuous	I_C	300			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	83.3	°C/W
Thermal resistance, Junction to Ambient	Θ_{JA}	200	°C/W

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 1.0 mAdc, I_B = 0) BC446	BV_{CEO}	60	—	—	Vdc
BC448		80	—	—	
BC450		100	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0) BC446	BV_{CBO}	60	—	—	Vdc
BC448		80	—	—	
BC450		100	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC446		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC448		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC450		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain — I_C = 2mA, V_{CE} = 5V full range	h_{FE}	50		460	
A		120		220	
BC446/448 only B		180		460	
I_C = 10mA, V_{CE} = 5V full range		50			
A		100			
BC446/448 only B		160			
I_C = 100mA, V_{CE} = 5V full range		50			
A		60			
BC446/448 only B		90			
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	—	0.125	0.25	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	0.85	—	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	0.76	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	100	200	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.0	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	20	—	pF

* Pulse test - Pulse width ≤ 300 μs - Duty cycle 2 %

FIG. 1 — DC CURRENT GAIN

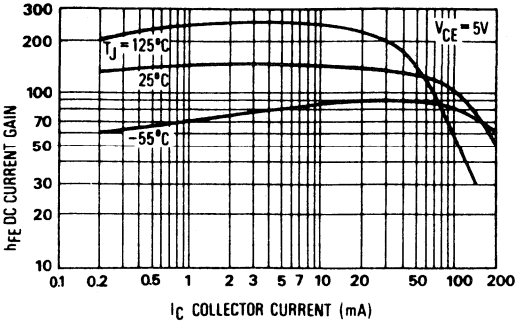


FIG. 2 — "ON" VOLTAGES

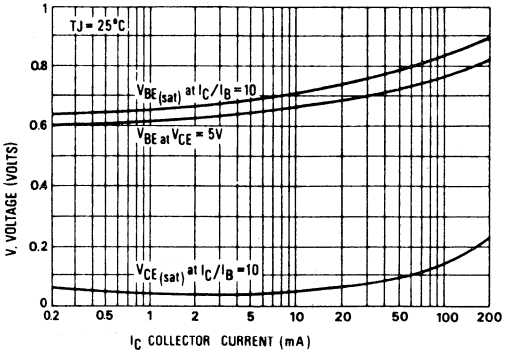


FIG. 3 — COLLECTOR SATURATION REGION

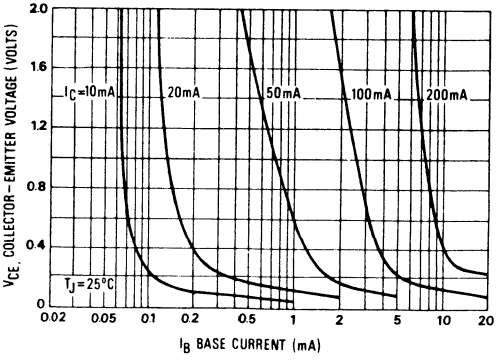


FIG. 4 — BASE-EMITTER TEMPERATURE COEFFICIENT

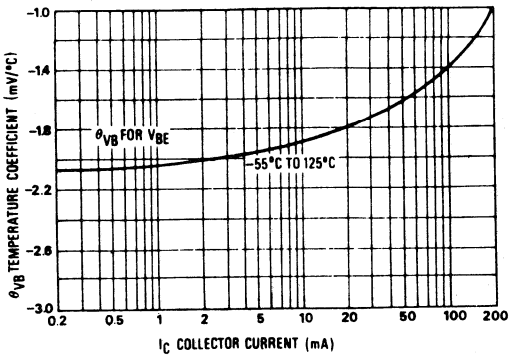


FIG. 5 — CAPACITANCE

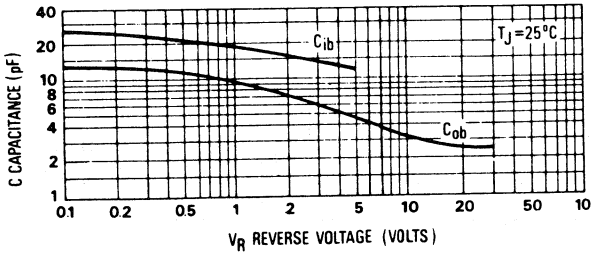
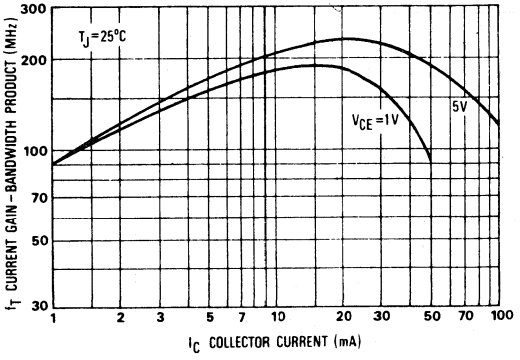


FIG. 6 — BANDWIDTH PRODUCT



BC485
BC487 • BC489

NPN SILICON ANNULAR* TRANSISTORS

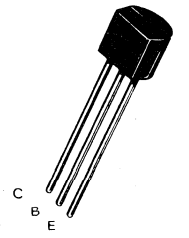
... designed for use as High Voltage-High Current driver and output transistors

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) I_C = 1.0 mAdc — BC485
  = 60 Vdc (Min) I_C = 1.0 mAdc — BC487
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC489
- Excellent Current-Gain Linearity — 1.0 mAdc to 100 mAdc
- Good h_{FE} up to 1 Amp.
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.2 Vdc (Typ) @ I_C = 500 mAdc
- Available in standardized gain groups (L/A/B)

NPN SILICON

HIGH VOLTAGE - HIGH CURRENT

TRANSISTORS



For standard package order BC485/BC487/BC489

For TO - 18 configuration order
BC485-18/BC487-18/BC489-18

For TO - 5 configuration order
BC485-5/BC487-5/BC489-5

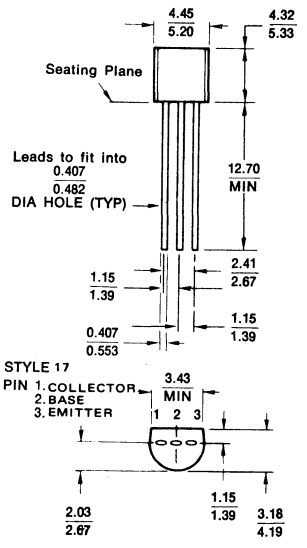
MAXIMUM RATINGS

Ratings	Symbol	BC485	BC487	BC489	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current-Continuous	I_C	1.0			Adc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	Θ_{JC}	0.083	°C/mW
Thermal Resistance, Junction to Ambient	* Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0) BC485	BV_{CEO}	45	—	—	Vdc
BC487		60	—	—	
BC489		80	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC485	BV_{CBO}	45	—	—	Vdc
BC487		60	—	—	
BC489		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC485		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC487		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC489		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain	h_{FE}				
I_C = 10 mAdc — V_{CE} = 2.0 Vdc		40			
I_C = 100 mAdc — V_{CE} = 2.0 Vdc					
Full Range		60		400	
— L		60	120	150	
— A		100	160	250	
— B		160	260	400	
I_C = 1 Ampdc — V_{CE} = 5.0 Vdc		15			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$				
I_C = 500 mAdc — I_B = 50 mAdc		—	0.2	0.50	Vdc
I_C = 1Adc — I_B = 100 mAdc		—	0.3	—	
Base Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	—	0.85	1.20	Vdc
I_C = 1 Ampdc — I_B = 100 mAdc			0.90		
DYNAMIC CHARACTERISTICS					
Current Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 2.0 Vdc, f= 100 MHz)	f_T	—	200	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	7	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	50	—	pF

* Pulse test - Pulse width = 300 μs - Duty cycle 2 %

FIG. 1 — ACTIVE REGION SAFE OPERATING AREA

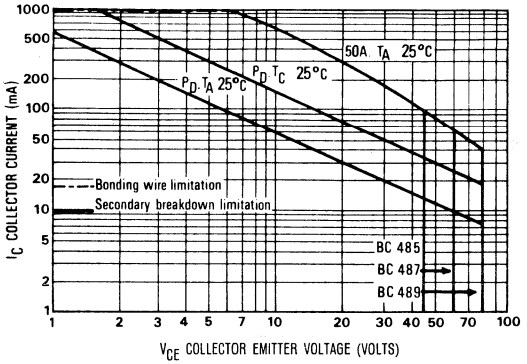


FIG. 2 — DC CURRENT GAIN

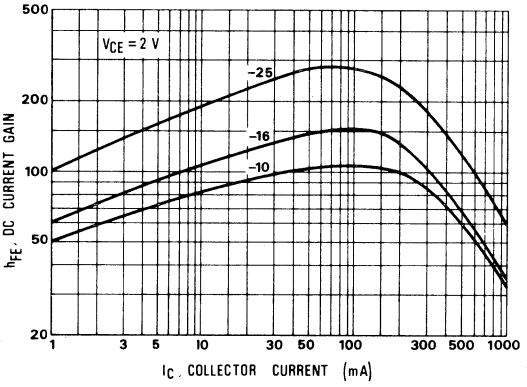


FIG. 3 — CURRENT GAIN BANDWIDTH PRODUCT

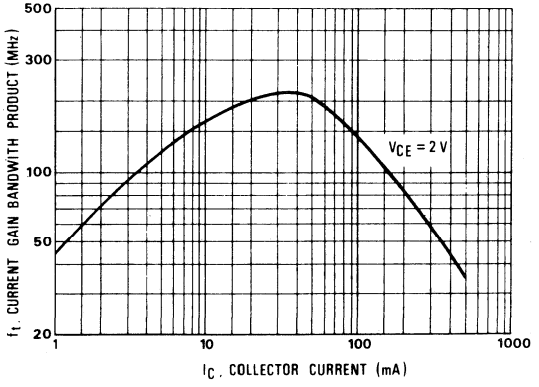


FIG. 4 — "SATURATION" AND "ON" VOLTAGES

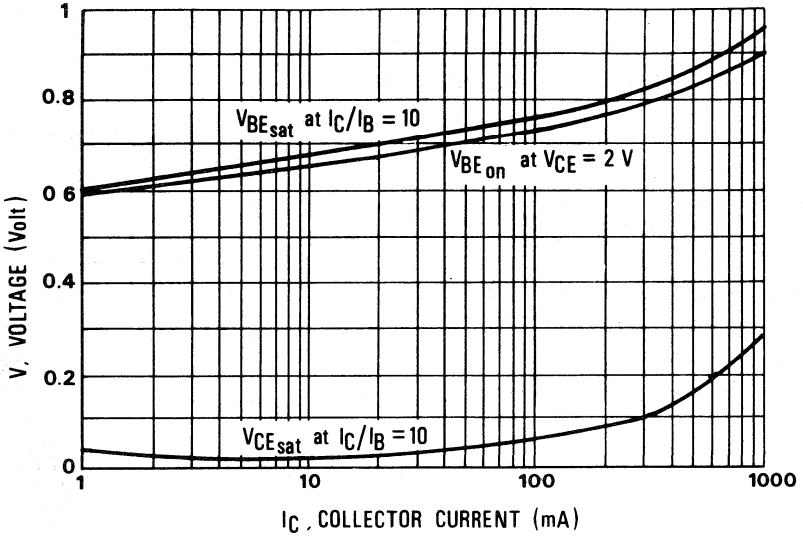
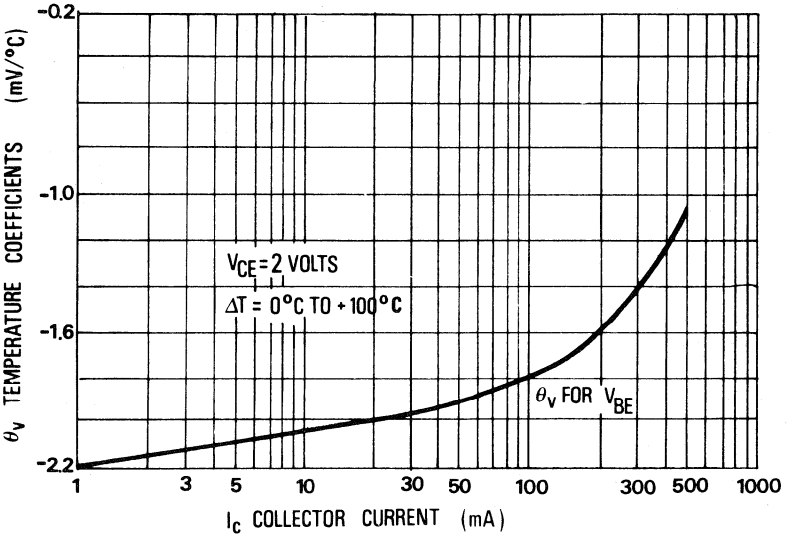


FIG. 5 — TEMPERATURE COEFFICIENTS



BC486
BC488 • BC490

PNP SILICON ANNULAR* TRANSISTORS

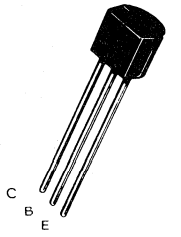
... designed for use as High Voltage-High Current driver and output transistors

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 45 Vdc (Min) I_C = 1.0 mAdc — BC 486
  = 60 Vdc (Min) I_C = 1.0 mAdc — BC 488
  = 80 Vdc (Min) I_C = 1.0 mAdc — BC 490
- Excellent Current-Gain Linearity — 1.0 mAdc to 100 mAdc
- Good h_{FE} up to 1 Amp.
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.2 Vdc (Typ) @ I_C = 500 mAdc
- Available in standardized gain groups (L/A/B)

PNP SILICON

HIGH VOLTAGE - HIGH CURRENT

TRANSISTORS



For standard package order BC486/BC488/BC490

For TO - 18 configuration order
BC486-18/BC488-18/BC490-18

For TO - 5 configuration order
BC486-5/BC488-5/BC490-5

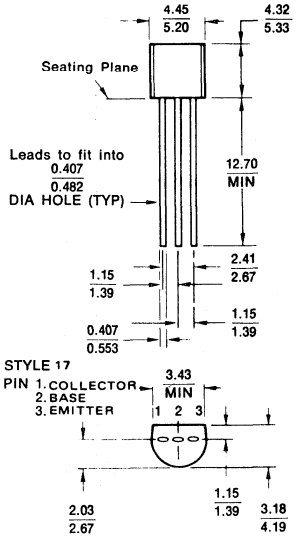
MAXIMUM RATINGS

Ratings	Symbol	BC486	BC488	BC490	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4			Vdc
Collector Current-Continuous	I_C	1.0			Adc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5.0			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12.0			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	—55 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	Θ_{JC}	0.083	°C/mW
Thermal Resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc



CASE 29-02 (17)
(TO92)
PLASTIC

Dimensions in millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0) BC486	BV_{CEO}	45	—	—	Vdc
BC488		60	—	—	
BC490		80	—	—	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0) BC486	BV_{CBO}	45	—	—	Vdc
BC488		60	—	—	
BC490		80	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	—	—	Vdc
Collector cutoff current	I_{CBO}				nAdc
V_{CB} = 30 Vdc — I_E = 0 BC486		—	—	100	
V_{CB} = 40 Vdc — I_E = 0 BC488		—	—	100	
V_{CB} = 60 Vdc — I_E = 0 BC490		—	—	100	
ON CHARACTERISTICS*					
DC Current Gain	h_{FE}				
I_C = 10 mAdc — V_{CE} = 2.0 Vdc		40			
I_C = 100 mAdc — V_{CE} = 2.0 Vdc					
Full Range		60	—	400	
— L		60	100	150	
— A		100	140	250	
— B		160	260	400	
I_C = 1 Ampdc — V_{CE} = 5.0 Vdc		15			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$				
I_C = 500 mAdc — I_B = 50 mAdc		—	0.25	0.50	Vdc
I_C = 1Adc — I_B = 100 mAdc		—	0.50	—	
Base Emitter Saturation Voltage	$V_{BE(sat)}$				
(I_C = 500 mAdc, I_B = 50 mAdc)		—	0.90	1.20	Vdc
I_C = 1 Ampdc — I_B = 100 mAdc			1.00		
DYNAMIC CHARACTERISTICS					
Current Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 2.0 Vdc, f= 100 MHz)	f_T	—	150	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	9	—	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	—	110	—	pF

* Pulse test - Pulse width = 300 μs - Duty cycle 2 %

FIG. 1 — ACTIVE REGION SAFE OPERATING AREA

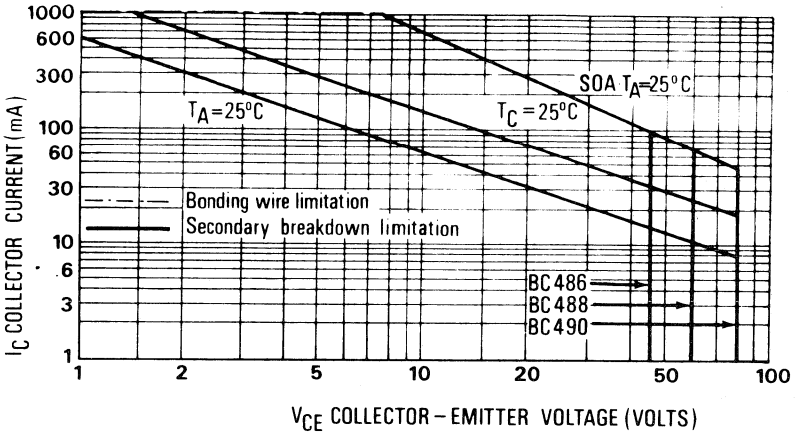


FIG. 2 — DC CURRENT GAIN

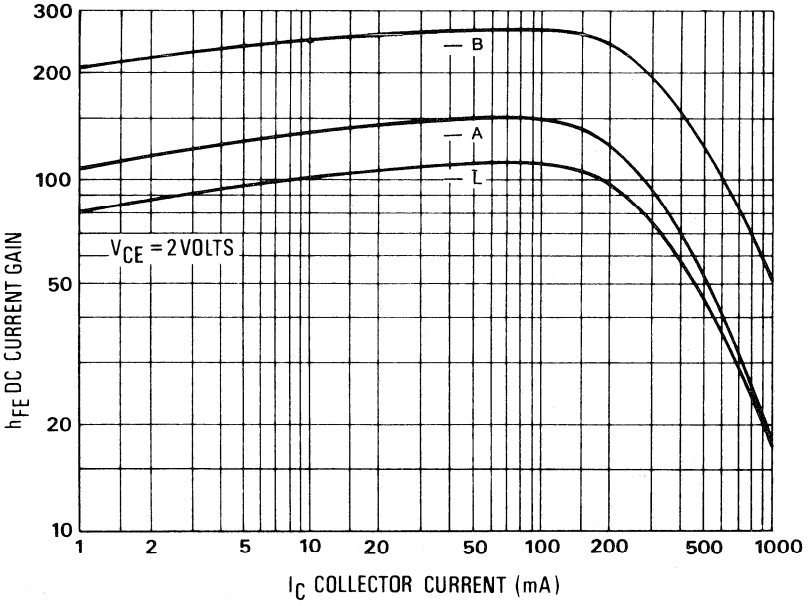


FIG. 3 — CURRENT GAIN BANDWIDTH PRODUCT

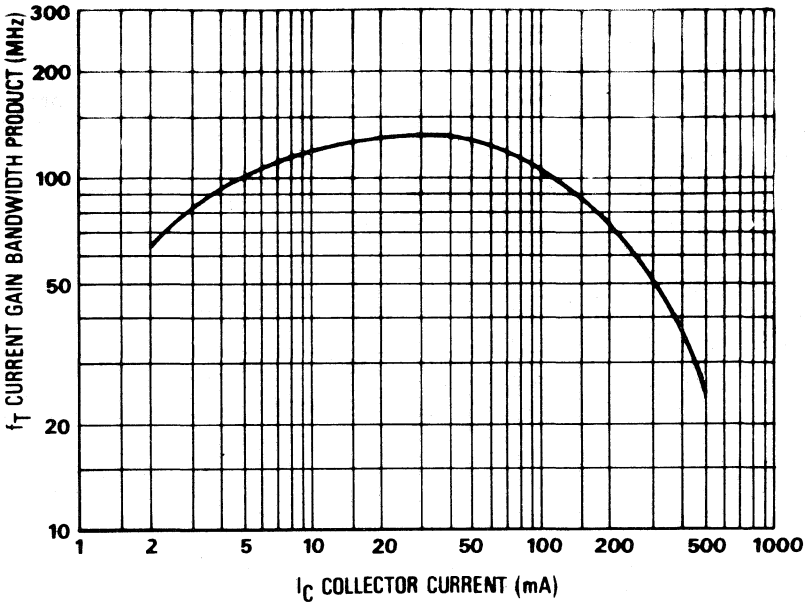


FIG. 4 — "SATURATION" AND "ON" VOLTAGES

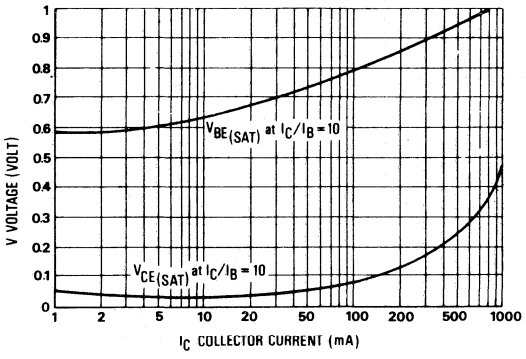
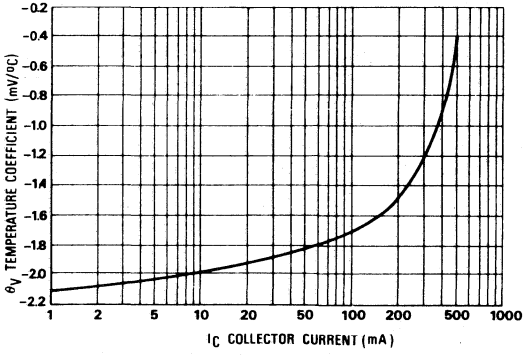


FIG. 5 — TEMPERATURE COEFFICIENTS



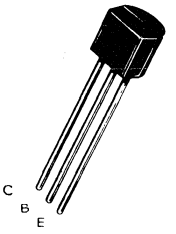
BC546
BC547 • BC548

NPN SILICON ANNULAR* TRANSISTORS

. . . designed for general-purpose use in audio, radio, and television applications.

- High Breakdown Voltage—
  BV_{CEO} = 65 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage—
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 100 mAdc
- Low output capacitance
  C_{ob} = 4.5 pf (Max) @ V_{CB} = 10 Vdc
- Complementary to PNP BC 556/557/558
- One-Piece, Injection-Molded Unibloc † Package

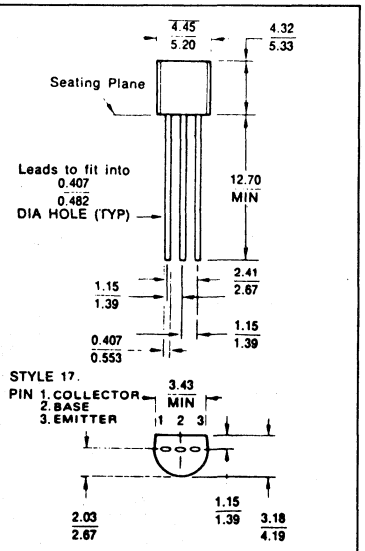
NPN SILICON AMPLIFIER TRANSISTORS



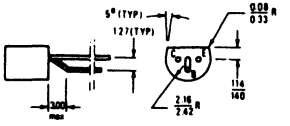
For standard package order BC546/547/548
For TO-18 configuration order BC546-18/547-18/548-18
For TO-5 configuration order BC546-5/547-5/548-5

MAXIMUM RATINGS

Rating	Symbol	BC546	BC547	BC548	Unit
Collector-Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector-Base Voltage	V_{CB}	80	50	30	Vdc
Emitter-Base Voltage	V_{EB}	6			Vdc
Collector-Current-Continuous Peak	I_C I_{CM}	100 200			mAdc
Base-Current peak	I_{BM}	200			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C



CASE 29-02 (17)
(TO92)
PLASTIC



TO - 18 configuration

Dimensions in millimeters

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW

* Annular Semiconductors patented by Motorola Inc

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	BC 546	BV_{CEO}	65			Vdc
	BC 547		45			
	BC 548		30			
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BC 546	BV_{EBO}	6			Vdc
	BC 547		6			
	BC 548		6			
Collector Cutoff Current		I_{CES}				ηAdc
(V_{CE} = 70 Vdc, V_{BE} = 0)	BC 546			0.20	15	
(V_{CE} = 50 Vdc, V_{BE} = 0)	BC 547			0.20	15	
(V_{CE} = 35 Vdc) V_{BE} = 0)	BC 548			0.20	15	
(V_{CE} = 30 V, T_A = 125 °C	BC 546				4	μAdc
	BC 547				4	
	BC 548				4	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				
(I_C = 10 μAdc, V_{CE} = 5 Vdc)	BC 546A/547A/548A			90		
	BC 546B/547B/548B			150		
	BC 548C			270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 546		120		450	
	BC 547		120		450	
	BC 548		120		800	
	BC 546A/547A/548A		120	180	220	
	BC 546B/547B/548B		200	290	450	
	BC 548C		420	520	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 546A/547A/548A			120		
	BC 546B/547B/548B			180		
	BC 548C			300		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.5 mA)				0.09	0.25	
(I_C = 100 mAdc, I_B = 5 mAdc)				0.2	0.60	
(I_C = 10 mA, I_B = See Note 1)				0.3	0.6	
Base Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.5 mA)				0.7		
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55		0.70	
(I_C = 10 mAdc, V_{CE} = 5 Vdc)					0.77	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V.

FIGURE 1 – NORMALIZED DC CURRENT GAIN

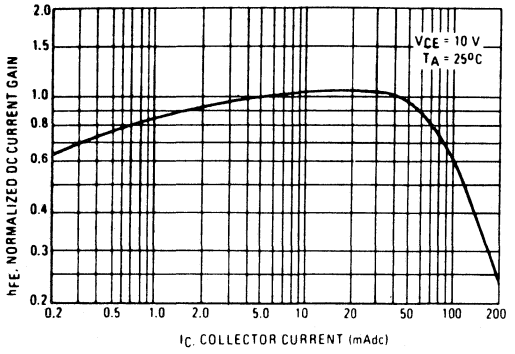


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

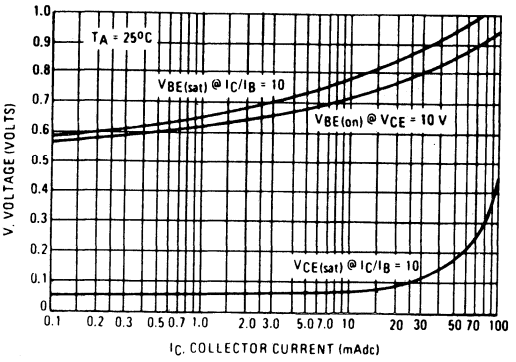


FIGURE 3 – COLLECTOR SATURATION REGION

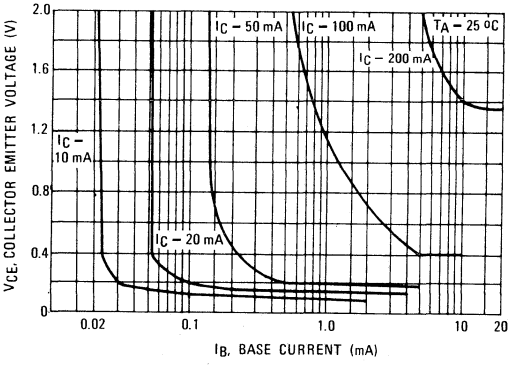


FIGURE 4 – BASE EMITTER TEMPERATURE COEFFICIENT

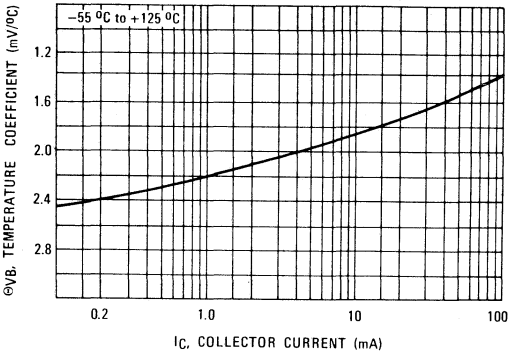


FIGURE 5 – CAPACITANCES

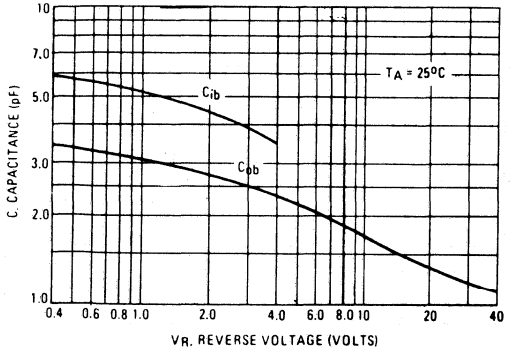


FIGURE 6 – CURRENT GAIN–BANDWIDTH PRODUCT

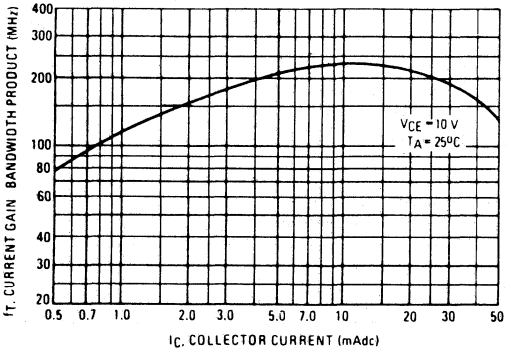


FIGURE 7 – DC CURRENT GAIN

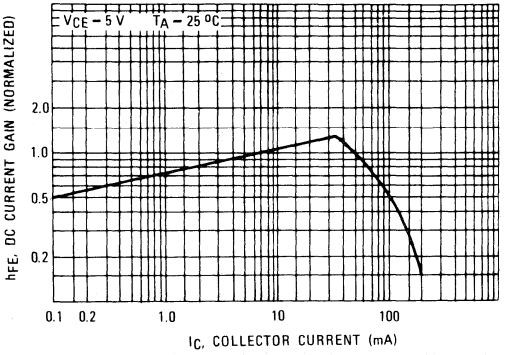


FIGURE 8 – "ON" VOLTAGE

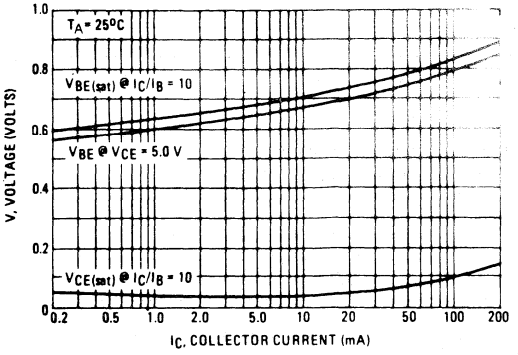


FIGURE 9 – COLLECTOR SATURATION REGION

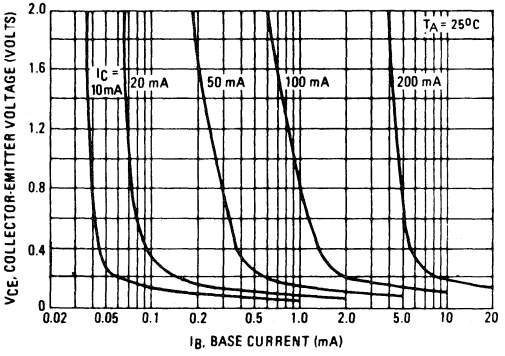


FIGURE 10 – BASE EMITTER TEMPERATURE COEFFICIENT

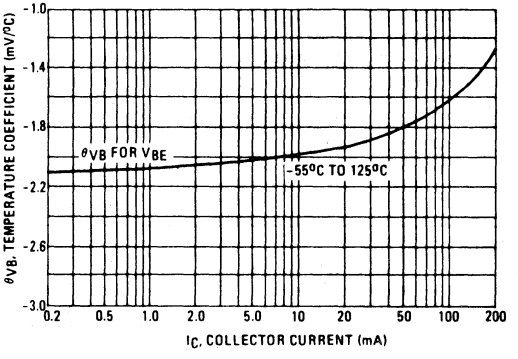


FIGURE 11 – CAPACITANCE

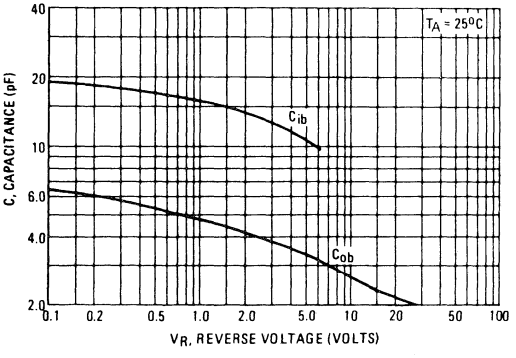
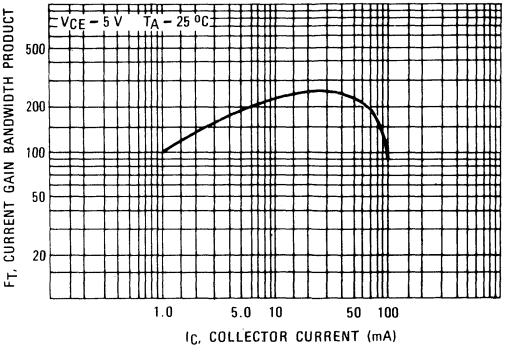


FIGURE 12 – CURRENT GAIN–BANDWIDTH PRODUCT



DYNAMIC CHARACTERISTICS, SMALL SIGNAL CHARACTERISTICS

Characteristics	Type	Symbol	Min	Typ	Max	Unit
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	 BC 546 BC 547 BC 548	f_T	 150 150 150	 300 300 300		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 1 MHz)		C_{ob}		1.7	4.5	pF
Input capacitance (V_{BE} = 0.5 V, I_C = 0, f = 1 MHz)		C_{ib}		10		pF
Input Impedance (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	 BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{ie}(h11e)	 1.6 3.2 6.0	 2.7 4.5 8.7	 4.5 8.5 15.0	K ohm
Voltage Feedback Ratio (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	 BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{re}(h12e)		 1.5 2.0 3.0		$X10^{-4}$
Small-Signal Current Gain (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	 BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{fe}(h21e)	 125 240 450	 220 330 600	 260 500 900	
Output Admittance (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)	 BC 546A/547A/548A BC 546B/547B/548B BC 548C	h_{oe}(h22e)		 8 10 12	 25 35 50	μ mhos
Noise Figure (I_C = 0.2 mAdc, V_{CE} = 5 Vdc, R_S = 2 Kohms, f = 1 KHz, Δf = 200 Hz)	 BC 546 BC 547 BC 548	NF		 2 2 2	 10 10 10	dB

FIGURE 13 – THERMAL RESPONSE

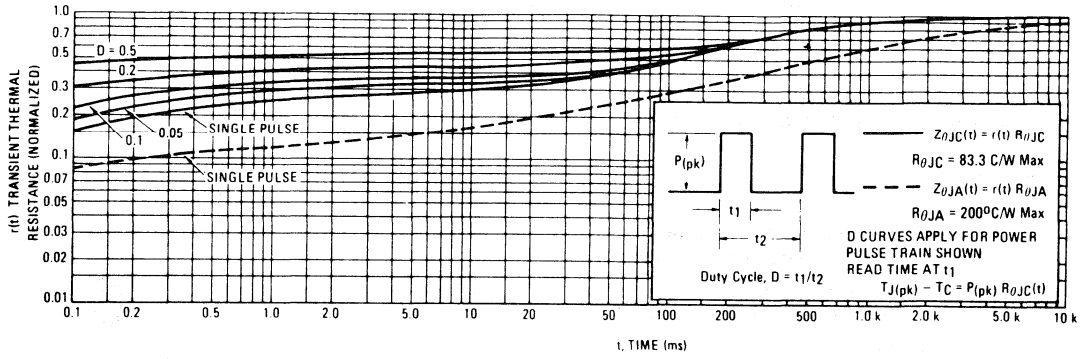
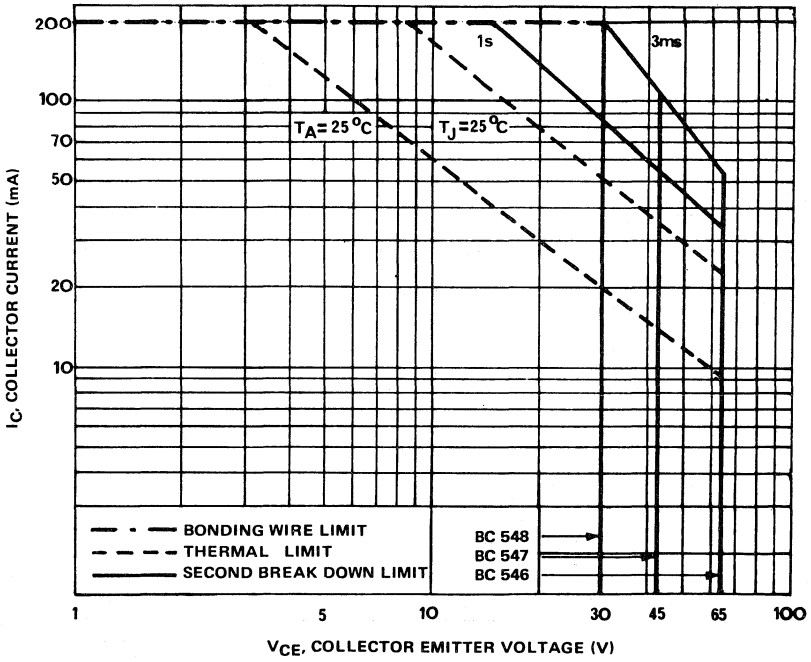


FIGURE 14 – ACTIVE REGION SAFE OPERATING AREA



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

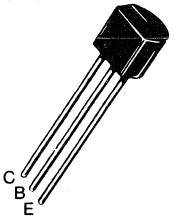
The data of Figure 14 is based upon $T_{J(pk)}$=150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data of Figure 13. At high case or ambient temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (see AN 415).

BC549
BC550

NPN SILICON ANNULAR♦ LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  N_F = 2.5 dB max (30 Hz-15 KHz)
- Low Noise At Low Frequency
  V_T = 12 nV/√ Hz max (120 Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  (2 mA/5 V)
- Full Applications Information

NPN SILICON LOW NOISE TRANSISTOR



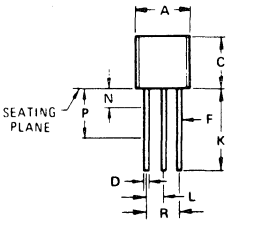
MAXIMUM RATINGS

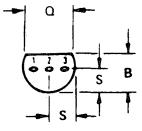
Rating	Symbol	Value BC549	Value BC550	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	625 5		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦Annular Semiconductors Patented by Motorola Inc.





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

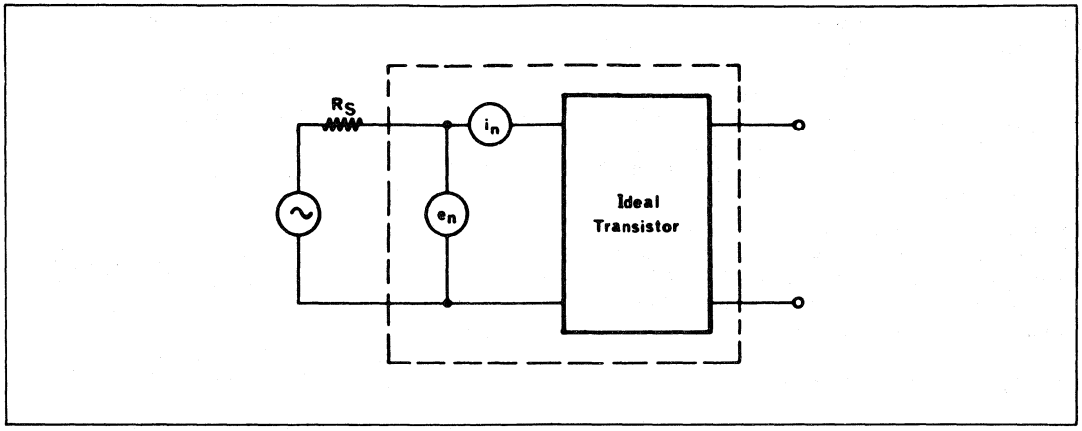
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0) BC549	BV_{CEO}	30			Vdc
BC550		45			
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0) BC549	BV_{CBO}	45			Vdc
BC550		50			
Emitter-Base Breakdown Voltage (I_C = 10 μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30 Vdc, I_E = 0, T_A = + 125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4 Vdc, I_C = 0)	I_{EBO}			15	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 μAdc, V_{CE} = 5 Vdc) BC549B/550B	h_{FE}	100	150		
BC549C/550C		100	270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc) BC549B/550B		180	290	460	
BC549C/550C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)			0.075	0.25	
(I_C = 10 mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100 mAdc, I_B = 5 mAdc, see note 2)			0.25	0.6	
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 5 mAdc)	VBE(S)		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10 μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100 μAdc, V_{CE} = 5 Vdc)			0.55		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V
Note 2: Pulse test = 300 μs; Duty Cycle = 2 %

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cbo}		2.5		pF
h-PARAMETERS (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)					
Input Impedance BC549B/BC550B BC549C/BC550C	h_{ie}, (h_{11e})	 3.2 6.0	 6.0 8.7	 8.5 15.0	KΩ
Voltage Feedback Ratio BC549B/BC550B BC549C/BC560C	h_{re} (h_{12e})		 2.0 3.0		10^{-4}
Small Signal Current Gain BC549B/BC550B BC549C/BC550C	h_{fe} (h_{21e})	 240 450	 330 600	 500 900	
Output Admittance BC549B/BC550B BC549C/BC550C	h_{oe} (h_{22e})		 10 12	 60 110	μmhos
NOISE PERFORMANCE					
Noise Figure (I_C = 200 μAdc, V_{CE} = 5 Vdc, R_S = 2 KΩ, f = 30 Hz – 15 KHz)	N_F		0.6	2.5	dB
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2 KΩ, f = 120 Hz) See Application note, Section I	V_T		8.0	12	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2KΩ, f = 10 Hz – 50 Hz) See Application note, Section II	V_T		74	135	$nV/\sqrt{Hz}$

FIGURE 1 – TRANSISTOR NOISE MODEL



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)
e_n = noise voltage of the transistor referred to the input (figures 2 & 3)
i_n = noise current of the transistor referred to the input (figure 4)
K = Boltzmann's constant (1.38×10^{-23} j/°K)
T = Temperature of the source resistance (°K)
R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC550 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120 Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n 4.5 nV/$\sqrt{Hz}$ from figure 3 (Note that this is for a one cycle bandwidth)
Read i_n 5.8 pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})^2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})^2.(1 \times 10^3)^2]^{1/2}$$

Thus: $\boxed{V_T = 8.2\ nV}$

This checks with the value of 8 nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7.

To minimize noise in a transistor stage, one might use figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\triangle f = 1$ Hz), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 =$ 10 Hz, $f_2 = 50$ Hz at $I_C = 200\ \mu A$ and $R_S = 2\ K\Omega$
This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)^2\ df$$

$(f_1 - f_2)$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4\ KT\ R_S + i_{n(f)}^2\ R_S^2$$

$e_{n(f)}$ and $4\ KT\ R_S$ are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f}$$ (1/f noise spectrum density)

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$
$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\ KT\ R_S) \times (f_2-f_1) + R_S^2\ i_{n(f1)}^2 \times f1 \times i_{n(f1)} \frac{f2}{f1}$$

Now:
$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)
$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\ (10\ Hz–50\ Hz) = [(25 + 33.1)\ 40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10\ Hz–50\ Hz) = 74\ nV}$

FIGURE 2 – NOISE VOLTAGE vs FREQUENCY

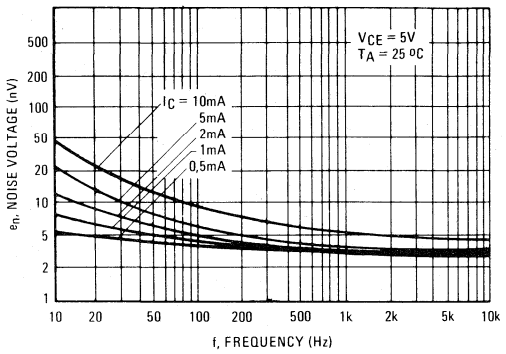


FIGURE 3 – NOISE VOLTAGE vs COLLECTOR CURRENT

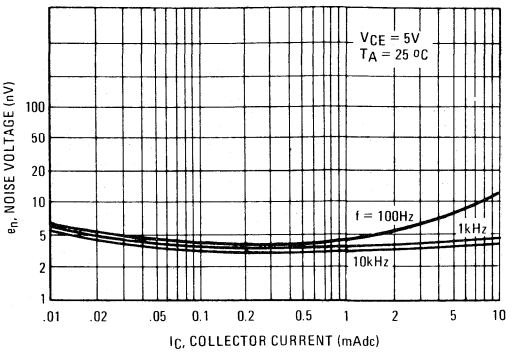
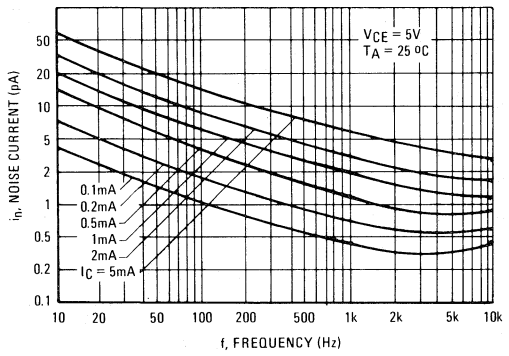


FIGURE 4 – NOISE CURRENT



• FIGURE 5 – WIDEBAND NOISE FIGURE

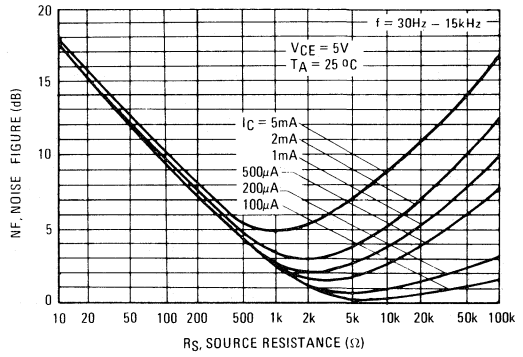


FIGURE 6 – TOTAL NOISE VOLTAGE (120 Hz)

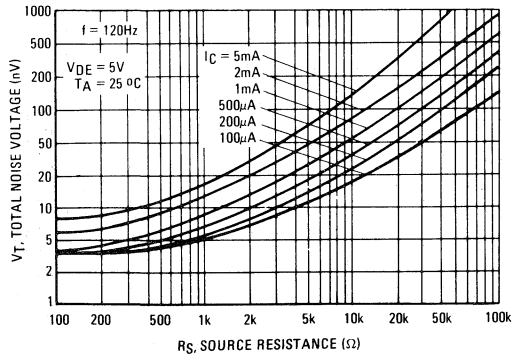


FIGURE 7 – NOISE FIGURE (120 Hz)

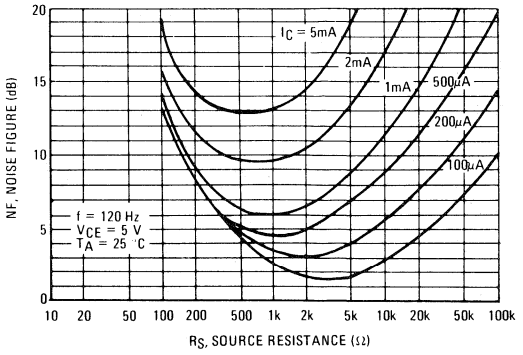


FIGURE 8 – NORMALIZED DC CURRENT GAIN

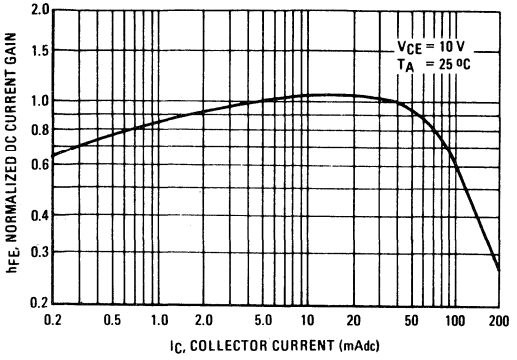


FIGURE 9 – "SATURATION" AND "ON" VOLTAGES

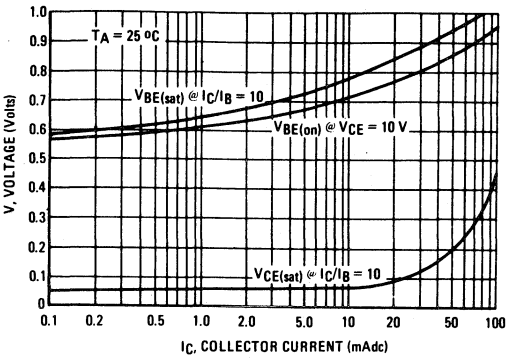


FIGURE 10 – CURRENT GAIN-BANDWIDTH PRODUCT

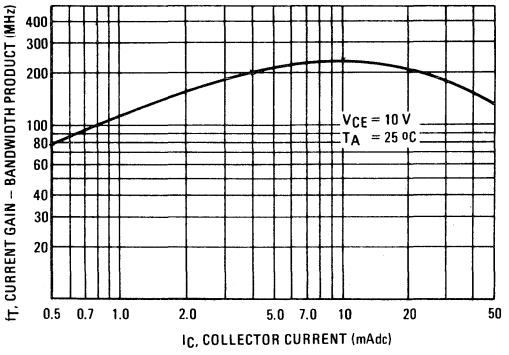


FIGURE 11 – CAPACITANCE

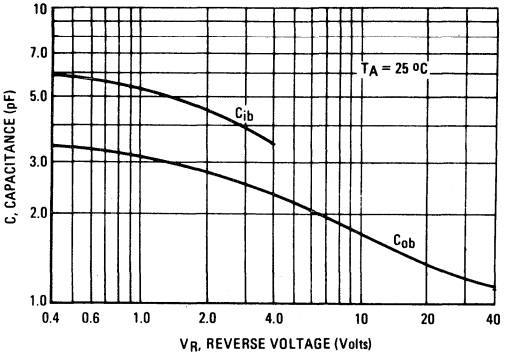


FIGURE 12 – OUTPUT ADMITTANCE

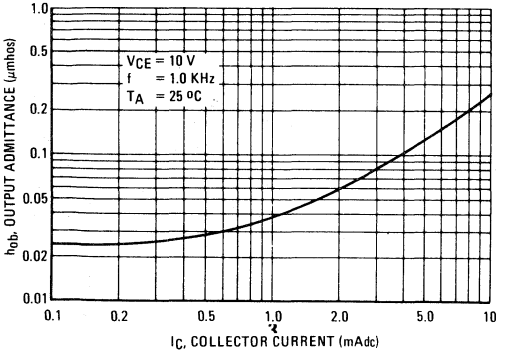
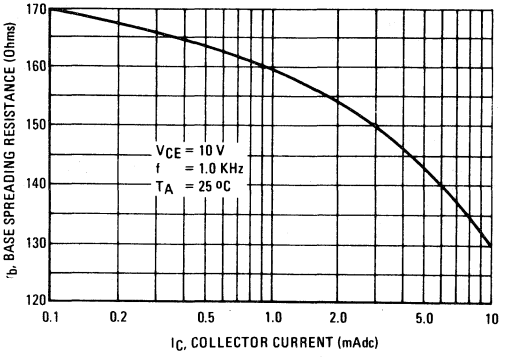


FIGURE 13 – BASE SPREADING RESISTANCE



BC556
BC557 • BC558

PNP SILICON ANNULAR* TRANSISTORS

. . . designed for general purpose use in audio, radio, and television applications.

- **High Breakdown Voltage—**

  BV_{CEO} = 65 Vdc (Min) @ I_C = 1.0 mAdc

- **Low Collector-Emitter Saturation Voltage—**

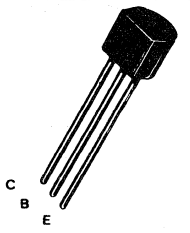
  $V_{CE\ (sat)}$ = 0.25 Vdc (Typ) @ I_C = 100 mAdc

- **Low output capacitance**

  C_{ob} = 6.0 pF (Max) @ V_{CB} = 10 Vdc

- **Complementary to NPN BC546/547/548**
- **One-Piece, Injection-Molded Unibloc† Package**

PNP SILICON AMPLIFIER TRANSISTORS



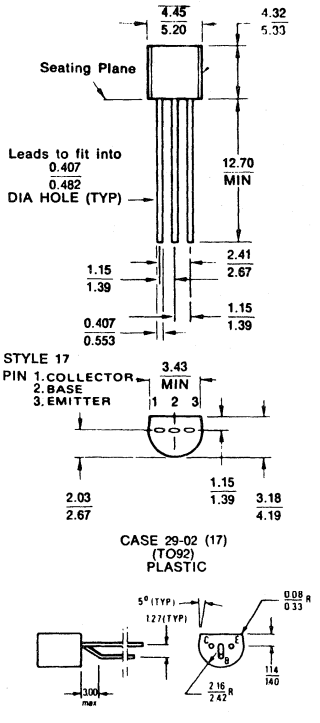
For standard package order BC556/557/558
For TO-18 configuration order BC556-18/557-18/558-18
For TO-5 configuration order BC556-5/557-5/558-5

MAXIMUM RATINGS

Rating	Symbol	BC556	BC557	BC558	Unit
Collector-Emitter Voltage	V_{CEO}	65	45	30	Vdc
Collector-Base Voltage	V_{CB}	80	50	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector-Current-Continuous Peak	I_C I_{CM}	100 200			mAdc
Base-Current peak	I_{BM}	200			mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	625 5			mW mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	1.5 12			W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to case	Θ_{JC}	0.083	°C/mW
Thermal resistance, Junction to Ambient	Θ_{JA}	0.20	°C/mW



* Annular Semiconductors Patented by Motorola Inc.
† Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BC 556 BC 557 BC 558	BV_{CEO}	65 45 30	– – –	– – –	Vdc
Emitter-Base Breakdown Voltage (I_E = 100μAdc, I_C = 0)	BC 556 BC 557 BC 558	BV_{EBO}	5 5 5	– – –	– – –	Vdc
Collector-Emitter Leakage Current		I_{CES}				
V_{CES} = 40 V	BC 556		–	2	100	nA
V_{CES} = 20 V	BC 557 BC 558		– –	2 2	100 100	
V_{CES} = 20 V, T_A = 125 °C	BC 556 BC 557 BC 558		– – –	– – –	4 4 4	μA
DC Current Gain		h_{FE}				
(I_C = 10 μ Adc, V_{CE} = 5 Vdc)	BC 556A/557A/558A		–	90	–	
	BC 556B/557B/558B		–	150	–	
	BC 557C/558C		–	270	–	
(I_C = 2 mAdc, V_{CE} = 5 Vdc)	BC 556		120	–	450	
	BC 557		120	–	450	
	BC 558		120	–	800	
	BC 556A/557A/558A		120	170	220	
	BC 556B/557B/558B		180	290	460	
	BC 557C/558C		380	500	800	
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	BC 556A/557A/558A		–	120	–	
	BC 556B/557B/558B		–	180	–	
	BC557C/558C		–	300	–	
Collector-Emitter Saturation Voltage		V_{CE} (sat)				
(I_C = 10 mAdc, I_B = 0,5 mAdc)			–	0.075	0.3	Vdc
(I_C = 10 mAdc, I_B = see Note 1)			–	0.30	0.60	
(I_C = 100 mAdc, I_B = 5 mAdc)			–	0.25	0.65	
Base-Emitter Saturation Voltage		V_{BE} (sat)				
(I_C = 10 mAdc, I_B = 0.5 mAdc)			–	0.70	–	Vdc
(I_C = 100 mAdc, I_B = 5 mAdc)			–	1.00	–	
Base-Emitter on Voltage		V_{BE} (on)				Vdc
(I_C = 2 mAdc, V_{CE} = 5 Vdc)			0.55	0.62	0.70	
I_C = 10 mA, V_{CE} = 5 Vdc				0.7	0.82	

Note 1 : I_C = 10 mAdc on the constant base current characteristic, which yields the point I_C = 11 mAdc, V_{CE} = 1 V

FIGURE 1 – NORMALIZED DC CURRENT GAIN

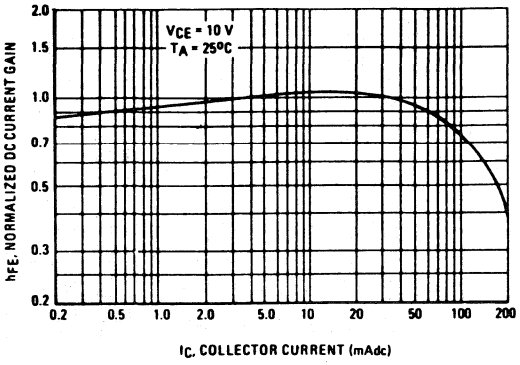


FIGURE 2 – "SATURATION" AND "ON" VOLTAGES

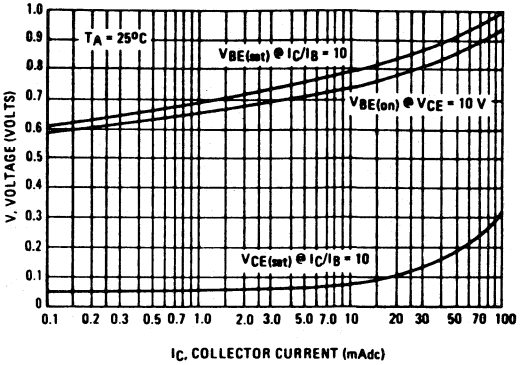


FIGURE 3 – COLLECTOR SATURATION REGION

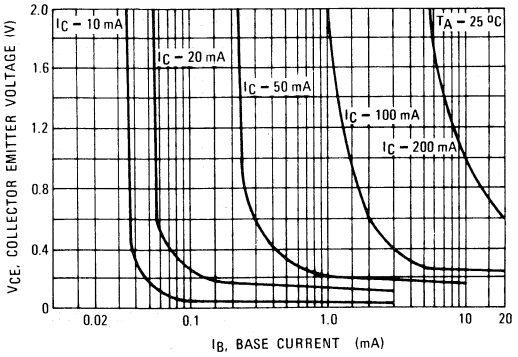


FIGURE 4 – BASE EMITTER TEMPERATURE COEFFICIENT

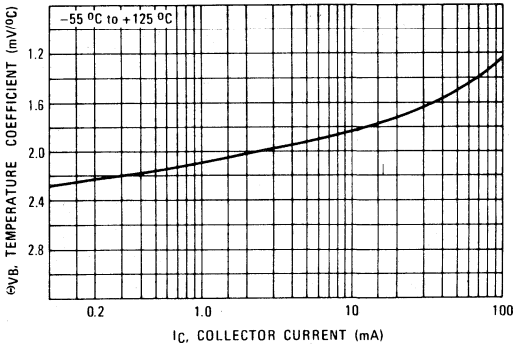


FIGURE 5 – CAPACITANCES

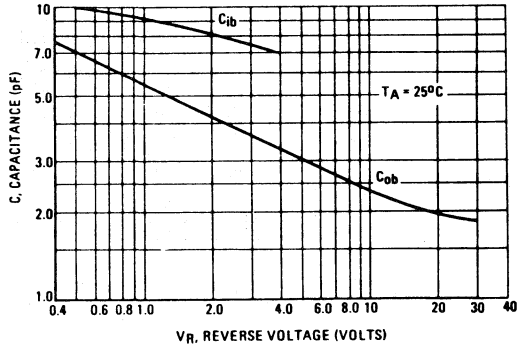


FIGURE 6 – CURRENT GAIN–BANDWIDTH PRODUCT

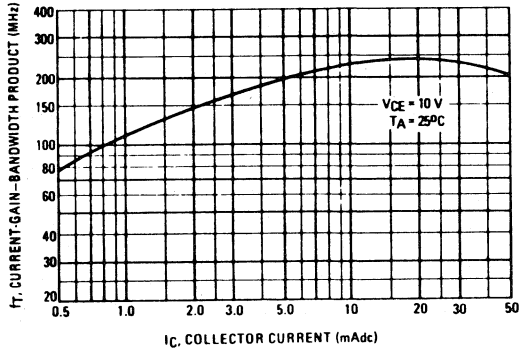


FIGURE 7 – DC CURRENT GAIN

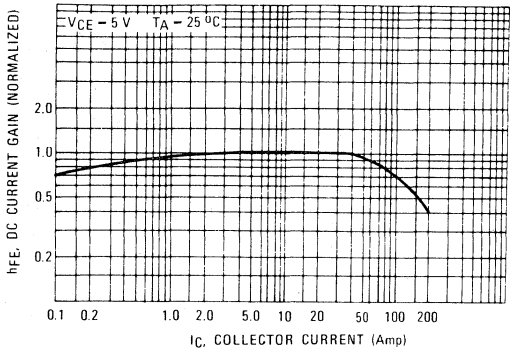


FIGURE 8 – "ON" VOLTAGE

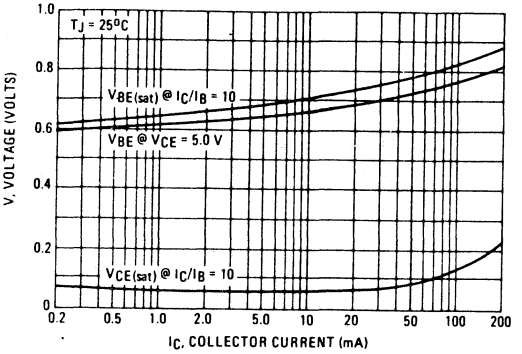


FIGURE 9 – COLLECTOR SATURATION REGION

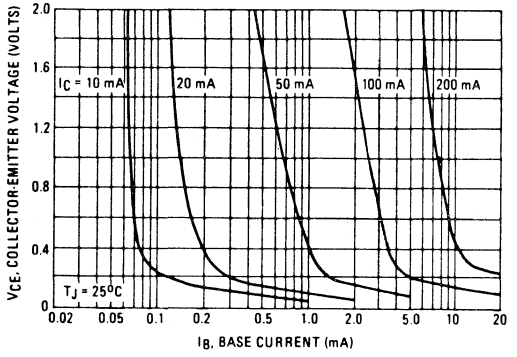


FIGURE 10 – BASE EMITTER TEMPERATURE COEFFICIENT

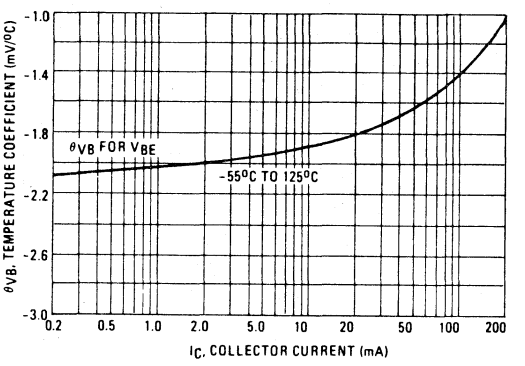


FIGURE 11 – CAPACITANCE

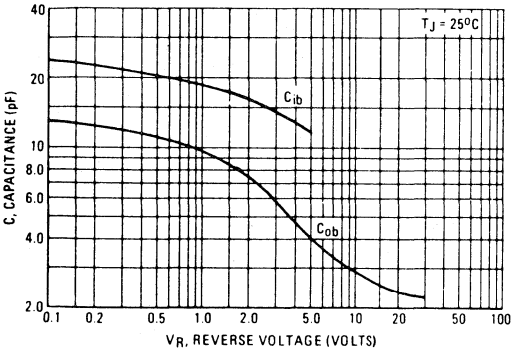
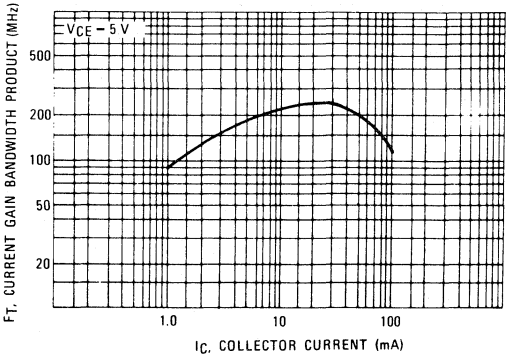


FIGURE 12 – CURRENT GAIN–BANDWIDTH PRODUCT



DYNAMIC CHARACTERISTICS / SMALL SIGNAL CHARACTERISTICS

Characteristic	Type	Symbol	Min	Typ	Max	Unit
Current-Gain – Bandwidth Product (I_C= 10 mAdc, V_{CE}= 5 Vdc, f = 50 MHz)		f_T				MHz
	BC 556		–	280	–	
	BC 557		–	320	–	
	BC 558		–	360	–	
Output Capacitance (V_{CB}= 10 Vdc, I_C= 0, f = 1 MHz)		C_{ob}	–	3	6.0	pF
Noise Figure (I_C= 0,2 mAdc, V_{CE}= 5 Vdc, R_S= 2 Kohms, f = 1 KHz, f = 200 Hz)		NF				dB
	BC 556		–	2	10	
	BC 557		–	2	10	
	BC 558		–	2	10	
Input Impedance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{ie}(h_{11e})$				kΩ
	BC 556A/557A/558A		1.2	2.7	4.5	
	BC 556B/557B/558B		3.0	4.5	8.0	
	BC 557C/558C		5.0	8.0	14.0	
Voltage Feedback Ratio (I_C= 2 mAdc, V_{CE}= 5 Vdc, f = 1 KHz)		$h_{re}(h_{12e})$				10^{-4}
	BC 556A/557A/558A		–	3.0	–	
	BC 556B/557B/558B		–	3.5	–	
	BC 557C/558C		–	4.0	–	
Small Signal Current Gain (I_C= 2 mAdc, V_{CE}= 5 Vdc f = 1 KHz)		$h_{fe}(h_{21e})$				–
	BC 556A/557A/558A		125	220	260	
	BC 556B/557B/558B		240	330	500	
	BC 557C/558C		450	600	900	
Output Admittance (I_C= 2 mAdc, V_{CE}= 5 Vdc, f= 1 KHz)		$h_{oe}(h_{22e})$				μmhos
	BC 556A/557A/558A		–	25	50	
	BC 556B/557B/558B		–	30	70	
	BC 557C/558C		–	60	110	

FIGURE 13 – THERMAL RESPONSE

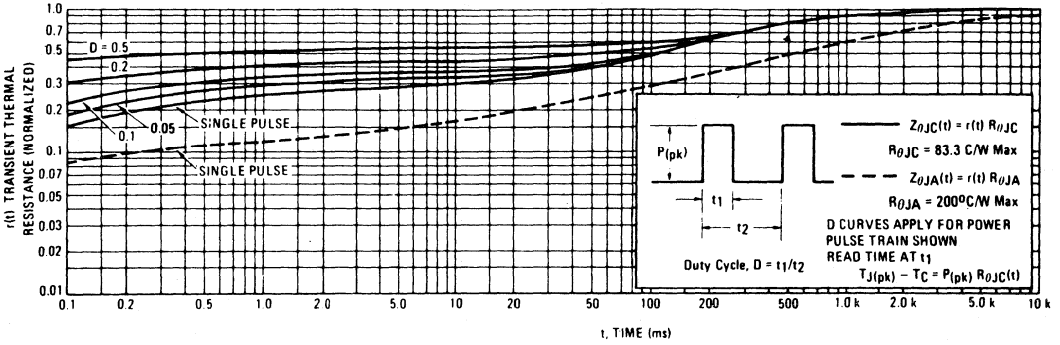
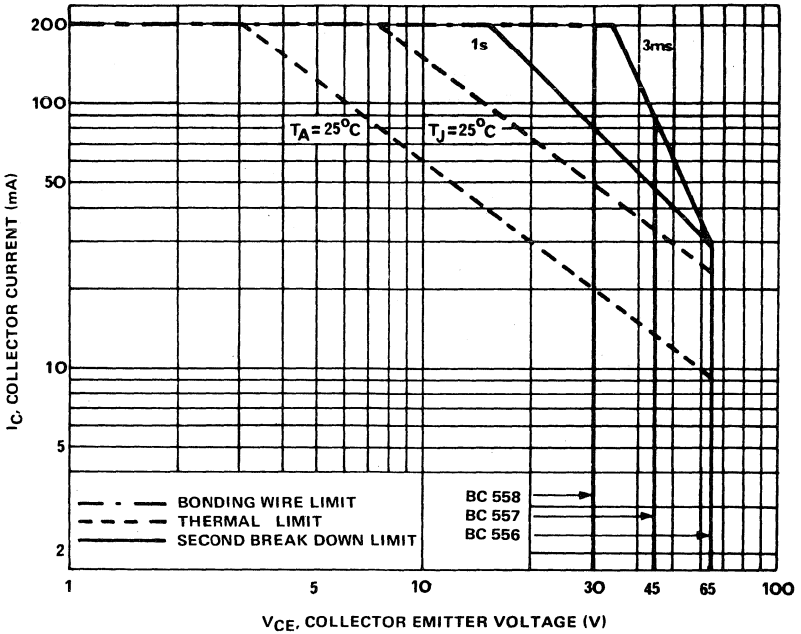


FIGURE 14 – ACTIVE REGION SAFE OPERATING AREA



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

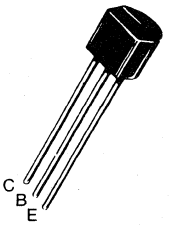
The data of Figure 14 is based upon $T_{J(pk)}$=150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data of Figure 13. At high case or ambient temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (see AN 415).

BC559
BC560

PNP SILICON ANNULAR♦ LOW NOISE, HIGH GAIN AMPLIFIER TRANSISTOR

- Low Wideband Noise Figure
  N_F = 2.5 dB max (30 Hz-15 KHz)
- Low Noise At Low Frequency
  V_T = 10 nV/√ Hz max (120 Hz)
- High Gain in 2 Ranges
  B range: 180 – 460
  C range: 380 – 800
  (2 mA/5 V)
- Full Applications Information

PNP SILICON LOW NOISE TRANSISTOR

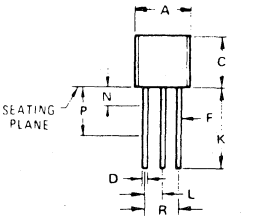


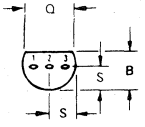
MAXIMUM RATINGS

Rating	Symbol	Value BC559	Value BC560	Unit
Collector-Emitter Voltage	V_{CEO}	35	45	Vdc
Collector-Base Voltage	V_{CBO}	45	50	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current Continuous Peak	I_C	0.1 0.2		Adc Adc
Base-Current-Continuous	I_B	0.05		Adc
Total Device Dissipation at T_A = 25 °C Derate above 25 °C	P_D	625 5		mW mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦Annular Semiconductors Patented by Motorola Inc.

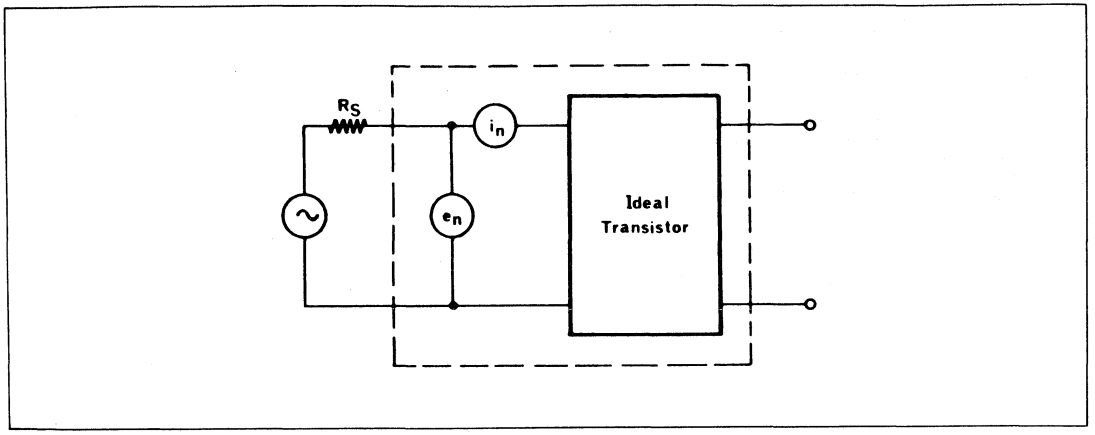
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0) BC559	BV_{CEO}	35			Vdc
BC560		45			
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0) BC559	BV_{CBO}	45			Vdc
BC560		50			
Emitter-Base Breakdown Voltage (I_C = 10 μAdc, I_C = 0)	BV_{EBO}	5			Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}			15	nAdc
(V_{CB} = 30 Vdc, I_E = 0, T_A = +125 °C)				5	μAdc
Emitter Cutoff Current (V_{EB} = 4 Vdc, I_C = 0)	I_{EBO}			15	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 μAdc, V_{CE} = 5 Vdc) BC559B/560B	h_{FE}	100	150		
BC559C/560C		100	270		
(I_C = 2 mAdc, V_{CE} = 5 Vdc) BC559B/560B		180	290	460	
BC559C/560C		380	500	800	
Collector-Emitter Saturation Voltage	$V_{CE(S)}$				Vdc
(I_C = 10 mAdc, I_B = 0.5 mAdc)			0.075	0.25	
(I_C = 10 mAdc, I_B = see note 1)			0.3	0.6	
(I_C = 100 mAdc, I_B = 5 mAdc, see note 2)			0.25		
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 5 mAdc)	$V_{BE(S)}$		1.1		Vdc
Base-Emitter On Voltage	$V_{BE(ON)}$				Vdc
(I_C = 10 μAdc, V_{CE} = 5 Vdc)			0.52		
(I_C = 100 μAdc, V_{CE} = 5 Vdc)			0.55		
(I_C = 2 mAdc, V_{CE} = 5 Vdc)		0.55	0.62	0.75	

Note 1: I_B is value for which I_C = 11 mA at V_{CE} = 1 V
Note 2: Pulse test = 300 μs; Duty Cycle = 2 %.

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5 Vdc, f = 100 MHz)	f_T		250		MHz
Collector-Base Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cbo}		2.5		pF
h-PARAMETERS (I_C = 2 mAdc, V_{CE} = 5 Vdc, f = 1 KHz)					
Input Impedance BC559B/BC560B BC559C/BC560C	h_{ie}, (h_{11e})	3.2 5.0	6.0 8.0	8.5 14.0	KΩ
Voltage Feedback Ratio BC559B/BC560B BC559C/BC560C	h_{re} (h_{12e})		3.5 4.0		10^{-4}
Small Signal Current Gain BC559B/BC560B BC559C/BC560C	h_{fe} (h_{21e})	240 450	330 600	500 900	
Output Admittance BC559B/BC560B BC559C/BC560C	h_{oe} (h_{22e})		10 12	60 110	μmhos
NOISE PERFORMANCE					
Noise Figure (I_C = 200 μAdc, V_{CE} = 5 Vdc, R_S = 2 KΩ, f = 30 Hz – 15 KHz)	N_F		0.5	2.0	dB
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2 KΩ, f = 120 Hz) See Application note, Section I	V_T		8.0	10	$nV/\sqrt{Hz}$
Equivalent Input Noise Voltage (I_C = 200 μAdc, V_{CE} = 5 V, R_S = 2KΩ, f = 10 Hz – 50 Hz) See Application note, Section II	V_T		74	110	$nV/\sqrt{Hz}$

FIGURE 1 – TRANSISTOR NOISE MODEL



NOISE APPLICATION NOTE

I. NOISE FIGURE RELATED TO V_T, e_n, and i_n

For a transistor,, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4\,KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \qquad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts/$\sqrt{Hz}$)

e_n = noise voltage of the transistor referred to the input (figures 2 & 3)

i_n = noise current of the transistor referred to the input (figure 4)

K = Boltzmann's constant (1.38×10^{-23} j/°K)

T = Temperature of the source resistance (°K)

R_S = Source resistance (Ohms)

Example:
Find the total noise at the input of a BC560 for a collector current of 1mA and a source impedance of 1KΩ at a frequency of 120 Hz and a temperature of 25 °C.

1. V_T is calculated from e_n, i_n

Read e_n 4.5 nV/$\sqrt{Hz}$ from figure 3 (Note that this is for a one cycle bandwidth)

Read i_n 5.8 pA/$\sqrt{Hz}$ from figure 4

$$V_T = [(3.5 \times 10^{-9})^2 + (4).(1.38 \times 10^{-23}).(300).(1 \times 10^3) + (5.8 \times 10^{-12})^2.(1 \times 10^3)^2]^{1/2}$$

Thus: $\boxed{V_T = 8.2\ nV}$.

This checks with the value of 8 nV shown in figure 6.

2. Noise figure is calculated from V_T

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by source resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2}$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(8 \times 10^{-9})2}{16.6 \times 10^{-18}}\right]^{1/2}$$

Thus: $\boxed{NF = 5.9\ dB}$

This checks with the values of 6 dB read from figure 7.

To minimize noise in a transistor stage, one might use figure is minimum. This is not necessarily true as shown by figure 6 where the total noise voltage is a minimum at small values of source impedance.
This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

II. NOISE VARIATION WITH FREQUENCY

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V_T = V_T . f.^{1/2}$
2. For variable transistor noise integrate the spectral density V_T (where $\triangle f = 1$ Hz), over the bandwidth of interest.

Example: Low Frequency Noise

Find the total noise at the input in the bandwidth $f_1 =$ 10 Hz, $f_2 = 50$ Hz at $I_C = 200\ \mu A$ and $R_S = 2\ K\Omega$ This example corresponds to the popular "FLICKER NOISE" test shown on many data sheets.

$$V_T^2 = \int_{-\infty}^{+\infty} V_T(f) \times [G(f)^2\ df$$

$(f_1 - f_2)$

where:

$$V_{T(f)}^2 = e_{n(f)}^2 + 4\ KT\ R_S + i_{n(f)}^2\ R_S^2$$

$e_{n(f)}$ and $4\ KT\ R_S$ are constant in the bandwidth

$$i_{n(f)} = \frac{i_n^2\ (1\ Hz)}{f} \quad \text{(1/f noise spectrum density)}$$

G(f) bandpass filter

$= 1$ for $f \in (f_1, f_2)$

$= 0$ for $f \notin (f_1, f_2)$

after integration:

$$V_{T(f_1-f_2)}^2 = (e_{n(f1)}^2 + 4\ KT\ R_S) \times (f_2-f_1) + R_S^2\ i_{n(f1)}^2 \times f1 \times i_{n(f1)} \frac{f2}{f1}$$

Now:

$e_n = 5\ nV/\sqrt{Hz}$ at 10 Hz (from figure 2)

$i_n = 7\ pA/\sqrt{Hz}$ at 10 Hz (from figure 4)

$$V_T^2\ (10\ Hz–50\ Hz) = [(25 + 33.1)\ 40 + 196 \times 10 \times 1.6].10^{-18}$$

Thus: $\boxed{V_T(10\ Hz–50\ Hz) = 74\ nV}$

FIGURE 2 – NOISE VOLTAGE V_S FREQUENCY

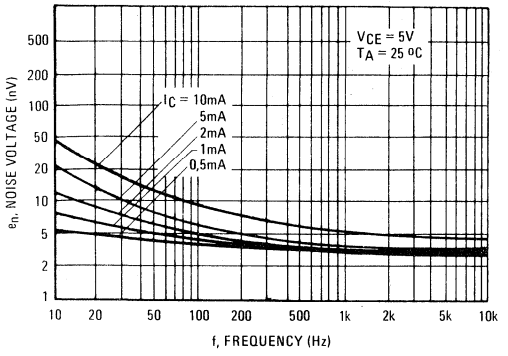


FIGURE 3 – NOISE VOLTAGE V_S COLLECTOR CURRENT

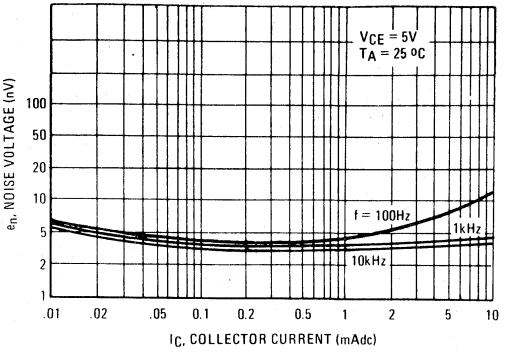


FIGURE 4 – NOISE CURRENT

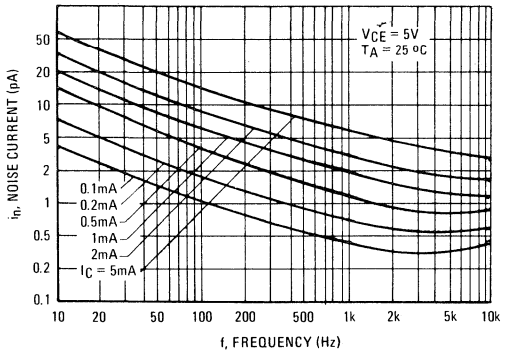


FIGURE 5 – WIDEBAND NOISE FIGURE

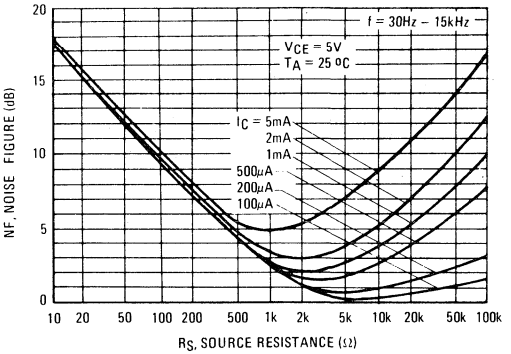


FIGURE 6 – TOTAL NOISE VOLTAGE (120 Hz)

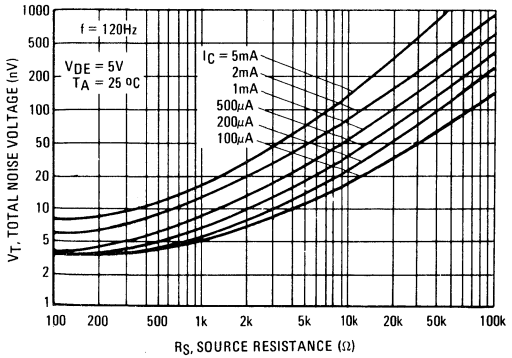


FIGURE 7 – NOISE FIGURE (120 Hz)

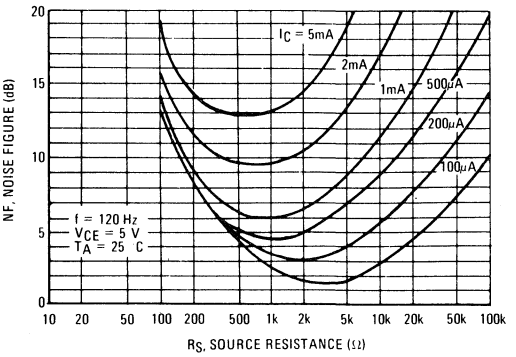


FIGURE 8 – NORMALIZED DC CURRENT GAIN

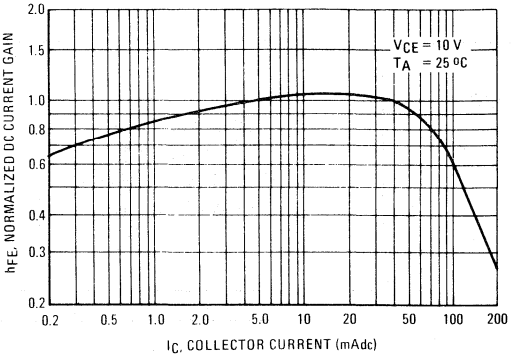


FIGURE 9 – "SATURATION" AND "ON" VOLTAGES

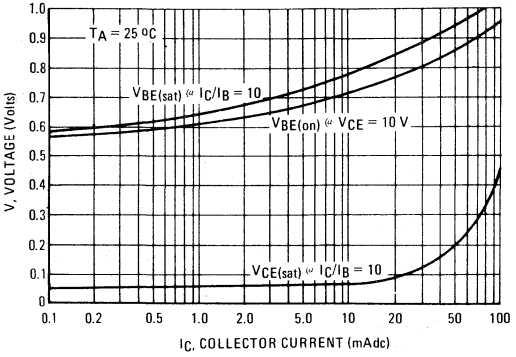


FIGURE 10 – CURRENT GAIN-BANDWIDTH PRODUCT

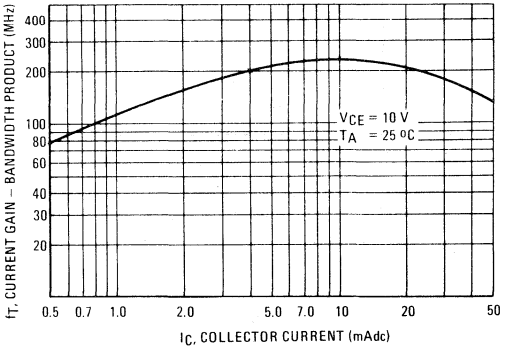


FIGURE 11 – CAPACITANCE

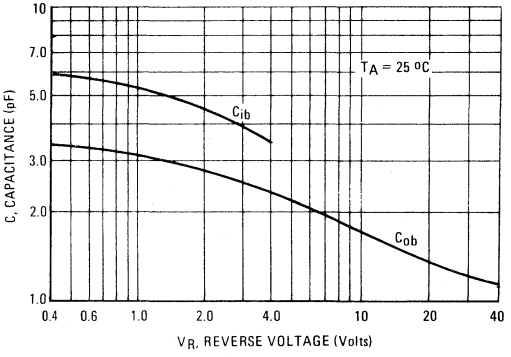


FIGURE 12 – OUTPUT ADMITTANCE

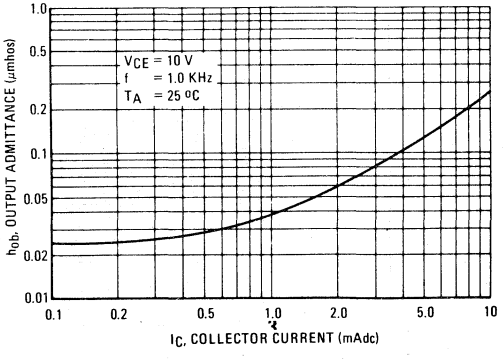
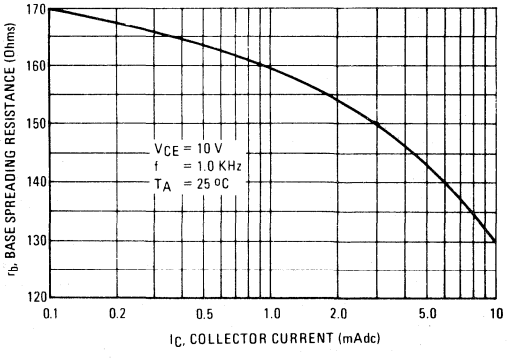


FIGURE 13 – BASE SPREADING RESISTANCE



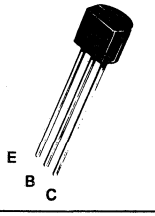
BC650,S
BC651,S

NPN SILICON ANNULAR▲ AMPLIFIER TRANSISTORS

. . . designed for use in low-level, low-noise amplifier applications.

- Very Low Noise Figure:
  NF = 0.5 dB (Typ) – BC650/S – BC651/S
  @ 100 Hz, 10 KΩ, 0.1 mA, 5.0 Volts
- Excellent h_{FE} Linearity from 1.0 μA to 10 mA
- High DC Current Gain:
  h_{FE} @ I_C = 2 mA, V_{CE} = 5 V
  C range: : 380 – 820
  D range: 680 – 1400
- Excellent Reliability with Nitride Chip Passivation and Third Generation Epoxy

NPN SILICON
LOW NOISE
AUDIO AMPLIFIER
TRANSISTORS

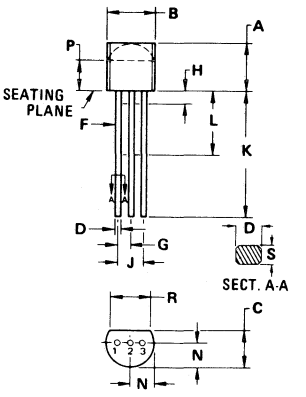


MAXIMUM RATINGS*			
Rating	**Symbol**	**Value**	**Unit**
Collector-Base Voltage BC651 BC650	V_{CB}	45 30	Vdc
Collector-Emitter Voltage BC651 BC650	V_{CEO}	45 30	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current	I_C	200	mAdc
Total Power Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	1.5 12	Watts mW/°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max.	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	83.3	°C/W

* Indicates JEDEC Registered Data



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

▲ Annular Semiconductors Patented by Motorola.

***ELECTRICAL CHARACTERISTICS** (T_A = 25 °C unless otherwise noted)

Characteristics		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	0.015	μA
Collector-Emitter Current (V_{CE} = 30 Vdc)		I_{CEO}	–	0.025	μA
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BC650 BC651	$V_{(BR)CBO}$	30 45	–	Vdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.015	μA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BC650 BC651	$V_{(BR)CEO}$	30 45	–	Vdc
ON CHARACTERISTICS					
DC Current Gain I_C = 2 mAdc, V_{CE} = 5 Vdc	BC650/BC651 BC650C/BC651C BC650D/BC651D	h_{FE}	380 380 680	1400 820 1400	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc) (I_C = 100 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	– –	0.2 0.6	Vdc
Base Emitter On Voltage (I_C = 2 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	0.55	0.70	Vdc
DYNAMIC CHARACTERISTICS					
Input Impedance (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = **1.0 kHz**)	BC650C/BC651C BC650D/BC651D	h_{ie}	2.0 4.0	20 60	kΩ
Voltage Feedback Ratio (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650C/BC651C BC650D/BC651D	h_{re}	1.0 2.0	30 60	X10-4
Output Admittance (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650C/BC651C BC650D/BC651D	h_{oe}	10 20	60 120	μmhos
Small Signal Current Gain (I_C = 2 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	BC650/BC651	h_{fe}	380	1600	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	3.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	–	8.0	pF
Current Gain – Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 5.0 V, f = 100 MHz)		f_T	100	700	MHz

NOISE FIGURE/TOTAL NOISE VOLTAGE CHARACTERISTICS (V_{CE} = 5.0 V, I_C = 0.2 mA T_A = 25 °C)

	NF Max. (1)	VT Max. (1)	NF Max. (2)	VT Max. (2)	NF Max. (3)	VT Max. (3)	Unit	Unit
BC650, BC651, C, D	8	14.4	2.5	7.6	1	6.4	dB	nV
BC650S, BC651S, CS, DS	4	9.1	1.5	6.8	1	6.4	dB	nV

(1) RS = 2 kΩ, BW = 1.0 Hz, f = 10 Hz
(2) RS = 2 kΩ, BW = 1.0 Hz, f = 120 Hz
(3) RS = 2 kΩ, BW = 1.0 Hz, f = 1 kHz

NOISE APPLICATION NOTE

For a transistor, total noise at the input may be expressed as:

$$V_T = \left[e_n^2 + 4KT\,R_S + i_n^2\,R_S^2\right]^{1/2} \quad (1)$$

Where:

V_T = total noise voltage at the transistor input (Volts $/\sqrt{Hz}$)

e_n = noise voltage of the transistor referred to the input

i_n = noise current of the transistor referred to the input

K = Boltzman's constant (1.38×10^{-23} j/°K)

T = temperature of the source resistance (°K)

R_S = source resistance (Ohms)

Example:

Find the total noise at the input of a BC650 for a collector current of 100 μA and a source impedance of 50 kilohm at a frequency of 100 Hz and at a temperature of 25 °C.

Read e_n = 2.0 nV $/\sqrt{Hz}$ from Figure 7.

(Note that this is for a one cycle bandwidth)

Read i_n = 0.31 pA $/\sqrt{Hz}$ from Figure 8.

$V_T = [(2.0 \times 10^{-9})^2 + (4)(1.38 \times 10^{-23})(297)(5 \times 10^4) + (0.31 \times 10^{-12})^2 (5 \times 10^4)^2]^{1/2} =$ 32.6 nV $/\sqrt{Hz}$.

Note that for the resistor alone ($e_n = i_n = 0$), V_T is 28.6 nV $/\sqrt{Hz}$.

Noise figure is defined as:

$$NF = 20 \log_{10} \frac{\text{total noise voltage}}{\text{noise voltage contributed by the Source Resistance}}$$

or

$$NF = 20 \log_{10} \left[\frac{V_T^2}{4\,KT\,R_S}\right]^{1/2} \quad (2)$$

Noise figure can be calculated for the above example as follows:

$$NF = 20 \log_{10} \left[\frac{(32.6 \times 10^{-9})^2}{8.2 \times 10^{-16}}\right]^{1/2} = 1.1\text{dB}$$

To minimize noise in a transistor stage, one might assume that noise is minimized when Noise Figure is minimum. This is not necessarily true since the total noise voltage is a minimum at small values of source impedance. This can be seen from equation (1) which shows that total noise is a direct function of source resistance.

Noise over a frequency band can be handled in one of two ways depending upon whether total transistor noise is constant or variable over the bandwidth of interest:

1. For Constant transistor noise, multiply, V_T by the square root of bandwidth. i.e., $V'_T = V_T \cdot \Delta f^{1/2}$.
2. For variable transistor noise, plot V_T (where Δf = 1.0 Hz) versus frequency over the bandwidth and integrate the result.

Total noise voltage at the output of the transistor stage can be found by multiplying V_T or V'_T by the voltage gain of the stage.

COMPUTER MODEL

In their book "Low-Noise Electronic Design," published by Wiley & Sons, (copyright 1973), the authors, C.D. Motchenbacher and F.C. Fitchen have presented a computer program for Noise Figure circuit analysis. The computer constants for both models of the BC650/S, BC651/S transistor are presented below for your convenience.

"NOSMOD" Model

Computer Symbol	Value
E	Read e_n from figure 7 at 10 kHz for desired current
I	Read i_n from figure 8 at 10 kHz for desired current
F1	1.0 Hz
F2	100,000 kHz
F3	100 Hz
F4	100,000 kHz

"XISTOR" Model

Computer Symbol	Value
N5	100 Ω
N6	70 Ω
14	Collector Current of application
17	5×10^{-10} Amps
F7	110000
F8	Read f_T from figure 16 for desired current
Q1	1.37
Q2	1.25
B	actual measured h_{FE}

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 V, T_A = 25°C)

CONTOURS OF CONSTANT NOISE FIGURE

NARROW BAND

FIGURE 1 – 10 Hz

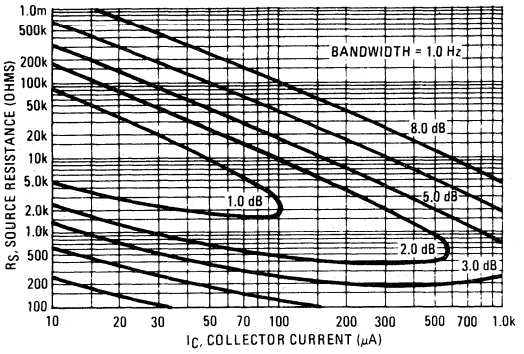
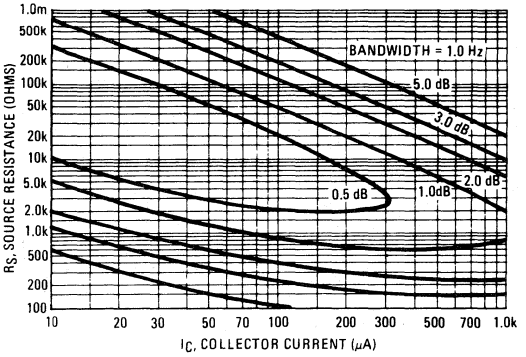


FIGURE 2 – 100 Hz



NARROW BAND

FIGURE 3 – 1.0 kHz

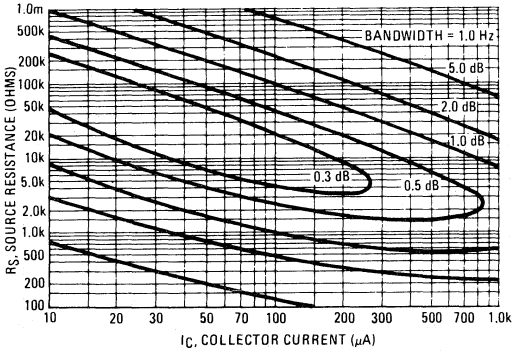
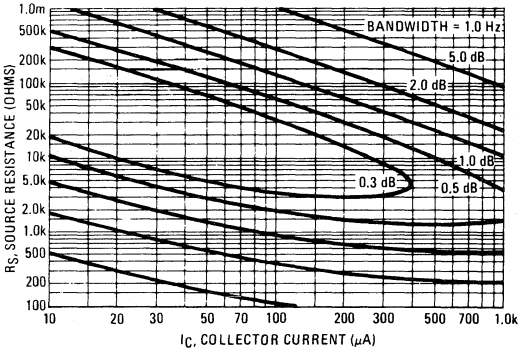


FIGURE 4 – 10 kHz



BROAD BAND

FIGURE 5 – 10 Hz – 10 kHz

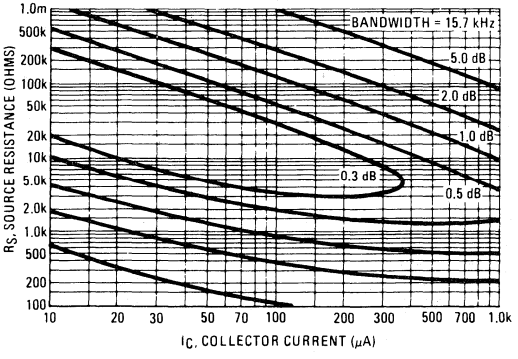
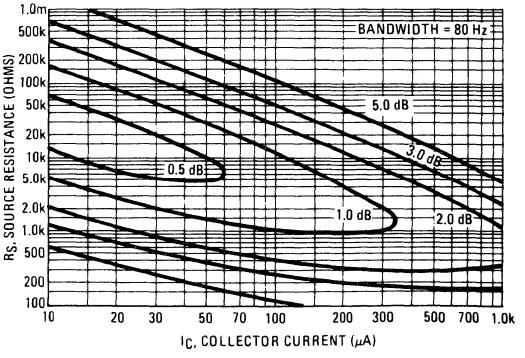


FIGURE 6 – 10 – 50 Hz LOW-FREQUENCY



TYPICAL ELECTRICAL CHARACTERISTICS
(V_{CE} = 5.0 V, T_A = 25°C)

FIGURE 7 – NOISE VOLTAGE

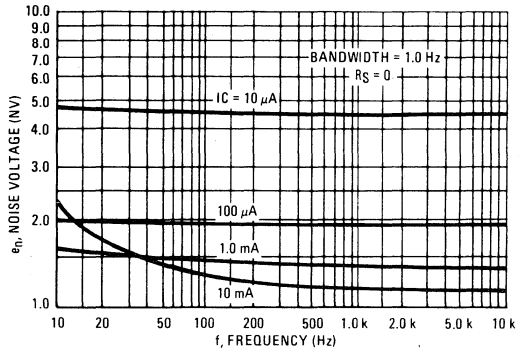


FIGURE 8 – NOISE CURRENT

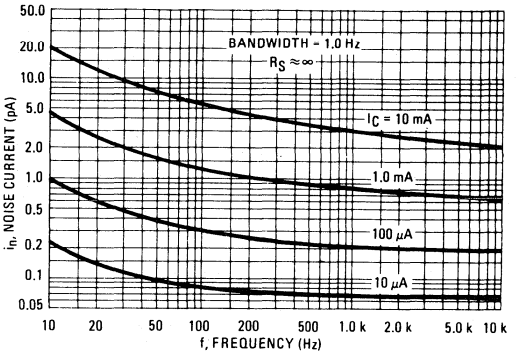


FIGURE 9 – SMALL-SIGNAL CURRENT GAIN

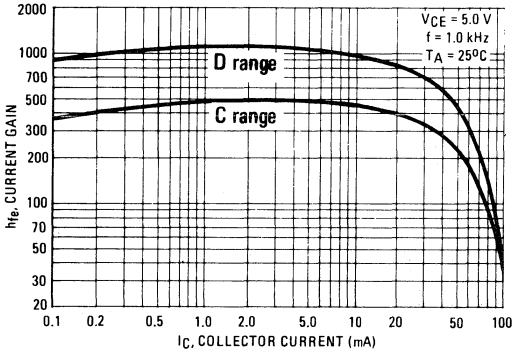


FIGURE 10 – INPUT IMPEDANCE

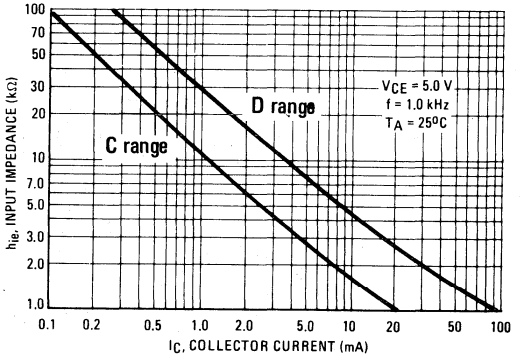


FIGURE 11 – OUTPUT ADMITTANCE

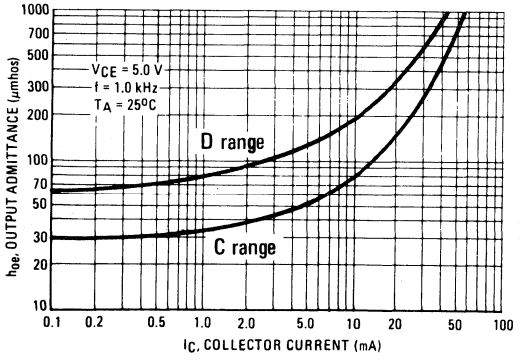


FIGURE 12 – TEMPERATURE COEFFICIENTS

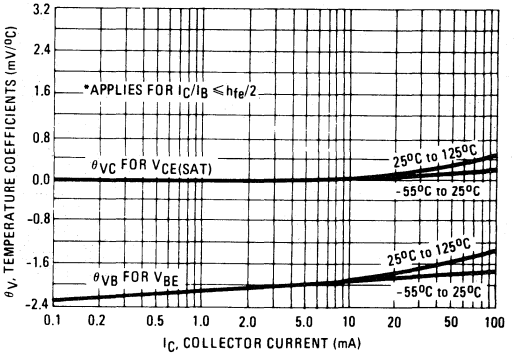


FIGURE 13 – DC CURRENT GAIN

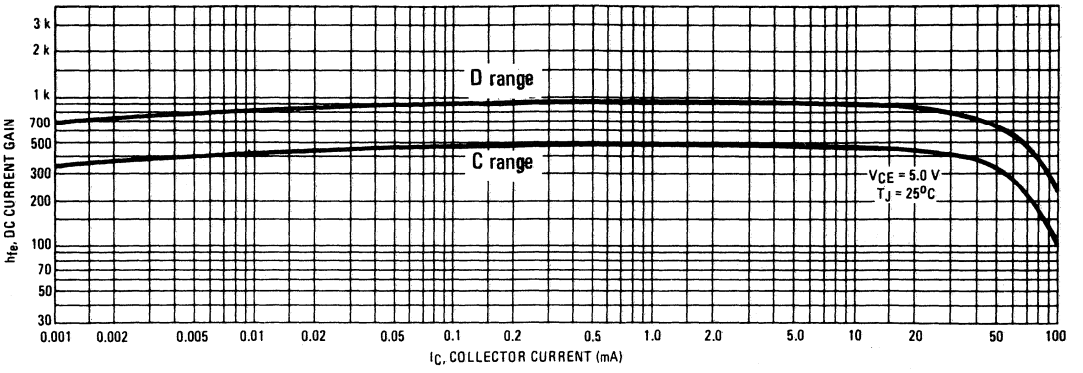


FIGURE 14 – COLLECTOR SATURATION REGION

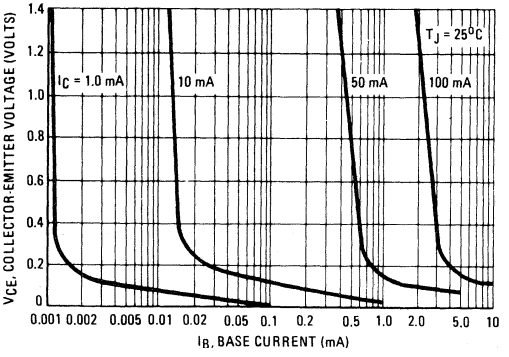


FIGURE 15 – "ON" VOLTAGES

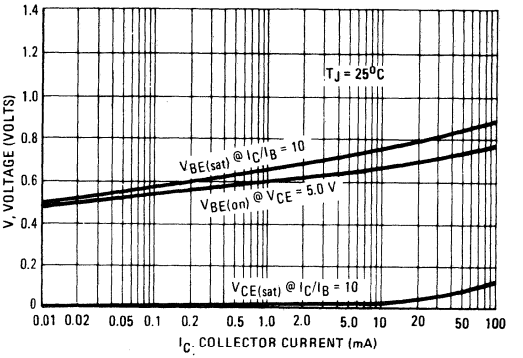


FIGURE 16 – CURRENT-GAIN – BANDWIDTH PRODUCT

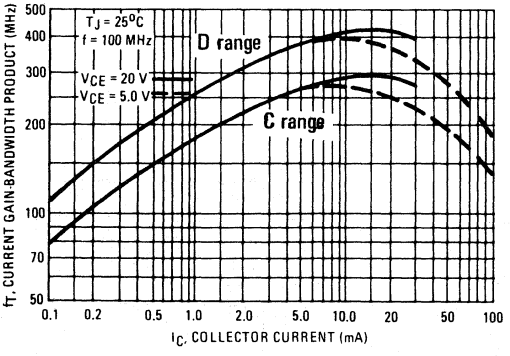
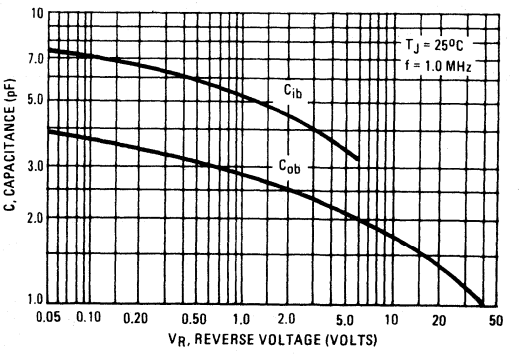


FIGURE 17 – CAPACITANCE



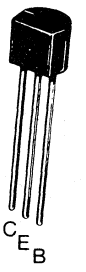
BF198

NPN SILICON ANNULAR♦ TRANSISTOR

. . . Transistor with low feedback capacitance especially for controlled TV/IF Amplifier

- Low common emitter feedback capacitance
  C_{RE} = .2 pf (typ)
- Low noise figure – NF = 3 db (typ)
  @ F = 35 MHz
- Forward AGC characteristics
- Y-Parameters at 35 MHz

NPN SILICON RF TRANSISTOR

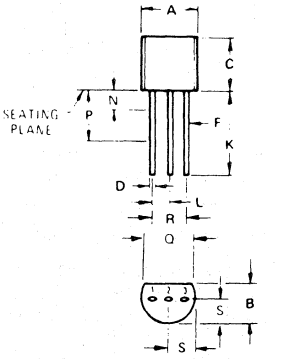


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector Current	I_C	25	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	83	°C/W



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700		0.500	-
L	1.150	1.390	0.045	0.055
N		1.270		0.050
P	6.350		0.250	
Q	3.430		0.135	
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	BV_{CEO}	30			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4			Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4 mAdc, V_{CE} = 10 Vdc)	h_{FE}	27	70		
Base-Emitter On Voltage (I_C = 4 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$		780	900	mVdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 4 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T		800		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_C = 1 mAdc, f = 1 MHz)	C_{re}		.2		pF
Noise Figure (I_C = 4 mAdc, V_{CC} = 12 Vdc, f = 50 ohms, f = 35 MHz	NF		3		dB

COMMON EMITTER PARAMETERS (V_{CE} = 10 V, I_C = 4 mA, f = 35 MHz)

Input Conductance	g_{ie}		5.0		mS
Input Capacitance	C_{ie}		30		pF
Forward Transfer Admittance magnitude	$\|Y_{fe}\|$		110		mS
Forward Transfer Admittance Phase Angle	ϕ_{fe}		−19°		
Feedback Capacitance	C_{re}		.2		pF
Output Conductance	g_{oe}		18		μS
Output Capacitance	C_{oe}		1.3		pF

FIGURE 1 – DC CURRENT GAIN

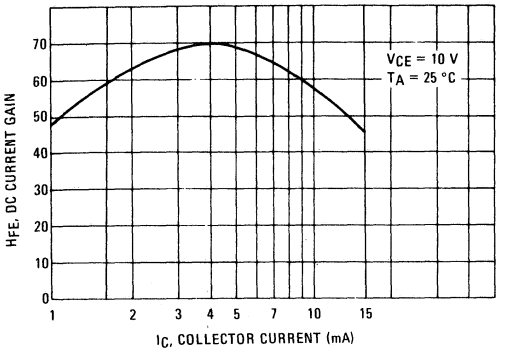


FIGURE 2 – CURRENT GAIN BANDWIDTH PRODUCT

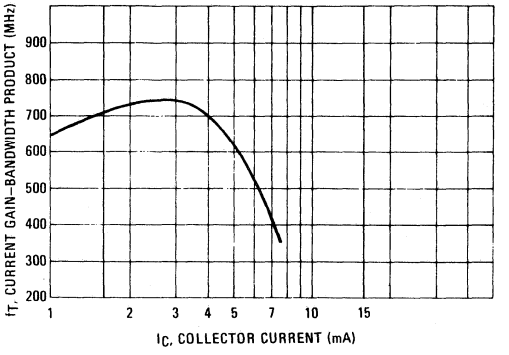


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

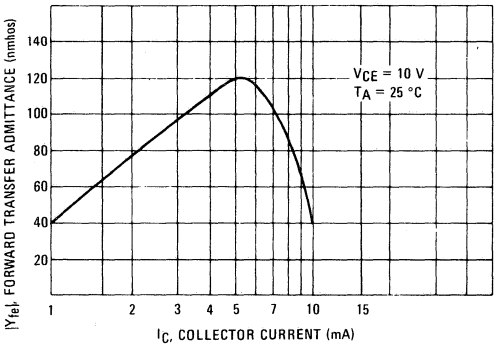


FIGURE 4 – AGC CHARACTERISTICS – POWER GAIN

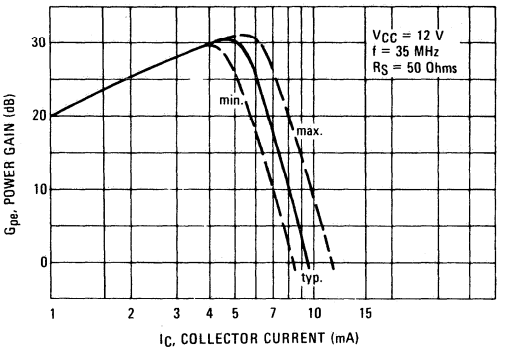
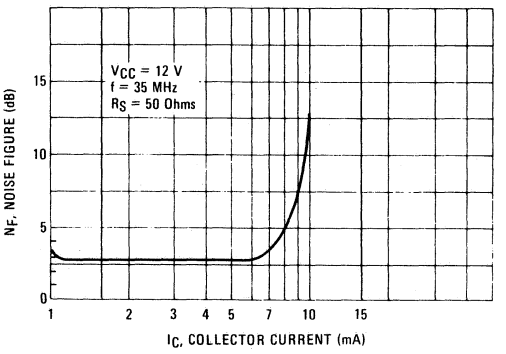


FIGURE 5 – NOISE FIGURE

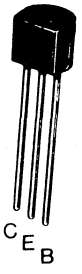


NPN SILICON ANNULAR♦ TRANSISTOR

. . . Transistor with low feedback capacitance especially for TV/IF Amplifier

- High detection level
- Low common emitter feedback capacitance
  C_{RE}: 0.25 pF (typ)
- High F_t . 750 MHz (typ)
- Y Parameter characteristics @ 35 MHz

NPN SILICON RF TRANSISTOR



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Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
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Characteristic	Symbol	Max	Unit
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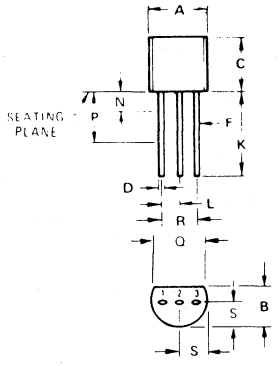

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

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Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	BV_{CEO}	25			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4			Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 7 mAdc, V_{CE} = 10 Vdc)	h_{FE}	40	85		
Base-Emitter On Voltage (I_C = 7 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$		770	900	mVdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	750		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		0.25	0.35	pF
Noise figure I_C = 4 mA, V_{CE} = 10 V, R_S = 50 Ω, f = 35 MHz	N_f		2.5		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 7 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 35 MHz	Unit
g_{11e}	4.0	mmhos
b_{11e}	7.0	mmhos
g_{22e}	25	μmhos
b_{22e}	380	μmhos
g_{12e}	−15.0	μmhos
b_{12e}	−70.0	μmhos
g_{21e}	150	mmhos
b_{21e}	−35	mmhos

FIGURE 1 – DC CURRENT GAIN

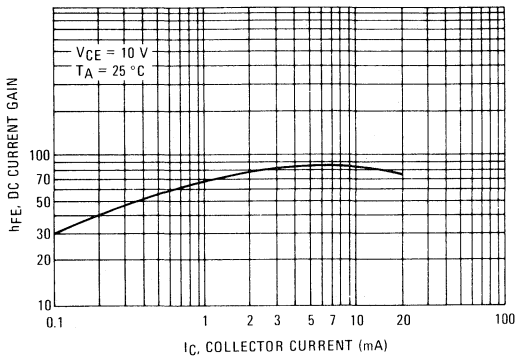


FIGURE 2 – CURRENT GAIN – BANDWITH PRODUCT

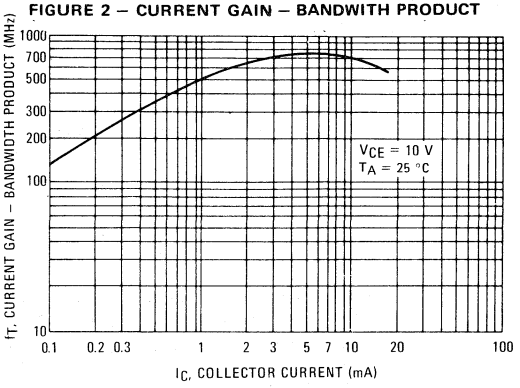


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

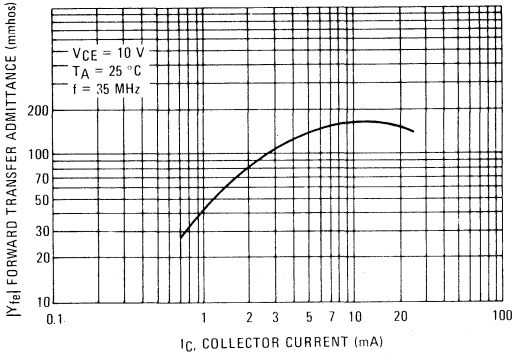


FIGURE 4 – CAPACITANCES

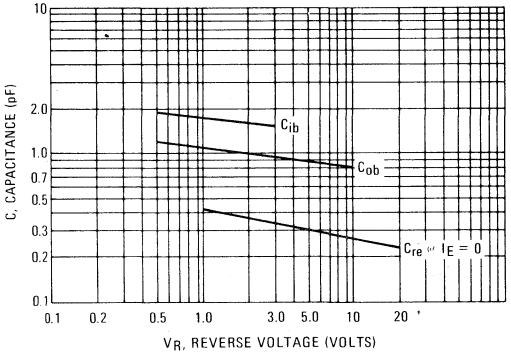
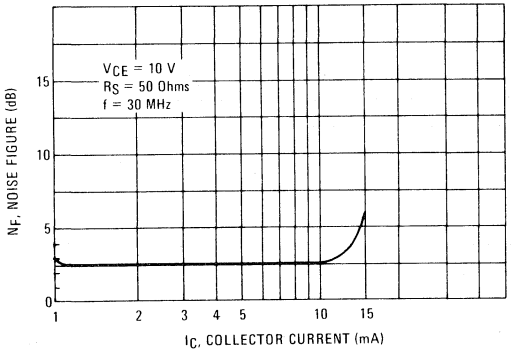


FIGURE 5 – NOISE FIGURE



BF240
BF241

NPN SILICON ANNULAR♦ TRANSISTOR

AM/FM Amplifier (Common Emitter Circuit).

Input stages for AM. General RF input, Mixer and oscillator stages.

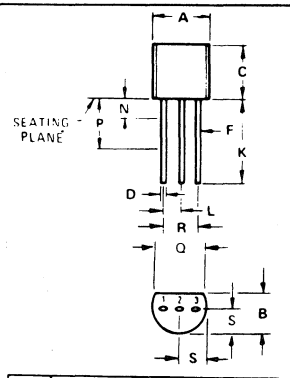
NPN SILICON
RF TRANSISTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector Current	I_C	25	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW
Thermal Resistance, Junction to Case	θ_{JC}	0.125	°C/mW



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 2 mAdc, I_B = 0)	BV_{CEO}	40			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4			Vdc
Collector Cutoff Current (V_{CB} = 20Vdc, I_E = 0)	I_{CBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain I_C = 1mAdc, V_{CE} = 10 Vdc BF240 BF241	h_{FE}	67 36		222 125	
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	.65	.70	.74	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) BF240 BF241	f_T		600 470		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		.28	.34	pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, R_S = 200 Ω – f = 100 KHz R_S = 50 Ω – f = 100 MHz	NF		2.5	3.5	dB
Output Admittance (I_C = 1mAdc, V_{CE} = 10 Vdc, f = 450 KHz f = 10.7 MHz	g_{oe}			8.3 10.5	μmho μmho

(1) Pulse test: pulse width ≤ 300 μs. Duty cycle ≤ 2.0%

FIGURE 1 – CURRENT GAIN-BANDWIDTH PRODUCT

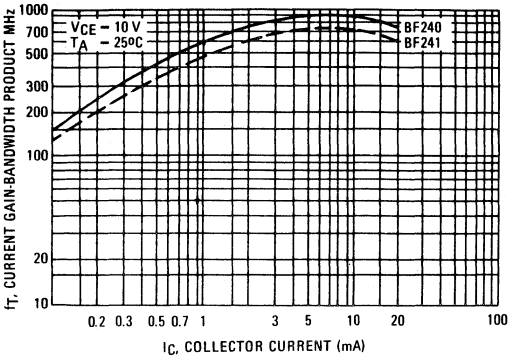


FIGURE 2 – CAPACITANCES

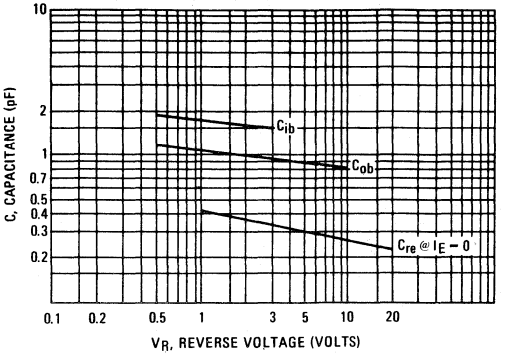


FIGURE 3 – DC CURRENT GAIN

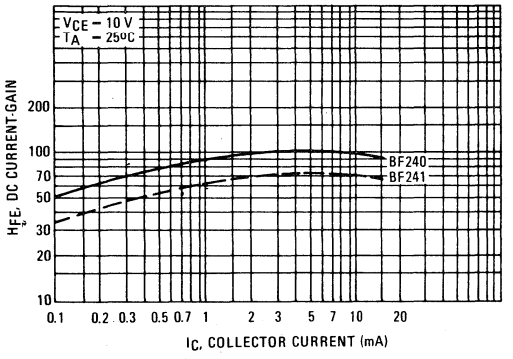


FIGURE 4 – b11e

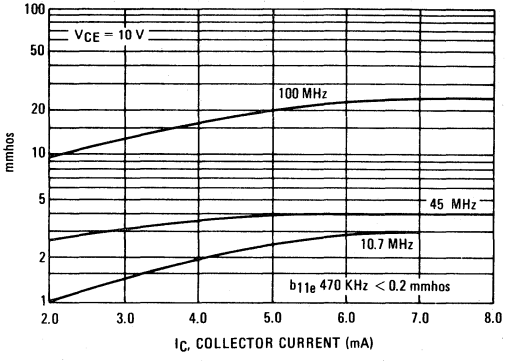


FIGURE 5 – b21e

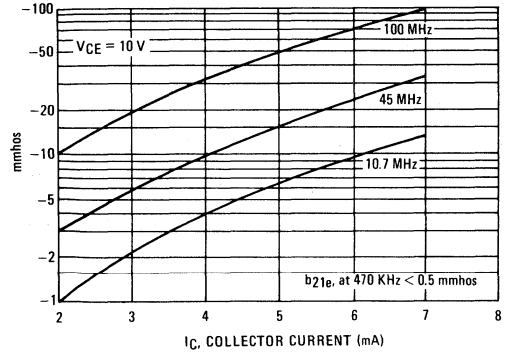


FIGURE 6 – b22e (boe)

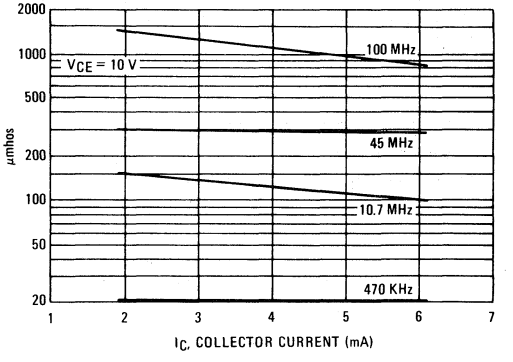


FIGURE 7 – g11e (gie)

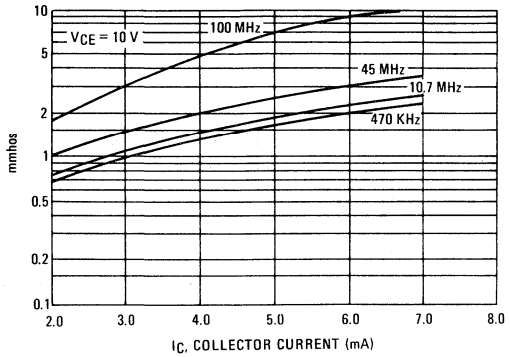


FIGURE 8 – g21e (Yfe)

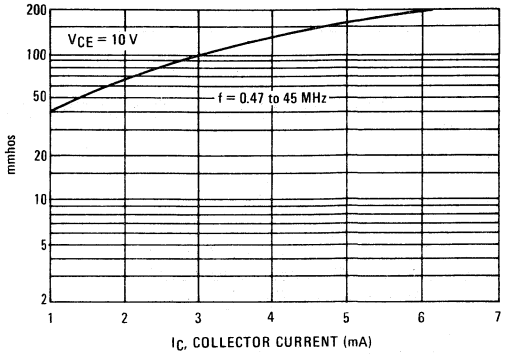
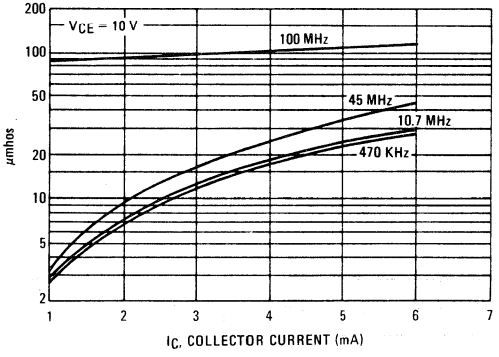


FIGURE 9 – g22e (goe)



BF254
BF255

NPN SILICON ANNULAR♦ TRANSISTOR

- Designed as a Common emitter amplifier for AM radios and FM/IF stages.
- High output impedance
- Complete Y-Parameter characterisation

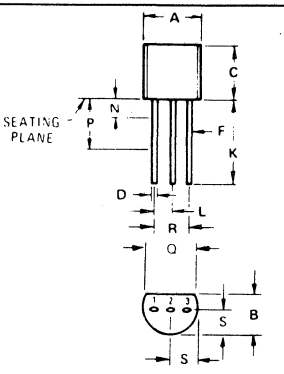
NPN SILICON RF TRANSISTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	Θ_{JA}	200	°C/W
Thermal Resistance, Junction to Case	Θ_{JC}	83	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	20			Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	30			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0			Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}			100	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain I_C = 1.0 mA, V_{CE} = 10 Vdc BF254 BF254-3 BF254-4 BF255 BF255-2 BF255-3	h_{FE}	 65 65 100 35 35 65		 220 125 220 125 75 125	
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) BF254 BF255	$V_{BE(on)}$		0.68		Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) BF254 BF255	f_T		260 200		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}		0.90		pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 MHz, R_S = 50 ohms)	NF		1.7		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 450 KHz		f = 10.7 MHz		Unit
	BF254	BF255	BF254	BF255	
g_{11e}	.20	.40	.26	.5	mmhos
b_{11e}	.05	.06	1.2	1.6	mmhos
g_{22e}	3.0	1.5	5.3	4.5	μmhos
b_{22e}	8.0	8.0	190	190	μmhos
b_{12e}	−5.0	−5.0	−130	−130	μmhos
g_{12e}	−0.7	−0.4	−3.0	−3.5	μmhos
g_{21e}	30	30	30	30	mmhos
b_{21e}	−0.003	−0.004	−0.7	−1.0	mmhos

FIGURE 1 – DC CURRENT GAIN

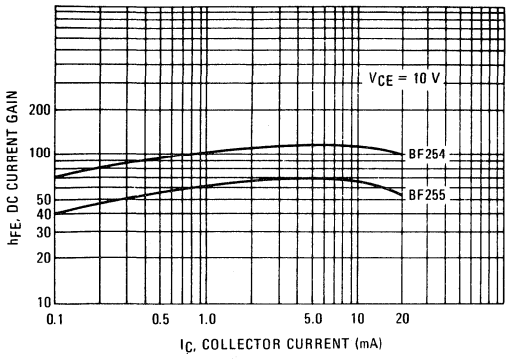


FIGURE 2 – CURRENT GAIN–BANDWITH PRODUCT

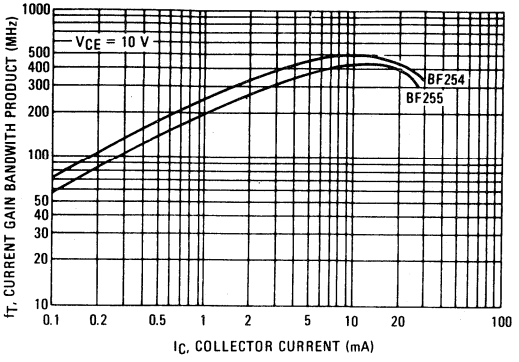


FIGURE 3 – "ON" VOLTAGE

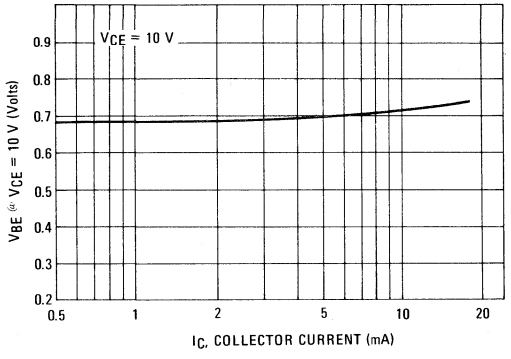
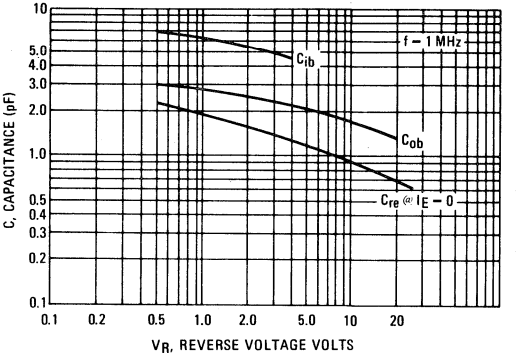


FIGURE 4 – CAPACITANCES



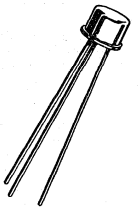
BF257
BF258 • BF259

NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for high-voltage DC - VHF video amplifier applications.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 300 (Min) @ I_C = 30 mAdc — BF259
- Low Collector Cutoff Current —
  I_{CBO} = 50 nAdc (Max) @ V_{CB} = 250 Vdc — BF259
- DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 30 mAdc

NPN SILICON AMPLIFIER TRANSISTORS



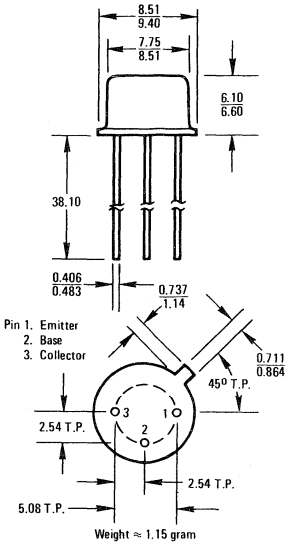
MAXIMUM RATINGS

Rating	Symbol	BF257	BF258	BF259	Unit
Collector-Emitter Voltage	V_{CEO}	160	250	300	Vdc
Collector-Emitter Voltage	V_{CER}	160	250	300	Vdc
Collector-Base Voltage	V_{CB}	160	250	300	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous	I_C	← 100 →			mAdc
Total Device Dissipation @ T_C = 25°C	P_D	← 5.0 →			Watts
Operating Junction Temperature Range	T_J	← +175 →			°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{THJcase}$	30	°C/W

♦Annular Semiconductor Patented by Motorola Inc.



CASE 31 (1)
TO-5
All Dimensions in Millimeters

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		BV_{CEO}				Vdc
(I_C = 30 mAdc, I_B = 0)	BF257		160	–	–	
	BF258		250	–	–	
	BF259		300	–	–	
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 100 μAdc, I_E = 0)	BF257		160	–	–	
	BF258		250	–	–	
	BF259		300	–	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	–	Vdc
(I_E = 100 μAdc, I_C = 0)						
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 100 Vdc, I_E = 0)	BF257		–	–	50	
(V_{CB} = 200 Vdc, I_E = 0)	BF258		–	–	50	
(V_{CB} = 250 Vdc, I_E = 0)	BF259		–	–	50	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}	25	–	–	–
(I_C = 30 mAdc, V_{CE} = 10 Vdc)						
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	–	1.0	Vdc
(I_C = 30 mAdc, I_B = 6.0 mAdc)						
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product		f_T	–	110	–	MHz
(I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)						
Reverse Transfer Capacitance		C_{re}	–	3.5	–	pF
(V_{CB} = 30 Vdc, I_E = 0, f = 500 kHz)						
Collector-Base Capacitance		C_{cb}	–	5.5	–	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 500 kHz)						

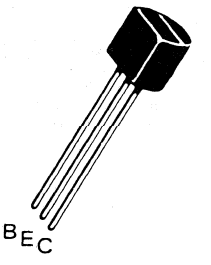
BF371
BF373

NPN SILICON EPITAXIAL TRANSISTOR

. . . designed for third-stage video IF applications in television receivers.

- High Detection Level (BF 373)
- Breakdown Voltages
  BF 371 BV_{CEO} = 30 V, BV_{CBO} = 40 V
  BF 373 BV_{CEO} = 45 V, BV_{CBO} = 45 V
- Low Collector-Base Capacitance –
  C_{cb} = 0.32 pF (Max) @ V_{CB} = 10 Vdc
- Complete y-Parameter Curves @ 35 MHz

NPN SILICON IF TRANSISTOR

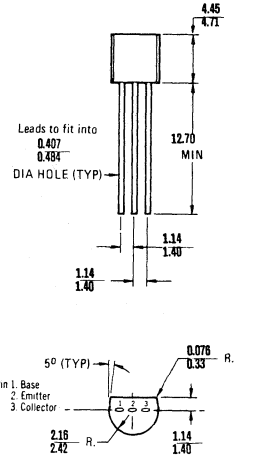


MAXIMUM RATINGS

Rating	Symbol	BF371	BF373	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	Vdc
Collector-Base Voltage	V_{CB}	40	45	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	100		mAdc
Total Device Dissipation @ T_A = 25°C	P_D	310	625	mW
derating		2.47	5.0	mW/°C above 25°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to + 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BF371	BF373	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.404 max.	0.2 max.	°C/mW



CASE 29 (2)
TO-92

All dimensions in Millimeters

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Type	Symbol	Min	Typ.	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BF 371 BF 373	BV_{CEO}	30 45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100μAdc, I_E = 0)	BF 371 BF 373	BV_{CBO}	40 45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10μAdc, I_C = 0)		BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 7.0 mAdc, V_{CE} = 10 Vdc) (I_C = 20 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	 40 15	 – –	 – –	–
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)		$V_{CE(sat)}$	–	–	0.50	Vdc
Base-Emitter On Voltage (I_C = 7.0 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	–	0.90	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 5 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	BF 371 BF 373	f_T	500 –	720 720	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	BF 371 BF 373	C_{re}	 –	0.23 0.20	 0.32	pF

POWER GAIN (SEE FIG.7)
(35 MHz)

FIG.1

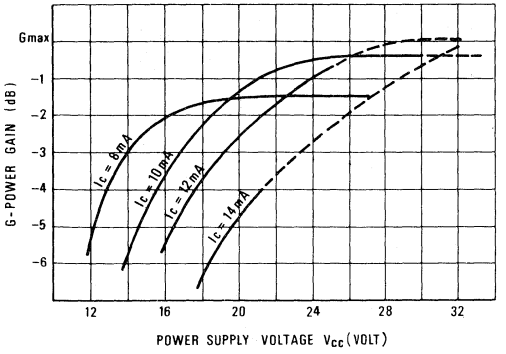
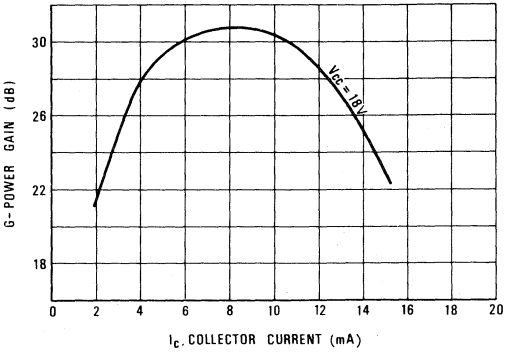


FIG. 2



COMMON – EMITTER Y PARAMETERS (f = 35 MHz, V_{CE}= 18 V_{DC}, T_A= 25°C)

FIG.3 - INPUT ADMITTANCE

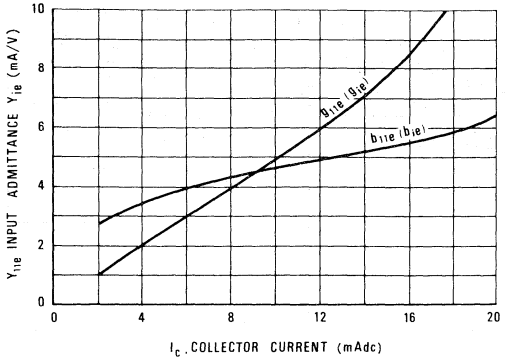


FIG.4 - REVERSE TRANSFER ADMITTANCE

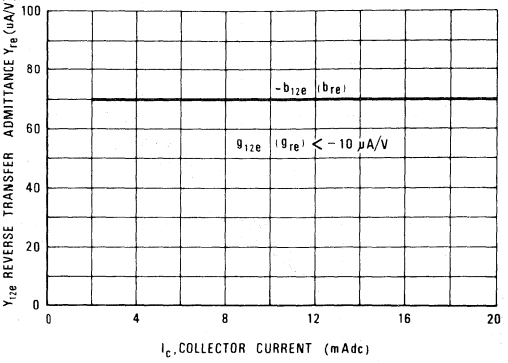


FIG. 5 - FORWARD TRANSFER ADMITTANCE

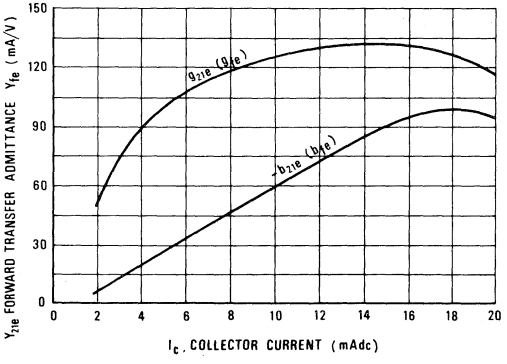


FIG. 6 - OUTPUT ADMITTANCE

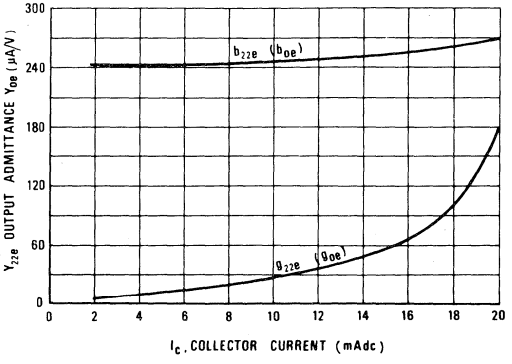
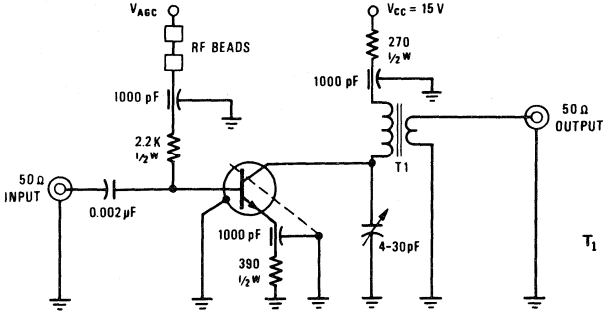


FIG. 7 - 35 MHz FUNCTIONAL TEST CIRCUIT
(UNNEUTRALIZED)



T_1 40/100 wire.
Primary 20 turns.
Secondary 3 turns.
Variable core.

FIG. 8 - VIDEO AMPLIFIER LINEARITY

(SEE FIG. 9)

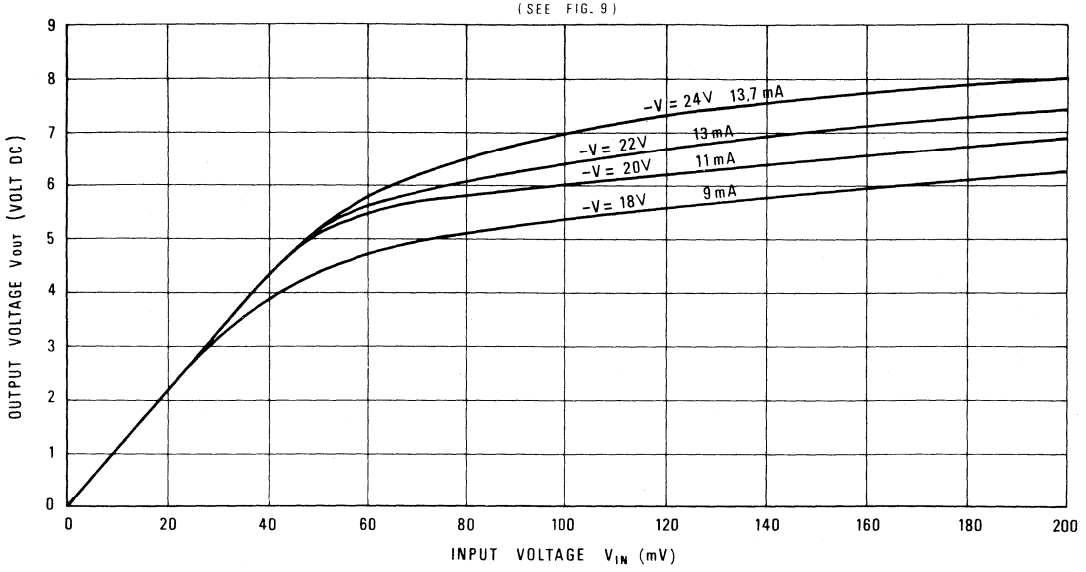
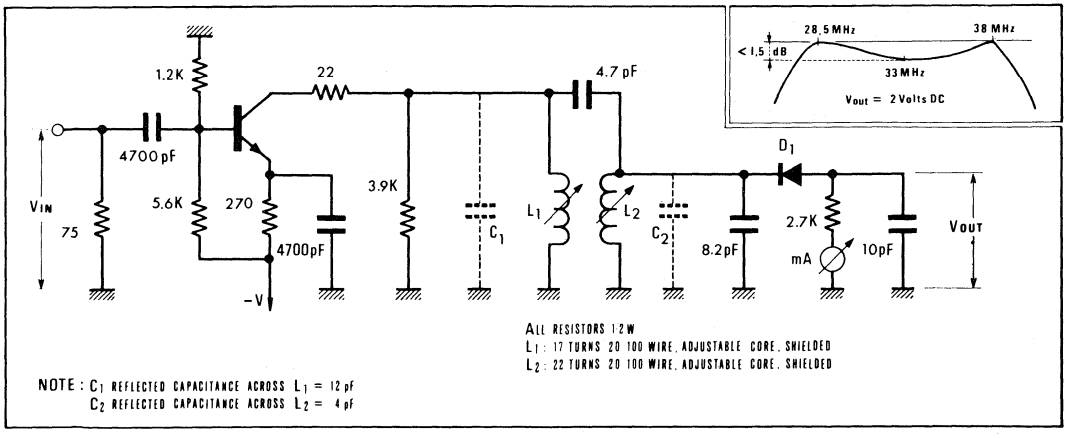


FIG. 9 - LINEARITY MEASUREMENT TEST CIRCUIT



BF374
BF375

NPN SILICON ANNULAR♦ TRANSISTOR

----designed for VHF/TV oscillator and FM/radio amplifier and oscillator applications.

- High Power Gain —
  G_{pe} = 20 dB (typical) at 200 MHz
- High Current Gain-Bandwidth Product —
  f_T = 800 MHz (typical)
- Low Collector — Base Capacitance —
  C_{cb} = 0.55 pF (typical)
- Complete y-Parameter Characterisation from 1 MHz to 100 MHz

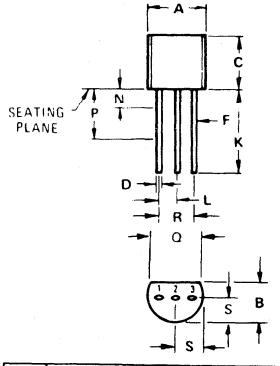
NPN SILICON VHF TRANSISTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW
Thermal Resistance, Junction to Case	θ_{JC}	0.125	°C/mW



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	25			Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	30			Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0			Vdc
Collector Cutoff Current (V_{CB} = 25 Vdc, I_E = 0)	I_{CBO}			100	nAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) BF374	h_{FE}	70		250	
BF375		35		120	
BF375C		70		120	
BF375D		35		90	
Collector-Emitter Saturation Voltage (I_C = 1.0 mAdc, I_B = 0.1 mAdc)	$V_{CE(sat)}$		50		mVdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			70		mVdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$		830		mVdc
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$		700		mVdc
(I_C = 10 mAdc, V_{CE} = 10 Vdc)			770		mVdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	800		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb} (C_{re})		0.55	0.6	pF
Collector-Base Time Constant (I_C = 4.0 mAdc, V_{CE} = 10 Vdc, f = 31.8 MHz)	r_bC_c		6		ps
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz, R_S = 50 ohms)	NF		4		dB
Common-Emitter Amplifier Power Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)	G_{pe}		20		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 10.7 MHz	f = 30 MHz	f = 100 MHz	Unit
G_{11e}	0.28	0.4	1.4	mmho
B_{11e}	0.6	1.6	5.0	mmho
G_{22e}	6.5	7	20	μmho
B_{22e}	0.1	0.3	1.0	mmho
G_{21e}	36	34	30	mmho
B_{21e}	− 0.8	− 2.5	− 9	mmho
B_{12e}	− 52	− 150	− 500	μmho

FIG. 1 — NORMALIZED DC CURRENT GAIN AT V_{CE} = 10 V

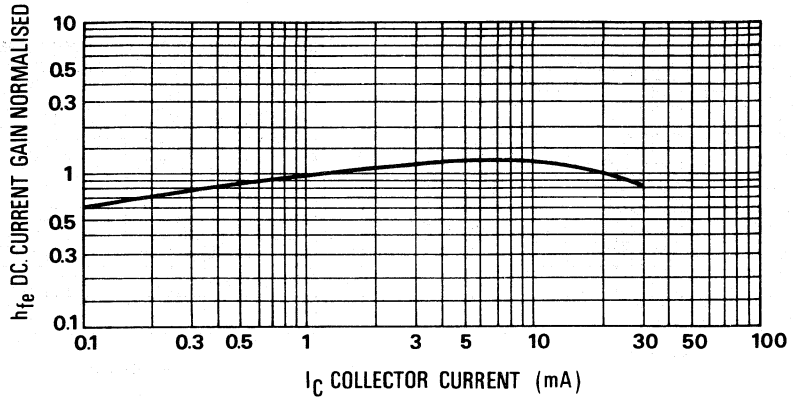


FIG. 2 — SATURATION AND ON VOLTAGE

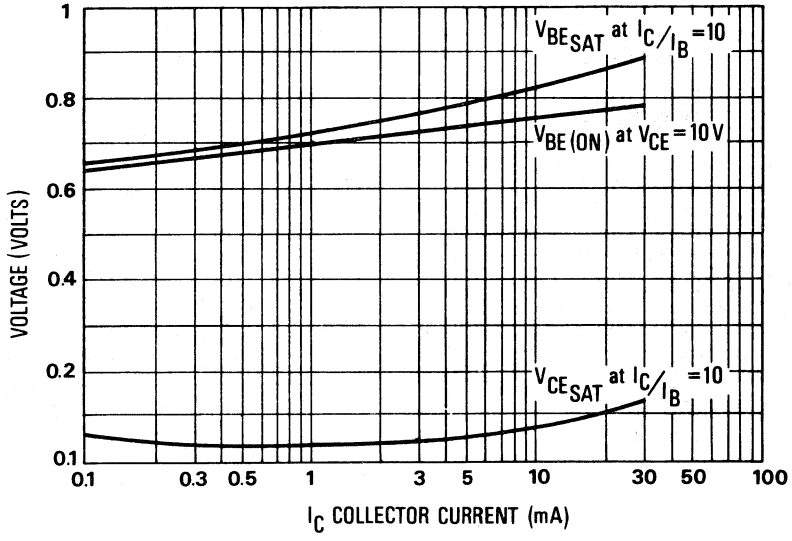


FIGURE 3 — INPUT ADMITTANCE
(Output short circuit)

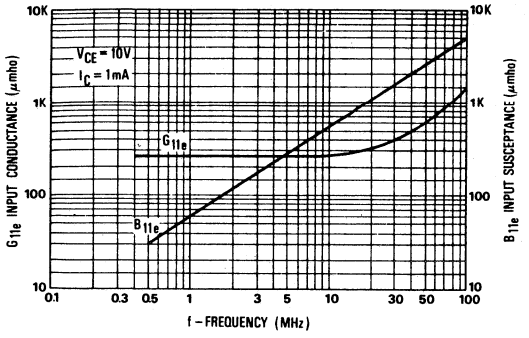


FIGURE 4 — OUTPUT ADMITTANCE
(Input short circuit)

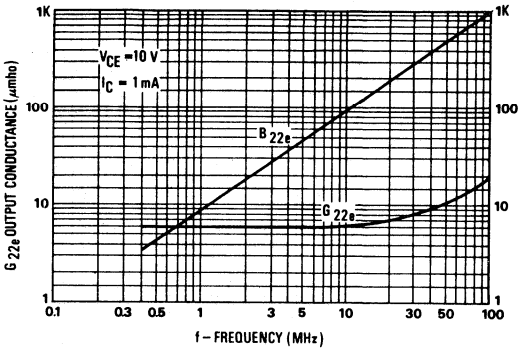


FIGURE 5 — FORWARD TRANSFER ADMITTANCE
(Output short circuit)

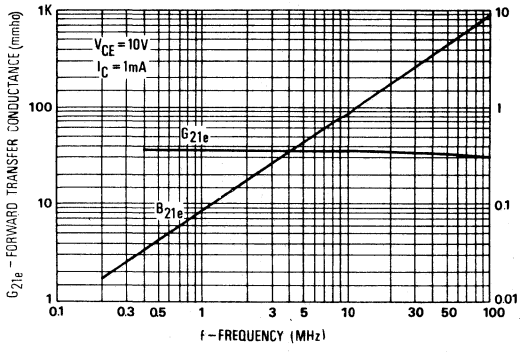
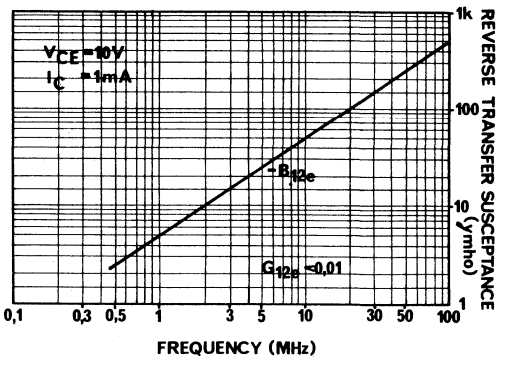


FIGURE 6 — REVERSE TRANSFER ADMITTANCE
(Input short circuit)



BF391
BF392 • BF393

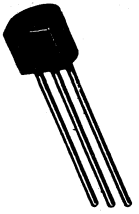
NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for high voltage video applications in television receivers requiring high breakdown voltage and low capacitance.

– High Collector-Emitter Breakdown Voltage @ I_C = 1.0 mAdc

BV_{CEO} = 200 Vdc BF 391
250 Vdc BF 392
300 Vdc BF 393

NPN SILICON HIGH VOLTAGE TRANSISTORS



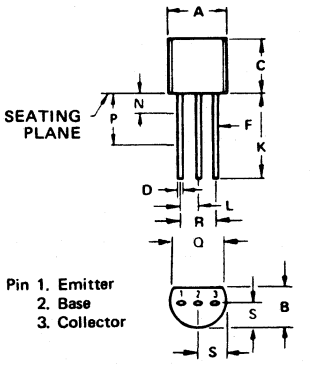
MAXIMUM RATINGS

Rating	Symbol	BF 391	BF 392	BF 393	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	300	Vdc
Collector-Base Voltage	V_{CB}	200	250	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	6.0	6.0	Vdc
Collector Current—Continuous	I_C	500			mAdc
Total Device Dissipation @T_A = 25 °C Derate Above 25 °C	P_D	625 1.2			mW mW/°C
Total Device Dissipation @T_C = 25 °C Derate Above 25 °C	P_D	1.5 12			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors Patented by Motorola Inc.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 10 mAdc, I_B = 0)	BF 391		200	–	
	BF 392		250	–	
	BF 393		300	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BF 391		200	–	
	BF 392		250	–	
	BF 393		300	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 100 μAdc, I_C = 0)	BF 391		6.0	–	
	BF 392		6.0	–	
	BF 393		6.0	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 160 Vdc, I_E = 0)	BF 391		–	0.1	
(V_{CB} = 200 Vdc, I_E = o)	BF 392		–	0.1	
(V_{CB} = 200 Vdc, I_E = 0)	BF 393		–	0.1	
Emitter Cutoff Current		I_{EBO}			μAdc
(V_{BE} = 4.0 Vdc, I_C = 0)	BF 391		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF 392		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF 393		–	0.1	
On Characteristics					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	All Types		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	All Types		40	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 mAdc, I_B = 2.0 mAdc)				2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 mA, I_B = 2.0 mA)				2.0	
Dynamic Characteristics					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz			50	–	
Collector-Base Capacitance		C_{re}			pF
(V_{CB} = 60 Vdc, I_E = 0, f = 1.0 MHz)				1.6	

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 – DC CURRENT GAIN

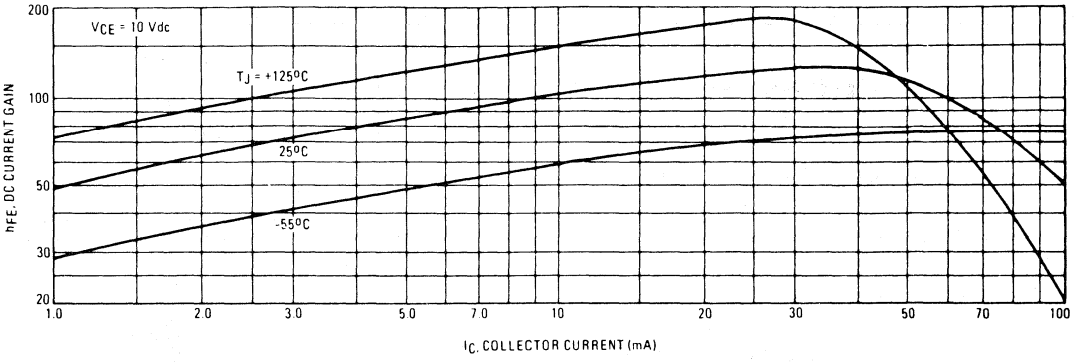


FIGURE 2 – CAPACITANCES

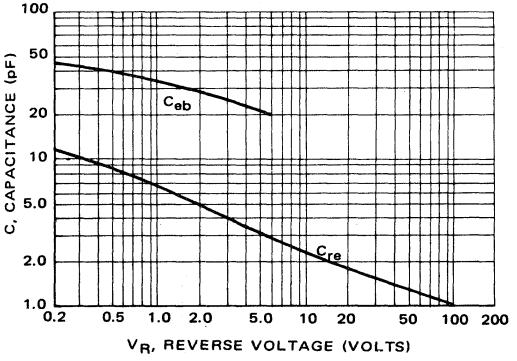


FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT

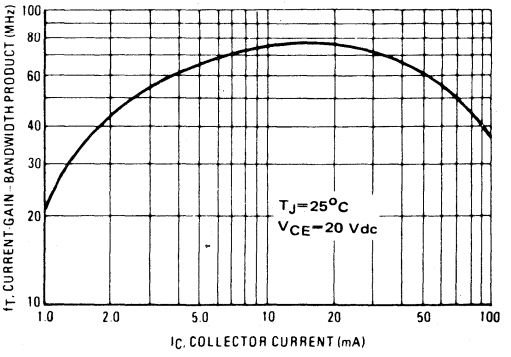


FIGURE 4 – "ON" VOLTAGES

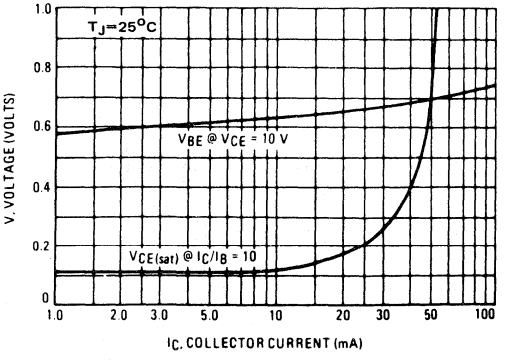
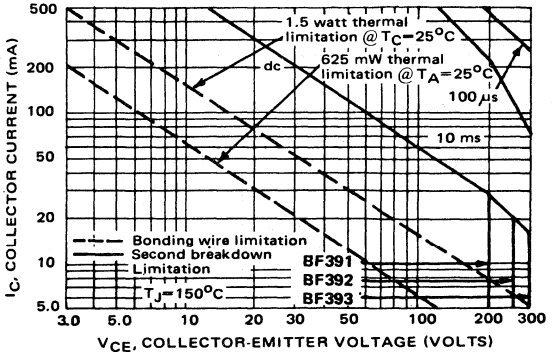


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



BF394
BF395

NPN SILICON ANNULAR♦ TRANSISTOR

---- designed as a common emitter amplifier for AM/FM radios.

- High Output Impedance
  — 140 Kohm typical at 470 KHz
  — 7.7 Kohm typical at 10.7 MHz
- Complete y-Parameter Characterisation from 400 KHz to 40 MHz
- Available in three 2 : 1 Gain Ranges

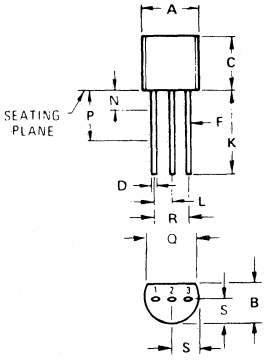
NPN SILICON
RF TRANSISTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation at T_A = 25°C Derate above 25°C	P_D	350 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	— 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	Θ_{JA}	0.357 max	°C/mW
Thermal Resistance, Junction to Case	Θ_{JC}	0.125 max	°C/mW



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	30			Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	30			Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5.0			Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}			100	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}			100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) BF394	h_{FE}	65		350	
BF394B		100	160	200	
BF395		35		125	
BF395C		65	95	125	
BF395D		35	65	75	
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) BF 394/BF 394 B	$V_{BE(on)}$	0.5	0.6	0.75	Vdc
BF 395/BF 395 C/BF 395 D		0.58	0.65	0.75	Vdc
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$		0.12	0.25	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 120 MHz)	f_T	80	180		MHz
Collector-Base Capacitance (common emitter feedback capacitance) (V_{CE} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb} (C_{re})		0.9		pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, R_S = 50 ohms, f = 1 MHz)	NF		1.7		dB

TYPICAL ADMITTANCE PARAMETERS (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, frequency as stated)

Symbol	f = 470 KHz	f = 10.7 MHz	f = 30 MHz	Unit
G_{11e}	200	260	600	μmho
B_{11e}	0.1	2.5	7.0	mmho
G_{22e}	4.0	4.7	9.0	μmho
B_{22e}	6.0	130	350	μmho
B_{12e}	− 5.0	− 110	− 300	μmho
G_{21e}	35	35	30	mmho
B_{21e}	—	− 0.7	− 2.0	mmho

FIG. 1 — NORMALIZED DC CURRENT GAIN

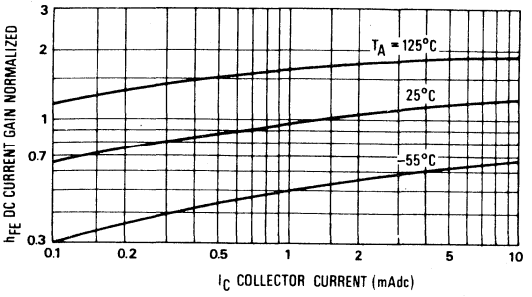


FIG. 2 — "ON" VOLTAGES

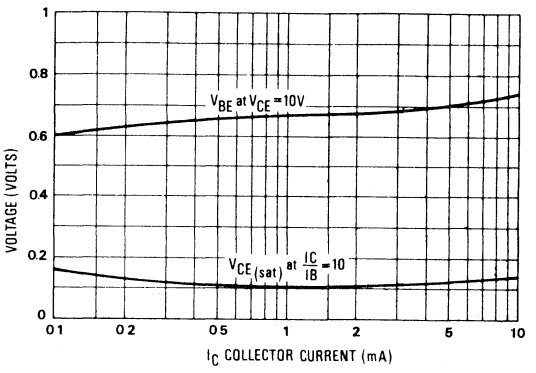


FIG. 3 — CURRENT GAIN — BANDWIDTH PRODUCT

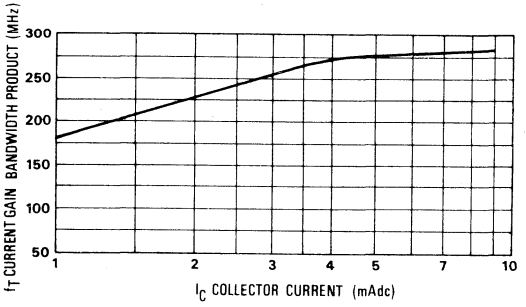


FIG. 4 — NOISE FIGURE

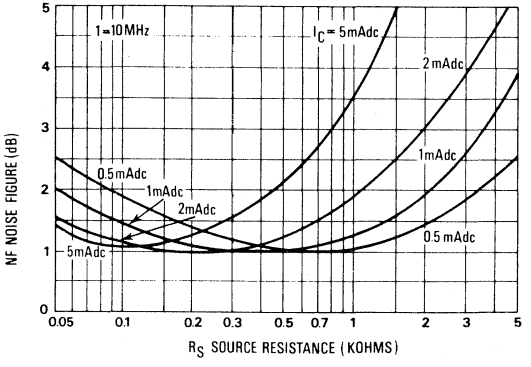


FIGURE 5 — INPUT ADMITTANCE
(Output short circuit)

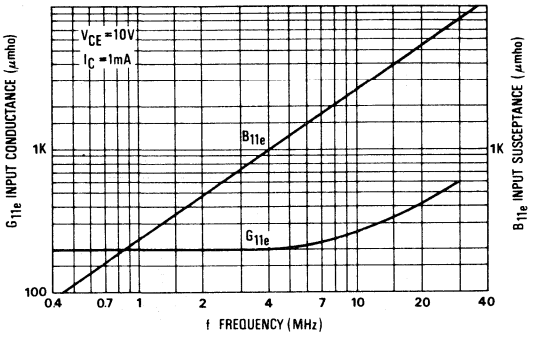


FIGURE 6 — OUTPUT ADMITTANCE
(Input short circuit)

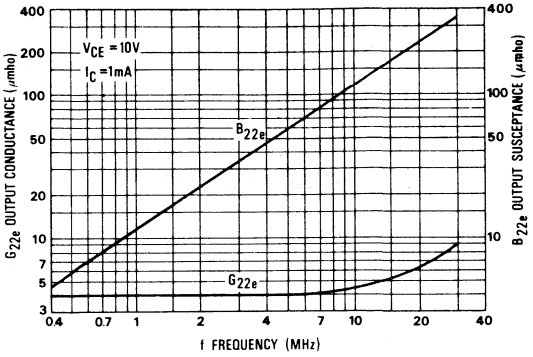


FIGURE 7 — FORWARD TRANSFER ADMITTANCE
(Output short circuit)

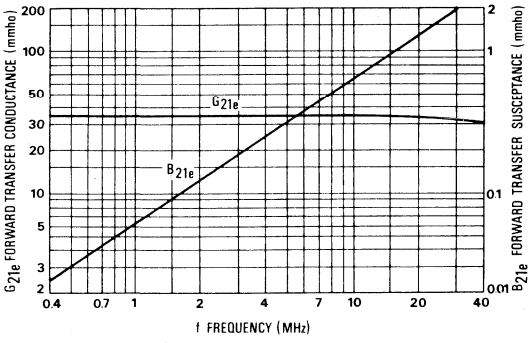
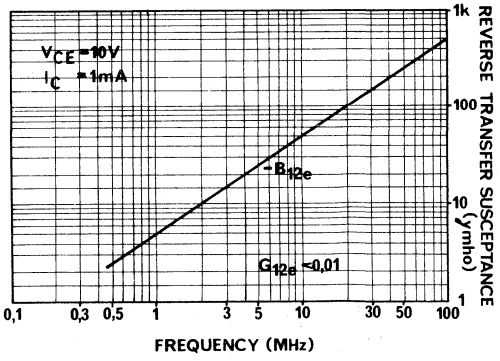


FIGURE 8 — REVERSE TRANSFER ADMITTANCE
(Input short circuit)



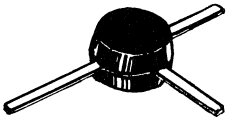
BF479

PNP SILICON ANNULAR♦ TRANSISTORS

... designed for common-base UHF RF amplifier applications.

- Guaranteed Noise Figure
  NF = 6 dB (Max) @ f = 800 MHz @ I_C = 10 mA
- Guaranteed Power Gain
  Gpb = 22 dB (Typ) @ f = 800 MHz
- Low Feedback Capacitance Allowing Stable Unneutralized Operation

PNP SILICON UHF TRANSISTORS



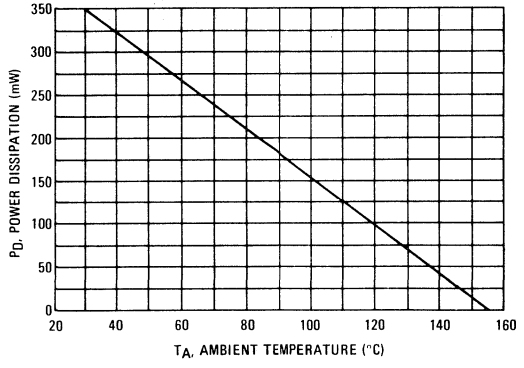
MAXIMUM RATINGS

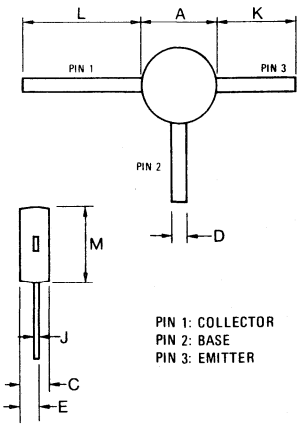
Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	350	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	°C/mW

FIGURE 1 – POWER DERATING





PIN 1: COLLECTOR
PIN 2: BASE
PIN 3: EMITTER

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.72	4.92	0.186	0.194
C	2.18	2.39	0.086	0.094
D	0.83	0.99	0.033	0.039
E	1.16	1.36	0.046	0.054
J	0.24	0.26	0.009	0.010
K	4.95	5.45	0.195	0.215
L	8.25	8.76	0.325	0.345
M	–	0.50	–	0.020

CASE 317A
STYLE 1

This is advance information and specifications are subject to change without notice.

♦Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	25	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	–	1.9	–	GHz
Collector Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}	–	0.67	–	pF
Noise Figure (I_C = 3 mAdc, V_{CB} = 10 Vdc, R_S = 50 Ohms) f = 200 MHz f = 800 MHz	NF	– –	2.0 3.5	– 5.5	dB
Noise Figure (I_C = 10 mAdc, V_{CB} = 10 Vdc, R_S = 50 Ohms) f = 200 MHz f = 800 MHz	NF	– –	3.0 4.5	– 6.0	dB
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (I_C = 10 mAdc, V_{CB} = 10 Vdc, R_S = 50 Ohms, f = 800 MHz)	G_{pb}	15	22	–	dB

FIGURE 2 – DC CURRENT GAIN

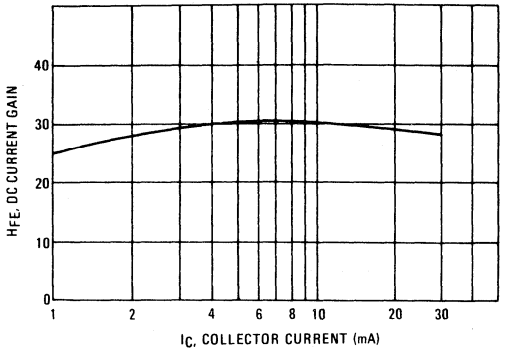


FIGURE 3 – COMMON BASE POWER GAIN

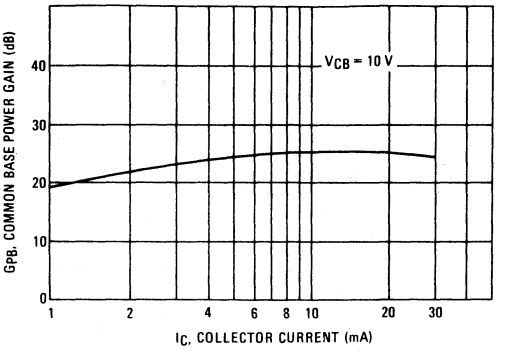


FIGURE 4 – CURRENT GAIN BANDWIDTH PRODUCT

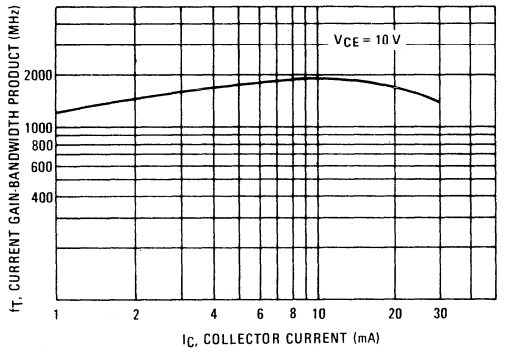


FIGURE 5 – NOISE FIGURE

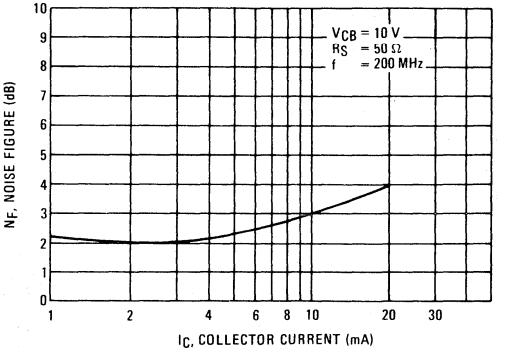
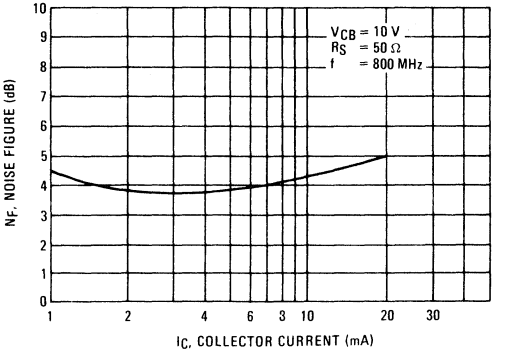


FIGURE 6 – NOISE FIGURE



TYPICAL COMMON BASE Y PARAMETERS

$T_A = 25\ °C$

FIGURE 7 – INPUT ADMITTANCE

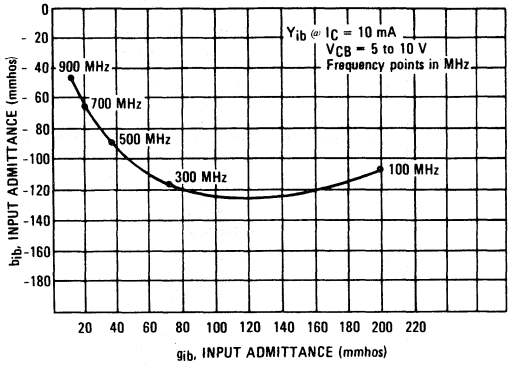


FIGURE 8 – REVERSE TRANSFER ADMITTANCE

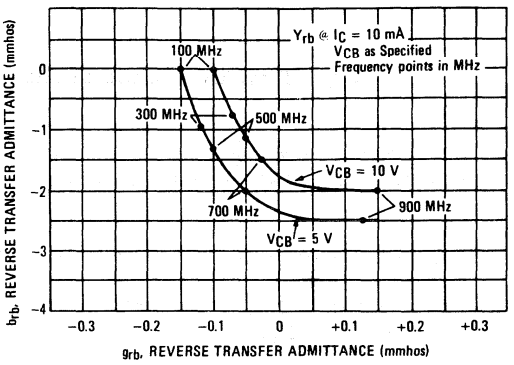


FIGURE 9 – FORWARD TRANSFER ADMITTANCE

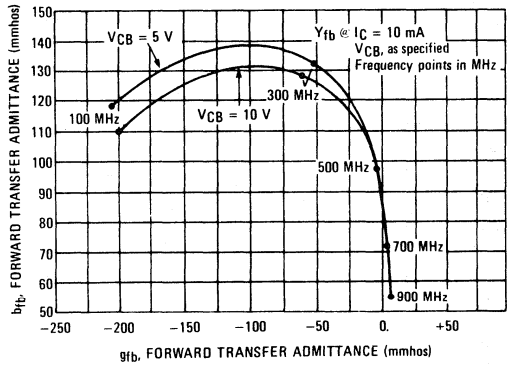
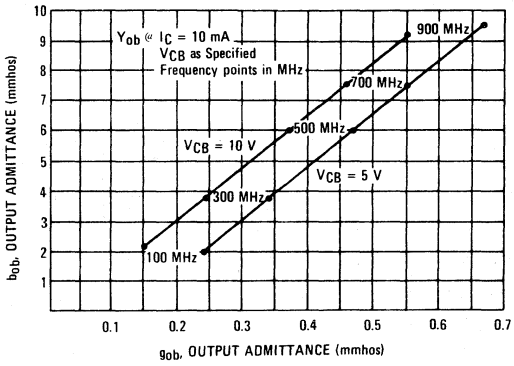


FIGURE 10 – OUTPUT ADMITTANCE



BF491
BF492 • BF493

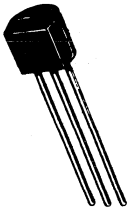
PNP SILICON HIGH VOLTAGE TRANSISTORS

SILICON ANNULAR♦ TRANSISTORS

. . . designed for high voltage video applications in television receivers requiring high breakdown voltage and low capacitance.

– High Collector-Emitter Breakdown Voltage @ I_C = 1.0 mAdc

BV_{CEO} =	200 Vdc	BF491
	250 Vdc	BF492
	300 Vdc	BF493



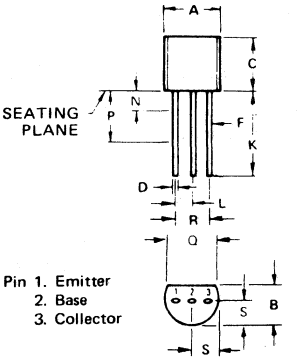
MAXIMUM RATINGS

Rating	Symbol	BF491	BF492	BF493	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	300	Vdc
Collector-Base Voltage	V_{CB}	200	250	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	8.0	8.0	Vdc
Collector Current—Continuous	I_C	500			mAdc
Total Device Dissipation @T_A = 25 °C Derate Above 25 °C	P_D	625 1.2			mW mW/°C
Total Device Dissipation @T_C = 25 °C Derate Above 25 °C	P_D	1.5 12			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	83.3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	200	°C/W

♦ Annular Semiconductors Patented by Motorola Inc.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Off Characteristics					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 1 mAdc, I_B = 0)	BF491		200	–	
	BF492		250	–	
	BF493		300	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	BF491		200	–	
	BF492		250	–	
	BF493		300	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 100 μAdc, I_C = 0)	BF491		6.0	–	
	BF492		8.0	–	
	BF493		8.0	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 160 Vdc, I_E = 0)	BF491		–	0.1	
(V_{CB} = 200 Vdc, I_E = o)	BF492		–	0.1	
(V_{CB} = 200 Vdc, I_E = 0)	BF493		–	0.1	
Emitter Cutoff Current		I_{EBO}			μAdc
(V_{BE} = 4.0 Vdc, I_C = 0)	BF491		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF492		–	0.1	
(V_{BE} = 6.0 Vdc, I_C = 0)	BF493		–	0.1	
On Characteristics					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	All Types		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	All Types		40	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 mAdc, I_B = 2.0 mAdc)				2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 mA, I_B = 2.0 mA)				2.0	
Dynamic Characteristics					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz			50	–	
Collector-Base Capacitance		C_{re}			pF
(V_{CB} = 100 Vdc, I_E = 0, f = 1.0 MHz)				1.6	

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 – DC CURRENT GAIN

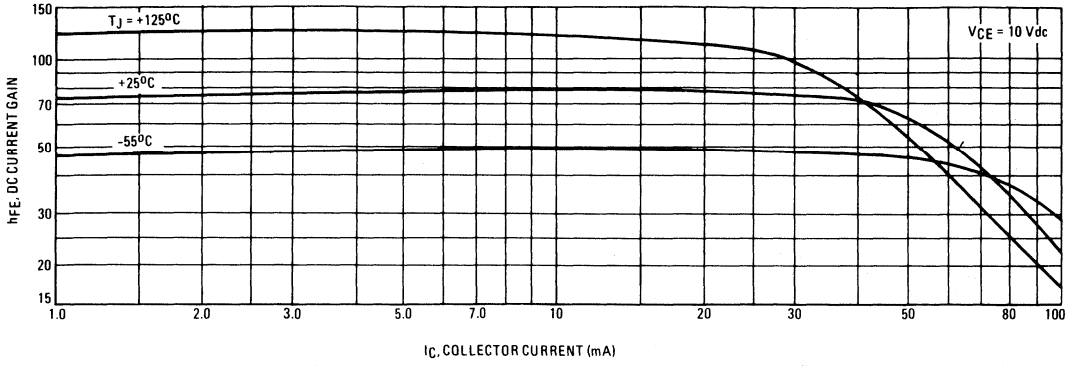


FIGURE 2 – CAPACITANCES

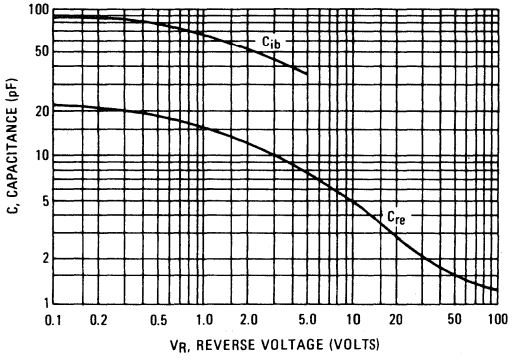


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

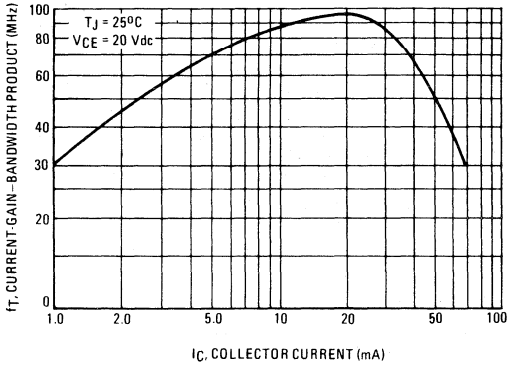


FIGURE 4 – "ON" VOLTAGES

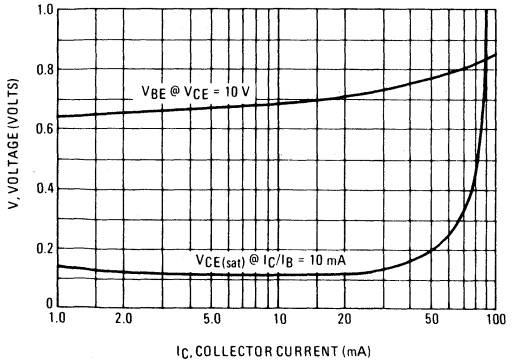
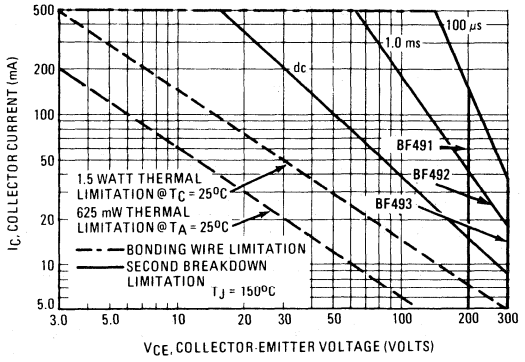


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

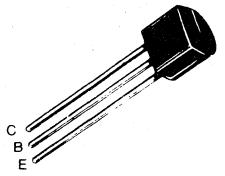


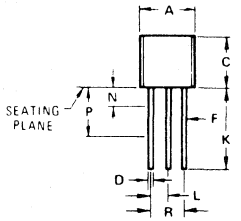
BF506

PNP SILICON ANNULAR♦ TRANSISTOR DESIGNED FOR TV TUNER APPLICATIONS AS VHF OSCILLATOR AND MIXER

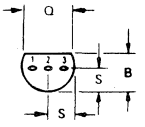
- High Oscillator Power
- Low Cross Modulation
- Plastic TO-92 Package

PNP SILICON VHF TRANSISTOR





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector current	I_C	50	mAdc
Total Device Dissipation @ $T_A = 25$ °C Derate above 25 °C	P_D	625 5.00	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

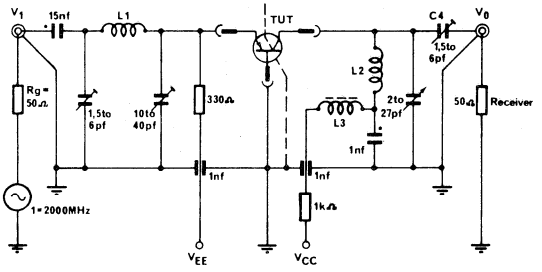
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	°C/mW

♦ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	600	–	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{CBO}	–	0.6	0.9	pF
Feedback Capacitance (Grounded Base) (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{rb}	–	0.15	0.25	pF
Noise Figure (I_C = 1 mA, R_S = 50 Ω, f = 200 MHz, V_{CC} = 6 V)	N_F	–	2.5	4	dB
Power Gain (I_C = 3 mA, R_L = 1 KΩ, f = 200 MHz, V_{CC} = 10.8 V)	G_{pb}	14	22	–	dB

200 MHz POWER GAIN NOISE FIGURE TEST CIRCUIT



*Leadless ceramic disc capacitor
L1 = 3 turns 0.0 mm enamel, 4 mm dia.
L2 = 2 turns 1 mm enamel, 6.5 mm dia.

FIGURE 1 – CURRENT GAIN – BANDWIDTH PRODUCT

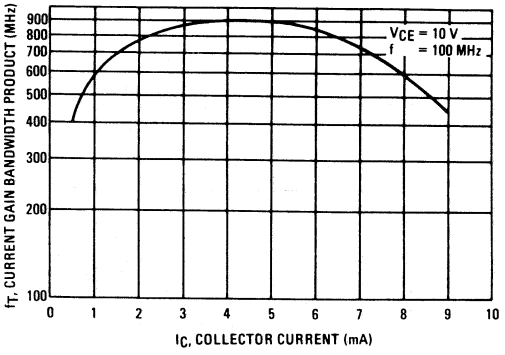


FIGURE 2 – NOISE FIGURE

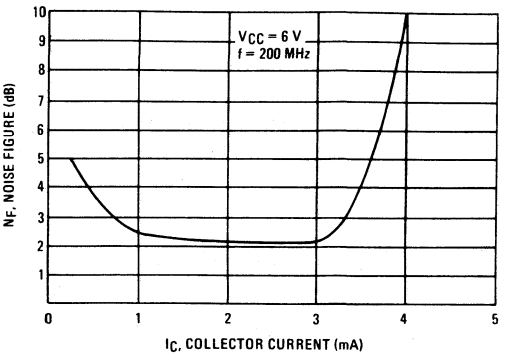


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

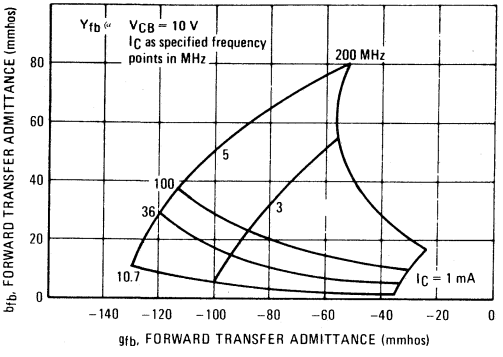


FIGURE 4 – INPUT ADMITTANCE

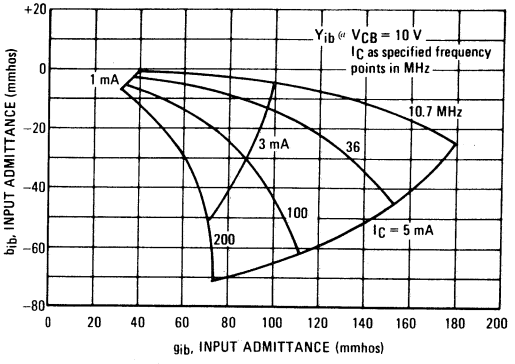
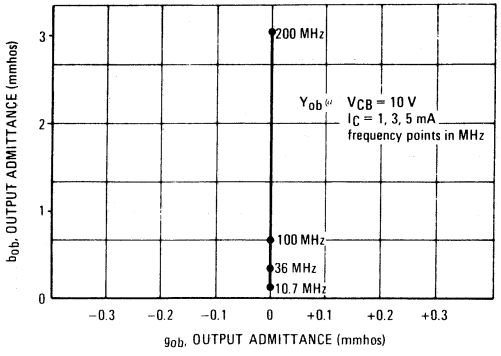


FIGURE 5 – OUTPUT ADMITTANCE



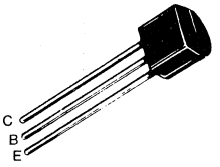
BF509

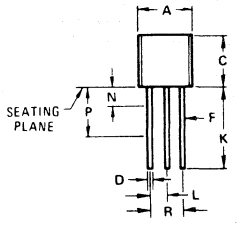
PNP SILICON ANNULAR♦ TRANSISTOR DESIGNED FOR TV TUNER APPLICATIONS

To be used as VHF Amplifier

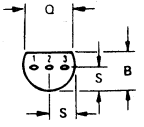
- High Power Gain
- Low Noise Figure
- Guaranteed AGC Range for 35 dB Gain Reduction at 200 MHz
- Plastic TO-92 Package

PNP SILICON VHF TRANSISTOR





STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	625 5.00	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	°C/mW

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦ Annular Semiconductors Patented by Motorola Inc.

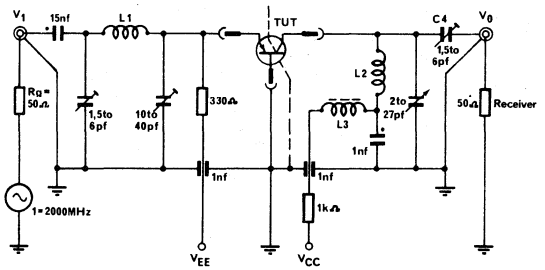
ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 3 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	600	850	–	MHz
Feedback Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{rb}	–	.15	.25	pF
Collector base capacitance (V_{CB} = 10 V, I_E =0, f = 1.0 MHz)	C_{CBO} (Cre)	–	0.6	0.9	pF
Noise Figure (I_C = 3 mAdc, V_{CC} = 10.8 V R_S = 50 Ohms, f = 200 MHz)	NF	–	–	2.5	dB
FUNCTIONAL TEST (see test jig fig 1)					
Common-base Amplifier Power Gain (I_C = 3 mAdc, V_{CC} = 10.8 V, R_L = 1 KΩ, f = 200 MHz)	G_{pb}	15	22	–	dB
Forward AGC Current $I_{C(Agc)}$ (Gain Reduction = 30 dB, R_S = 50 Ohms, V_{CC} = 10.8 V, f = 200 MHz)	$I_{C(Agc)}$	6	–	8.8	mAdc

AGC CHARACTERISTICS

V_{CC} = 10.8 Vdc, R_S = 50 Ohms, f = 200 MHz, See Figure 1 and 2.

200 MHz POWER GAIN NOISE FIGURE TEST CIRCUIT



*Leadless ceramic disc capacitor
L1 – 3 turns 0.0 mm enamel, 4 mm dia.
L2 = 2 turns 1 mm enamel, 6.5 mm dia.

FIGURE 1 – DC CURRENT GAIN

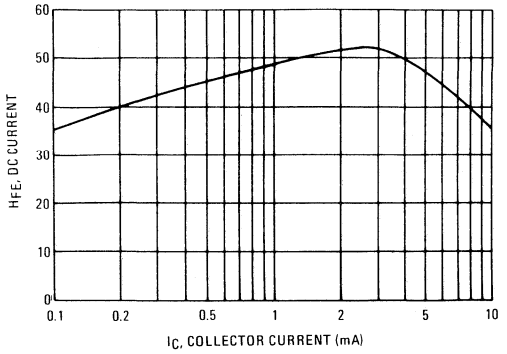


FIGURE 2 – CURRENT GAIN – BANDWIDTH PRODUCT

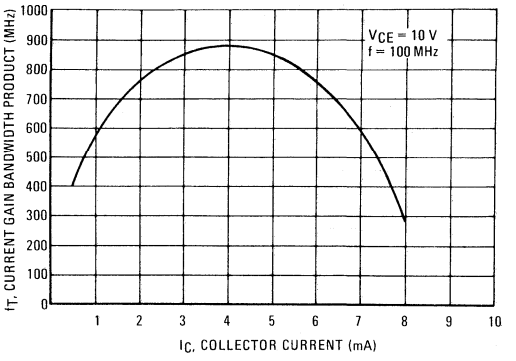


FIGURE 3 – CAPACITANCES

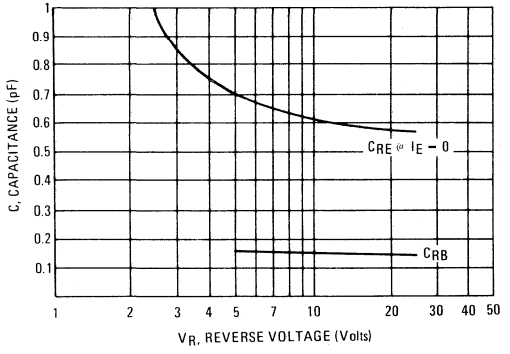


FIGURE 4 – TYPICAL POWER GAIN

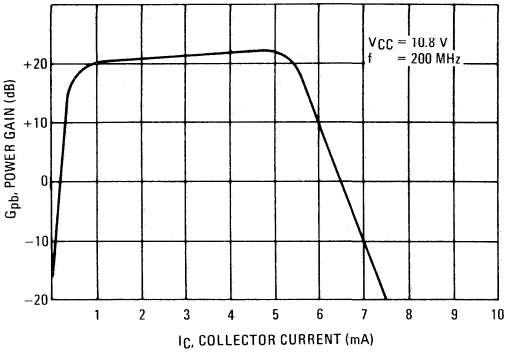


FIGURE 5 – FORWARD TRANSFER ADMITTANCE

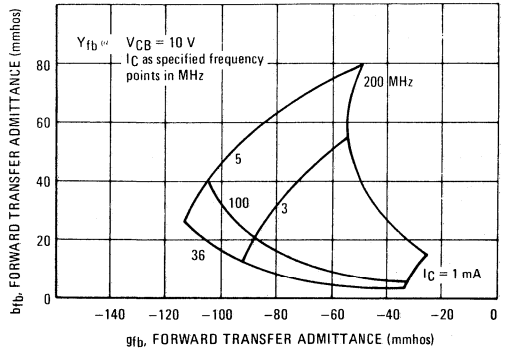


FIGURE 6 – INPUT ADMITTANCE

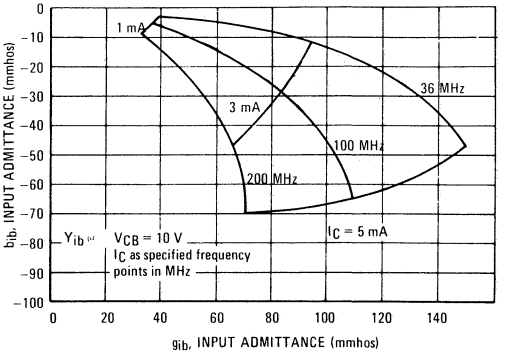
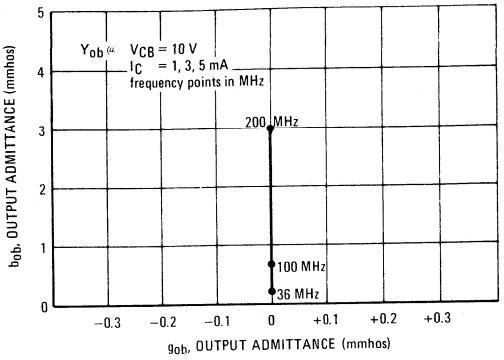


FIGURE 7 – OUTPUT ADMITTANCE



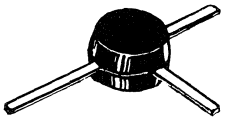
BF679

PNP SILICON ANNULAR♦ TRANSISTORS

. . . to be used as UHF AGC amplifier for frequencies up to 860 MHz or self oscillating mixer.

- Guaranteed Noise Figure
  NF = 5 dB (Max) @ f = 800 MHz
- Guaranteed Power Gain
  G_{pb} = 17 dB (Typ) @ f = 800 MHz
- Guaranteed AGC Range for 35 dB Gain Reduction at 850 MHz.

PNP SILICON UHF TRANSISTORS

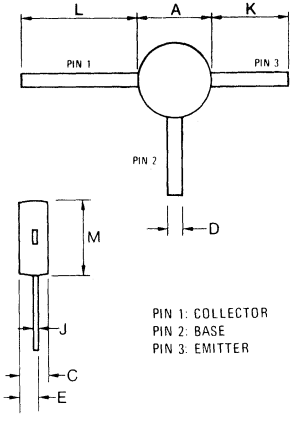


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	350	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

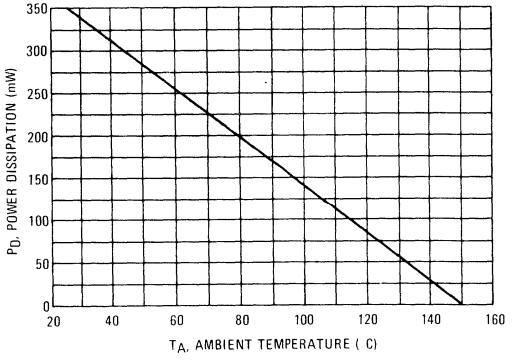
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	°C/mW



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.72	4.92	0.186	0.194
C	2.18	2.39	0.086	0.094
D	0.83	0.99	0.033	0.039
E	1.16	1.36	0.046	0.054
J	0.24	0.26	0.009	0.010
K	4.95	5.45	0.195	0.215
L	8.25	8.76	0.325	0.345
M	–	0.50	–	0.020

CASE 317A
STYLE 1

FIGURE 1 – POWER DERATING



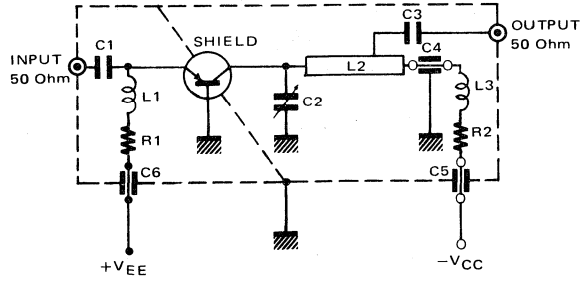
This is advance information and specifications are subject to change without notice.

♦Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	35	45	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 3 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	–	850	–	MHz
Feedback capacitance (Grounded emitter) (V_{CB} = 10 Vdc, I_B = 0, f = 1 MHz)	C_{re}	–	0.4	–	pF
Feedback Capacitance (Grounded base) (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{rb}	–	0.15	–	pF
Noise Figure (I_C = 3 mAdc, V_{CB} = 10 Vdc, R_S = 50 Ohms, f = 800 MHz)	NF	–	–	5	dB
FUNCTIONAL TEST					
Common-base Amplifier Power Gain (I_C = 3 mAdc, V_{CC} = 10 Vdc, R_L = 2 KΩ f = 800 MHz)	G_{pb}	12	17	–	dB
Forward AGC Current (V_{CC} = 10.8 V, Gain Reduction = 30 dB, R_S = 50 Ohms, R_L = 2 KΩ, f = 800 MHz)	I_{AGC}	6.4	–	7.8	mAdc

AGC CHARACTERISTICS R_S = 50 Ohms, f = 800 MHz.



C1 C3	160 pF
C5 C6	1000 pF FEEDTHROUGH
C2	0.4 – 0.6 pF JOHANSEN OR EQUIVALENT
R1	1.5 KΩ
R2	820 Ω
L2	SILVER PLATED BRASS ROD, 3 mm ϕ 20 mm LONG, TAP AT 9 mm FROM COLD END
C4	150 pF
L1 L3	10 TURNS, 24 WIRE, ϕ 3 mm

NOTE: FOR R_{out} = 50 OHM AND CORRECT TAPPING: R_L = 2 K OHM

FIGURE 2 – DC CURRENT GAIN

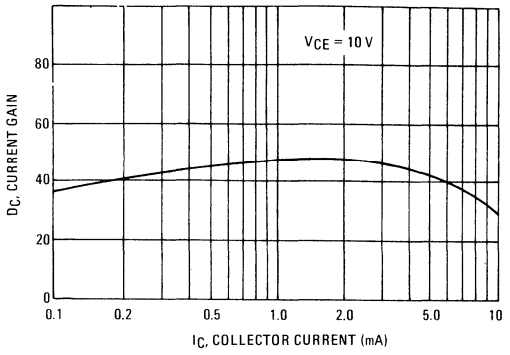


FIGURE 3 – CURRENT GAIN–BANDWIDTH PRODUCT

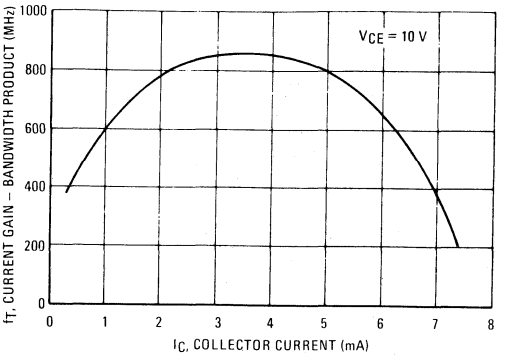


FIGURE 4 – CAPACITANCES

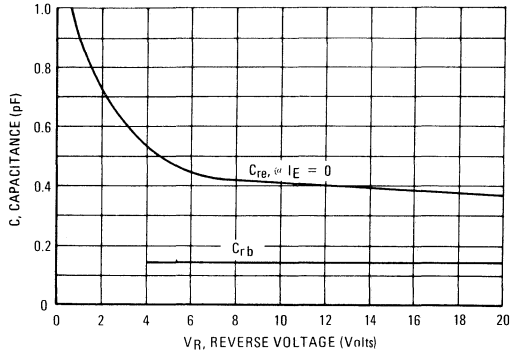


FIGURE 5 – NOISE FIGURE

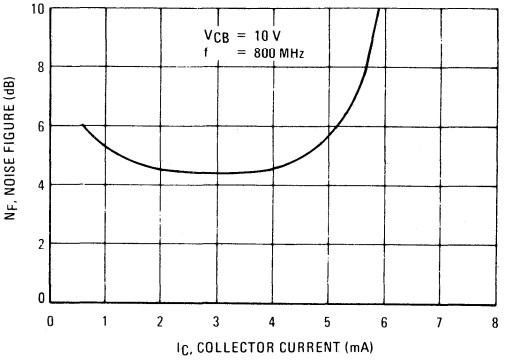


FIGURE 6 – POWER GAIN

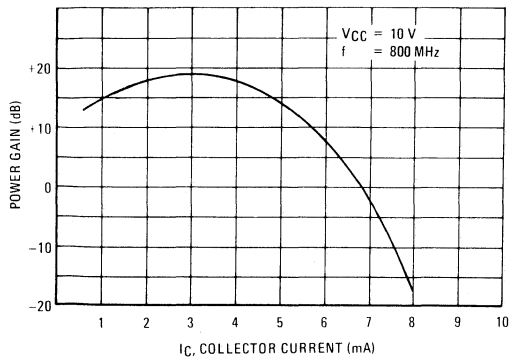


FIGURE 7 – INPUT ADMITTANCE

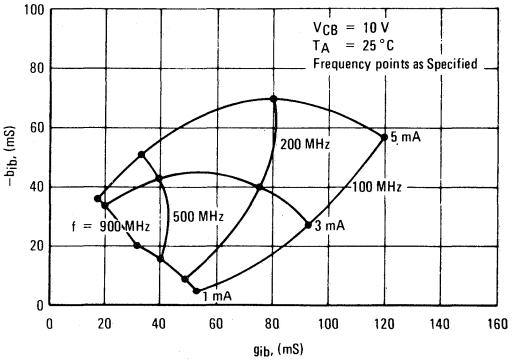


FIGURE 8 – OUTPUT ADMITTANCE

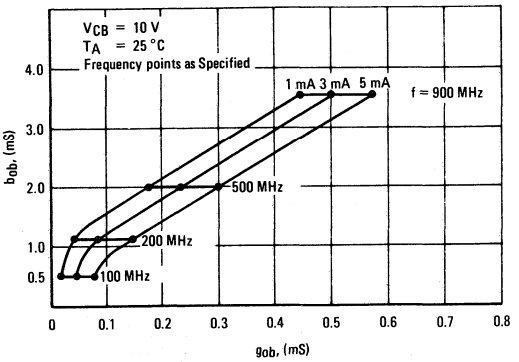
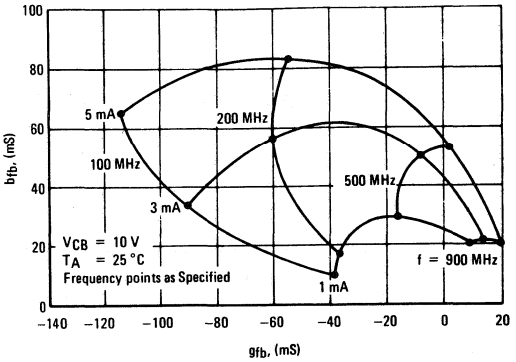


FIGURE 9 – FORWARD TRANSFER ADMITTANCE



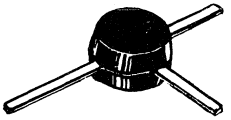
BF680

PNP SILICON ANNULAR♦ TRANSISTORS

. . . designed for TV tuner applications as UHF oscillator and/or mixer.

- High Oscillator Power up to 860 MHz.
- Guaranteed Power Gain
  G_{pb} = 17 dB (Typ) @ f = 800 MHz.

PNP SILICON UHF TRANSISTORS

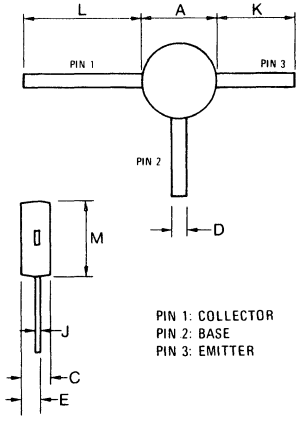


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	350	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	357	°C/mW

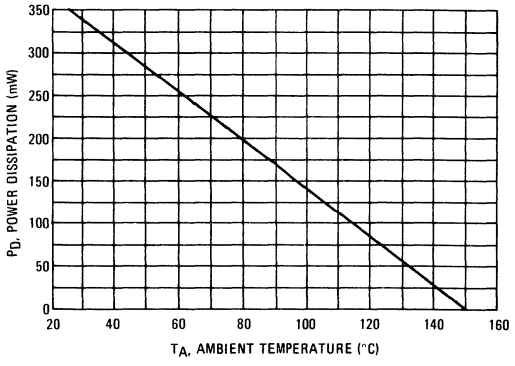


PIN 1: COLLECTOR
PIN 2: BASE
PIN 3: EMITTER

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.72	4.92	0.186	0.194
C	2.18	2.39	0.086	0.094
D	0.83	0.99	0.033	0.039
E	1.16	1.36	0.046	0.054
J	0.24	0.26	0.009	0.010
K	4.95	5.45	0.195	0.215
L	8.25	8.76	0.325	0.345
M	–	0.50	–	0.020

CASE 317A
STYLE 1

FIGURE 1 – POWER DERATING



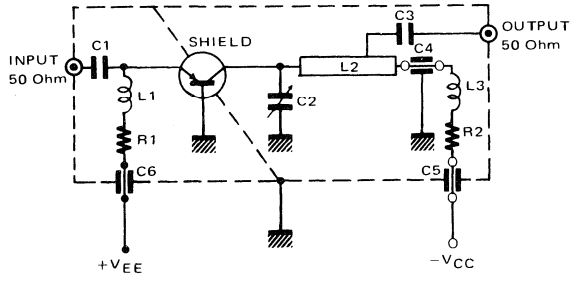
This is advance information and specifications are subject to change without notice.

♦Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	BV_{CEO}	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	h_{FE}	35	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 3 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	–	850	–	MHz
Feedback capacitance (Grounded emitter) (V_{CB} = 10 Vdc, I_B = 0, f = 1 MHz)	C_{re}	–	0.4	–	pF
Feedback Capacitance (Grounded base) (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{rb}	–	0.15	–	pF
Noise Figure (I_C = 3 mAdc, V_{CB} = 10 Vdc, R_S = 50 Ohms, f = 800 MHz)	NF	–	5	–	dB
FUNCTIONAL TEST					
Common-base Amplifier Power Gain (I_C = 3 mAdc, V_{CC} = 10 Vdc, R_L = 2 KΩ, f = 800 MHz	G_{pb}	–	17	–	dB

TEST CIRCUIT POWER GAIN AND NOISE FIGURE
(R_S = 50 Ω, f = 800 MHz)



C1 C3	160 pF
C5 C6	1000 pF FEEDTHROUGH
C2	0.4 – 0.6 pF JOHANSEN OR EQUIVALENT
R1	1.5 KΩ
R2	820 Ω
L2	SILVER PLATED BRASS ROD, 3 mm ϕ 20 mm LONG, TAP AT 9 mm FROM COLD END
C4	150 pF
L1 L3	10 TURNS, 24 WIRE, ϕ 3 mm

NOTE: FOR R_{out} = 50 OHM AND CORRECT TAPPING: R_L = 2 K OHM

Characteristic	Symbol	Min.	Typ.	Max.	Unit
SUMMARY COMMON BASE–Y PARAMETERS (V_{CE} = 10 Vdc, I_C = 3 mAdc, f = 500 MHz)					
Input Conductance	g_{ib}	–	40	–	mmhos
Input Susceptance	$-b_{ib}$	–	43	–	mmhos
Forward Transfer Admittance Magnitude	$\|Y_{fb}\|$	–	53	–	mmhos
Forward Transfer Admittance Phase Angle	ϕ_{fb}	–	95	–	degrees
Output Conductance	g_{ob}	–	25	–	mmhos
Output Susceptance	b_{ob}	–	2.0	–	mmhos
SUMMARY COMMON BASE–Y PARAMETERS (V_{CE} = 10 Vdc, I_C = 3 mAdc, f = 800 MHz)					
Input Conductance	g_{ib}	–	23	–	mmhos
Input Susceptance	$-b_{ib}$	–	31	–	mmhos
Forward Transfer Admittance Magnitude	$\|Y_{fb}\|$	–	31	–	mmhos
Forward Transfer Admittance Phase Angle	ϕ_{fb}	–	65	–	degrees
Output Conductance	g_{ob}	–	0.51	–	mmhos
Output Susceptance	b_{ob}	–	3.5	–	mmhos

FIGURE 2 – DC CURRENT GAIN

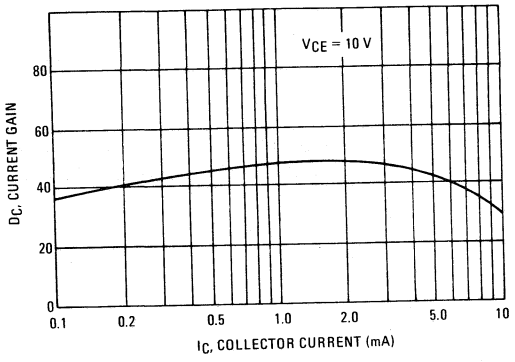


FIGURE 3 – CURRENT GAIN–BANDWIDTH PRODUCT

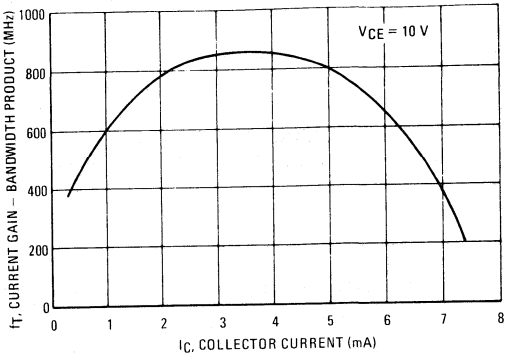
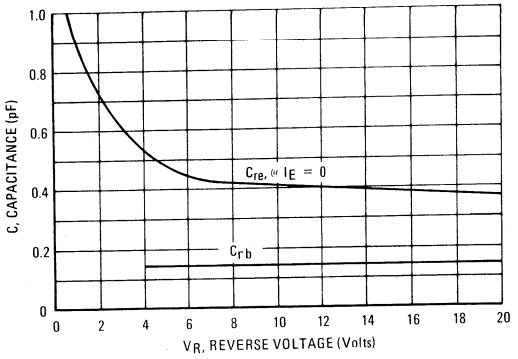


FIGURE 4 – CAPACITANCES



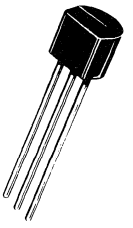
MPS-A05, MPS-A06 (NPN)
MPS-A55, MPS-A56 (PNP)

COMPLEMENTARY SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for use as medium-power driver and low-power outputs.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-A05, MPS-A55
  = 80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-A06, MPS-A56
- Excellent Current-Gain Linearity –
  1.0 mAdc to 150 mAdc – MPS-A55, MPS-A56
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.25 Vdc (Max) @ I_C = 100 mAdc

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS



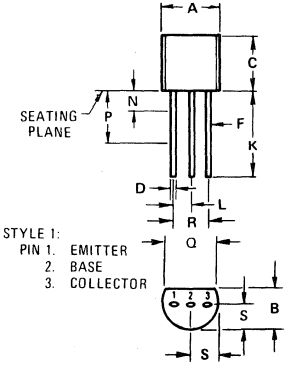
MAXIMUM RATINGS

Rating	Symbol	MPS-A05 MPS-A55	MPS-A06 MPS-A56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	500		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Temperature Temperature Range	T_J,T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(1)	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	oC/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

♦Annular Semiconductors Patented by Motorola Inc.

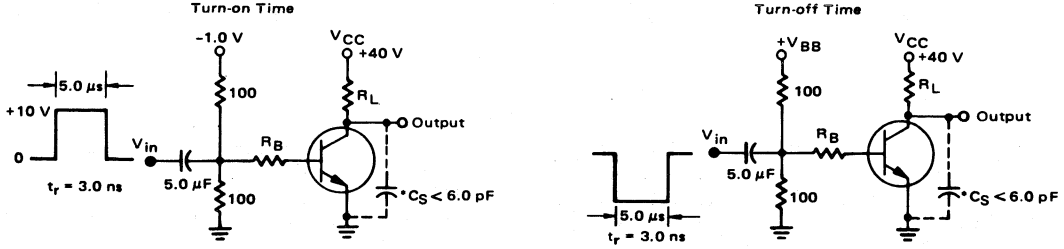
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	MPS-A05, MPS-A55	BV_{CEO}	60	–	Vdc
	MPS-A06, MPS-A56		80	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)		I_{CEO}	–	0.1	μAdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MPS-A05, MPS-A55		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MPS-A06, MPS-A56		–	0.1	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			50	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	–	0.25	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 10 mAdc, V_{CE} = 2.0 Vdc, f = 100 MHz)		f_T	100	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS

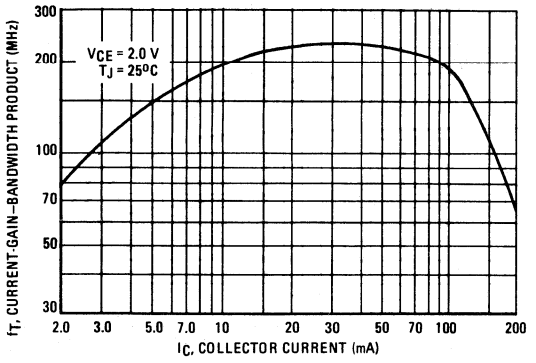


*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

NPN
MPS-A05, MPS-A06

PNP
MPS-A55, MPS-A56

FIGURE 2 – CURRENT-GAIN–BANDWIDTH PRODUCT



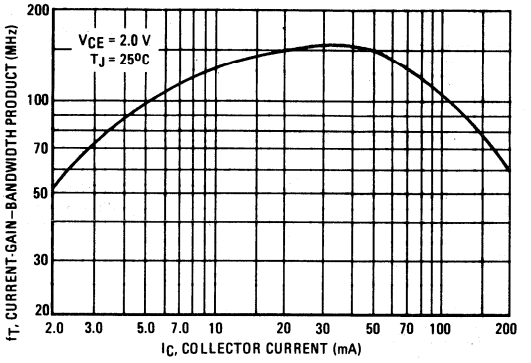
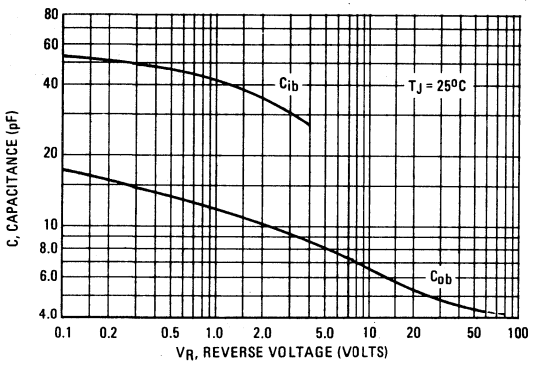


FIGURE 3 – CAPACITANCE



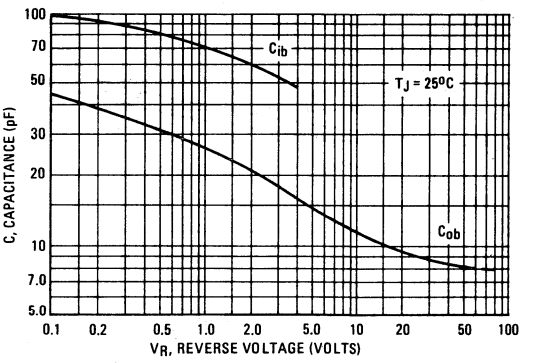
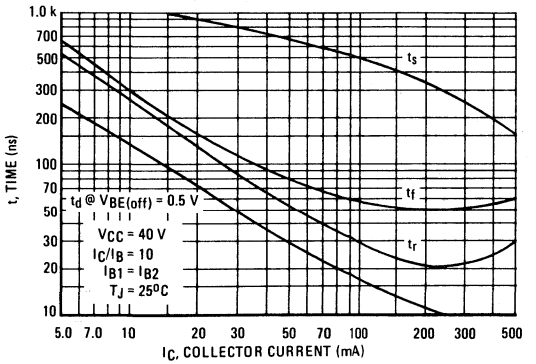


FIGURE 4 – SWITCHING TIME



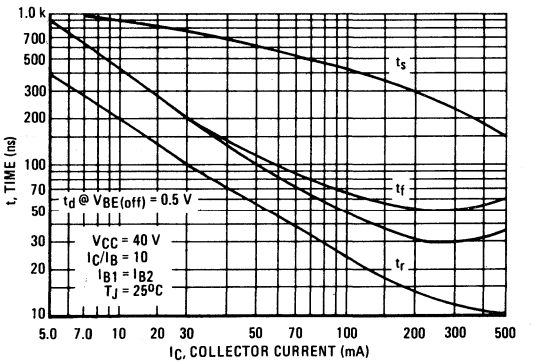


FIGURE 5 – THERMAL RESPONSE

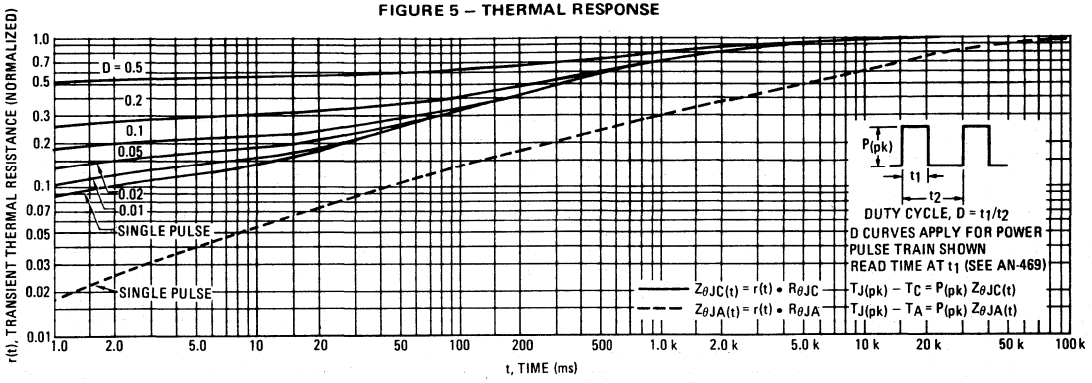
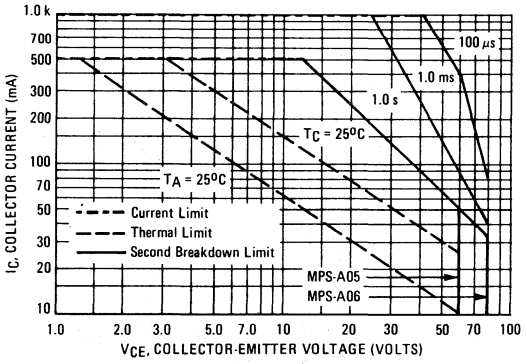
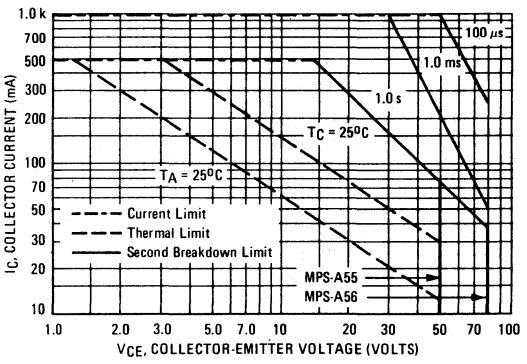


FIGURE 6 – ACTIVE – REGION SAFE OPERATING AREA

MPS-A05, MPS-A06



MPS-A55, MPS-A56



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 6 is based upon $T_{J(pk)} = 150^oC$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown. (See AN-415A)

NPN
MPS-A05, MPS-A06

FIGURE 7 – DC CURRENT GAIN

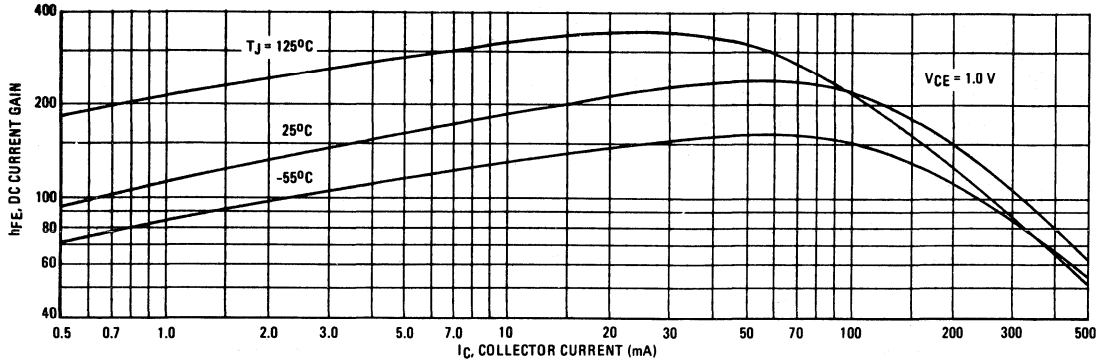


FIGURE 8 – "ON" VOLTAGES

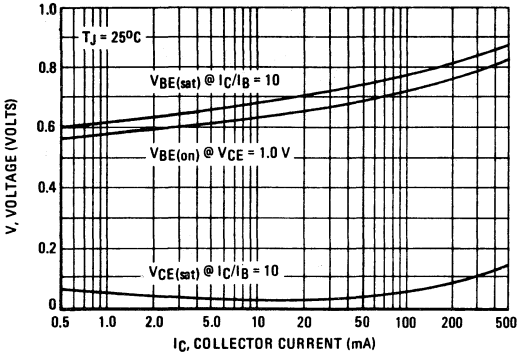


FIGURE 9 – COLLECTOR SATURATION REGION

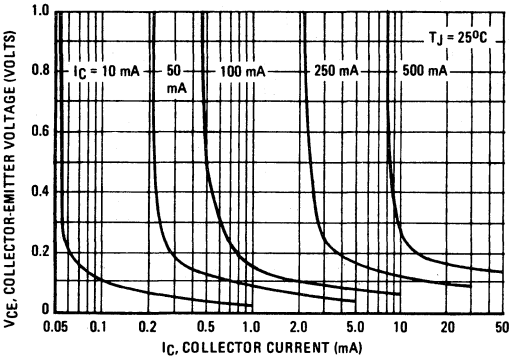
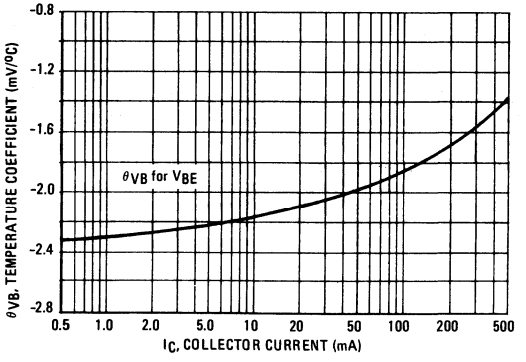


FIGURE 10 – BASE-EMITTER TEMPERATURE COEFFICIENT



PNP
MPS-A55, MPS-A56

FIGURE 11 – DC CURRENT GAIN

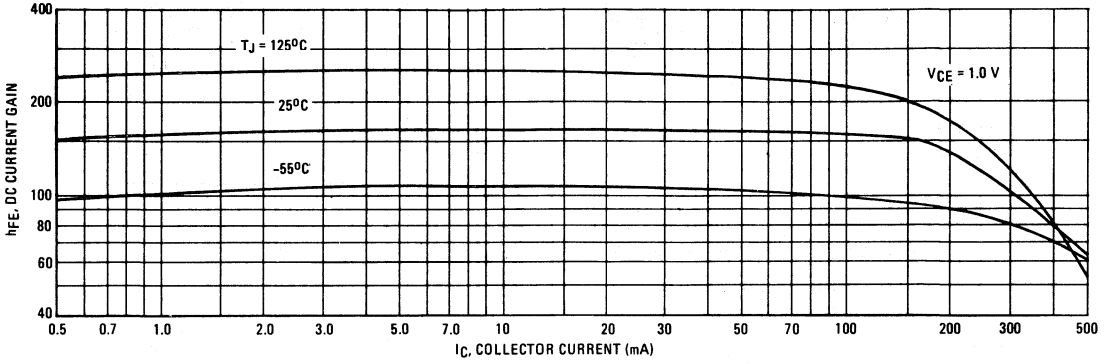


FIGURE 12 – "ON" VOLTAGES

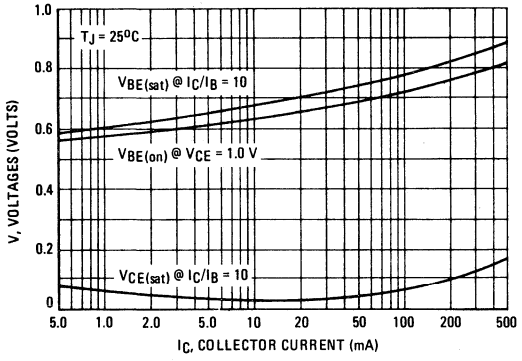


FIGURE 13 – COLLECTOR SATURATION REGION

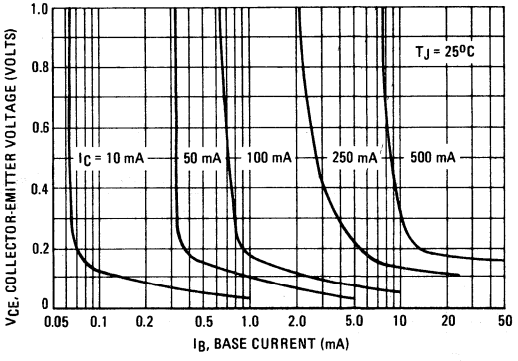
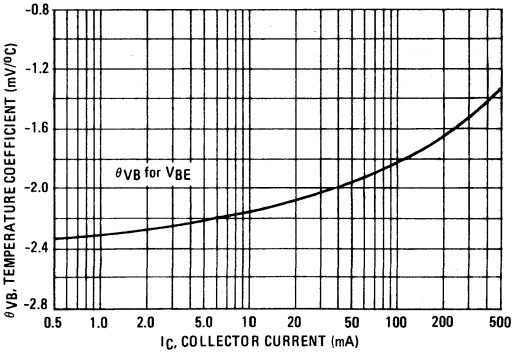


FIGURE 14 – BASE-EMITTER TEMPERATURE COEFFICIENT



MPS-A13
MPS-A14

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for pre-amplifier input applications requiring high input impedance.

- High DC Current Gain –
  h_{FE} = 5,000 (Min) @ I_C = 10 mAdc (MPS-A13)
  10,000 (Min) @ I_C = 10 mAdc (MPS-A14)
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 30 Vdc (Min) @ I_C = 10 mAdc
- Low Noise Figure –
  NF = 2.0 dB (Typ) @ I_C = 1.0 mAdc
- Monolithic Construction for High Reliability

NPN SILICON DARLINGTON TRANSISTORS

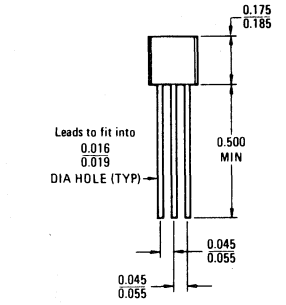
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}*	30	Vdc
Collector-Emitter Voltage	V_{CES}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current – Continuous	I_C	300	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	500 4.54	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.220	°C/mW

*Due to the monolithic construction of this device, breakdown voltages of both transistors are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



CASE 29 (1)
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, I_B = 0)		BV_{CES}	30	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)		I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A13		5000	–	–	
	MPS-A14		10,000	–	–	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A13		10,000	–	–	
	MPS-A14		20,000	–	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 0.1 mAdc)		$V_{CE(sat)}$	–	0.8	1.5	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.25	2.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	125	200	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	5.0	–	pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 100 k ohms, f = 1.0 kHz)		NF	–	2.0	–	dB

FIGURE 1 – NORMALIZED DC CURRENT GAIN

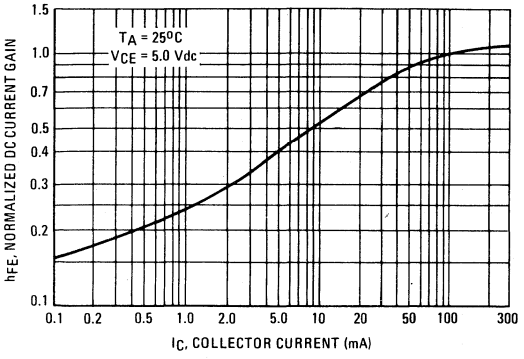


FIGURE 2 – BASE-EMITTER "ON" VOLTAGE

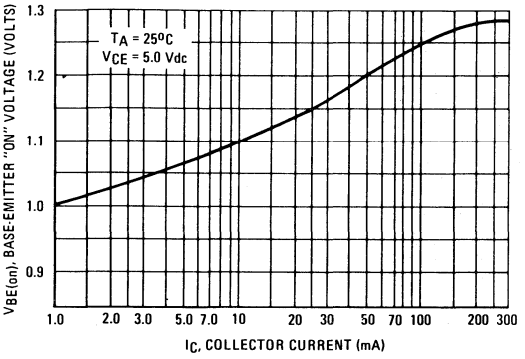


FIGURE 3 – TRANSCONDUCTANCE versus FREQUENCY

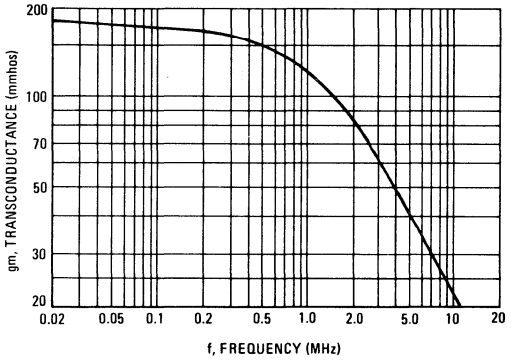


FIGURE 4 – NOISE FIGURE versus CURRENT

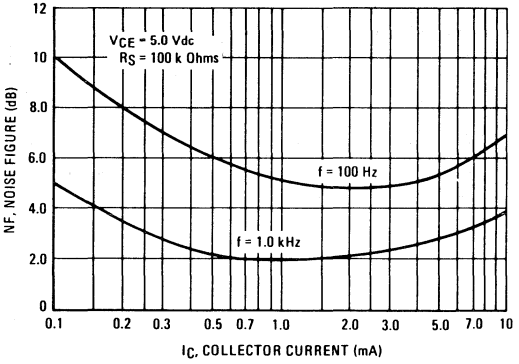


FIGURE 5 – NOISE FIGURE versus FREQUENCY

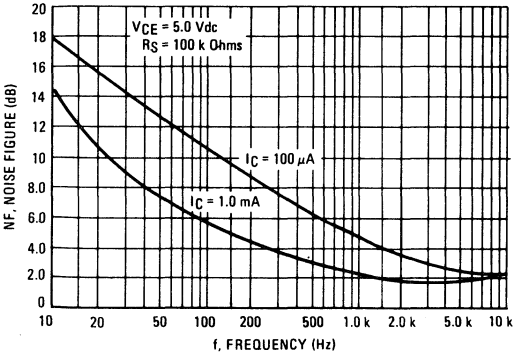
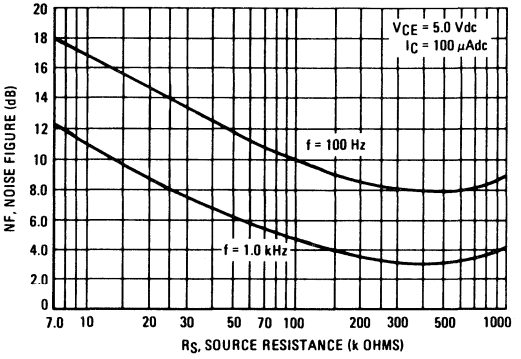


FIGURE 6 – NOISE FIGURE versus SOURCE RESISTANCE



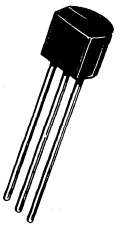
MPS-A16
MPS-A17

NPN SILICON ANNULAR♦ TRANSISTORS

. . . designed for use in moderate speed switching and clipping applications that require large input voltage capability.

- High-Emitter-Base Breakdown Voltage –
  BV_{EBO} = 12 Vdc (Min) @ I_E = 0.1 mAdc – MPS-A16
  = 15 Vdc (Min) @ I_E = 0.1 mAdc – MPS-A17

NPN SILICON TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	MPS-A16	MPS-A17	Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Emitter-Base Voltage	V_{EB}	12	15	Vdc
Collector Current – Continuous	I_C	100		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.73		mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

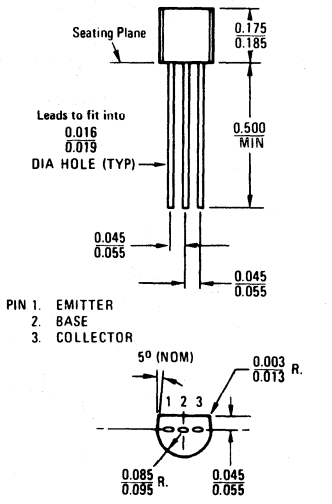
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)		BV_{CEO}	40	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	MPS-A16 MPS-A17	BV_{EBO}	12 15	– –	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{BE} = 10 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc)		h_{FE}	200	600	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	–	0.25	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	MPS-A16 MPS-A17	f_T	100 80	– –	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	4.0	pF

♦Annular Semiconductors Patented by Motorola Inc.



To convert inches to millimeters multiply by 25.4

All JEDEC dimensions and notes apply

CASE 29-01
TO-92
PLASTIC

FIGURE 1 – DC CURRENT GAIN

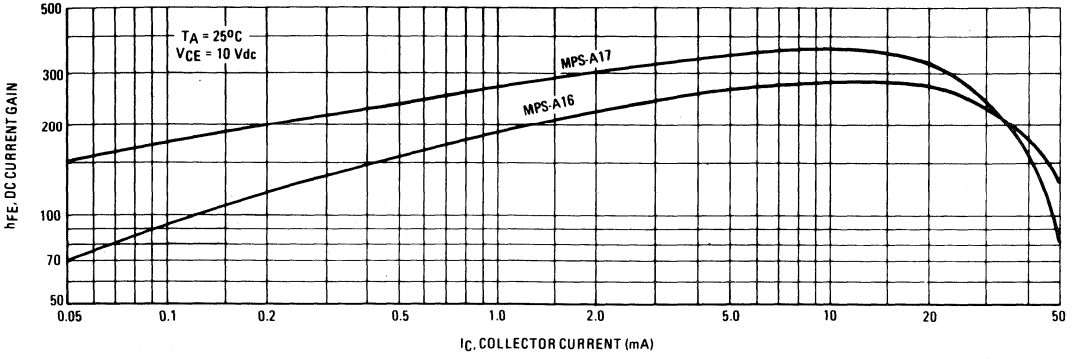


FIGURE 2 – SMALL SIGNAL CURRENT GAIN

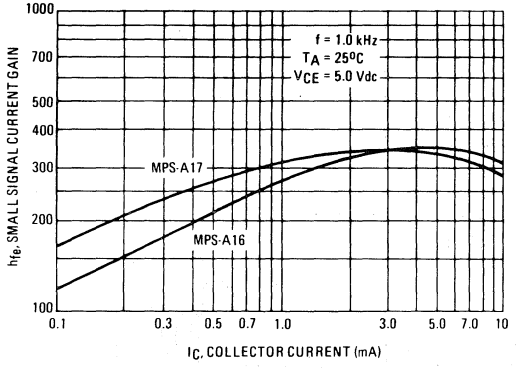


FIGURE 3 – SATURATION AND ON VOLTAGES

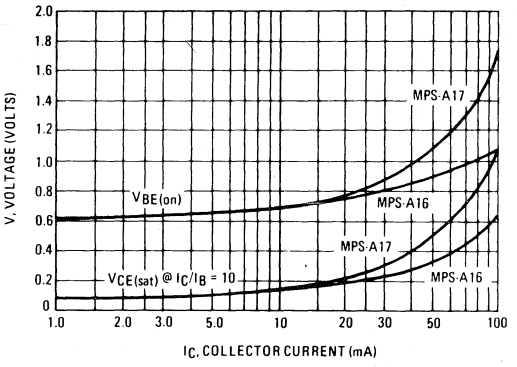


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT

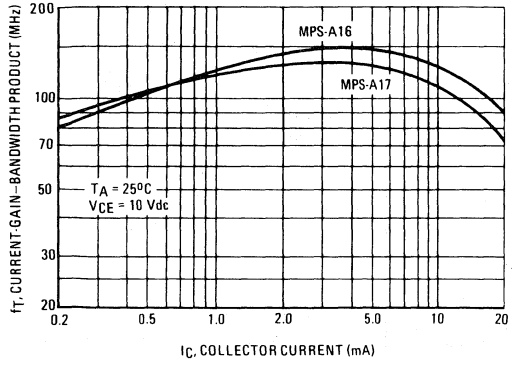
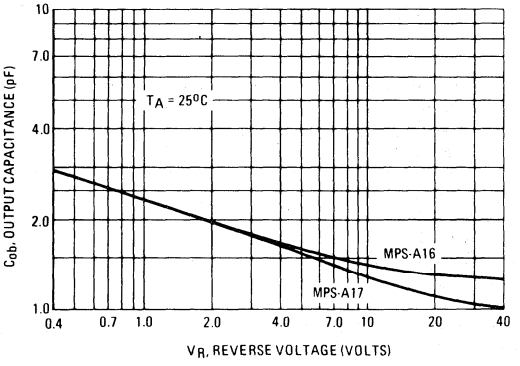


FIGURE 5 – OUTPUT CAPACITANCE



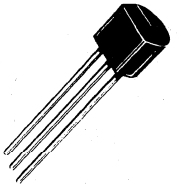
MPS-A62
MPS-A63 • MPS-A64

PNP SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for pre-amplifier input applications requiring high input impedance.

- High DC Current Gain @ I_C = 10 mAdc –
  h_{FE} = 5,000 (Min) MPS-A63
  10,000 (Min) MPS-A64
  20,000 (Min) MPS-A62
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 30 Vdc (Min) @ I_C = 100 μAdc – MPS-A63, MPS-A64
- Low Noise Figure –
  NF = 2.0 dB (Typ) @ I_C = 1.0 mAdc – MPS-A63, MPS-A64
- Monolithic Construction
- Complements to NPN MPS-A12, MPS-A13, MPS-A14

PNP SILICON DARLINGTON TRANSISTORS

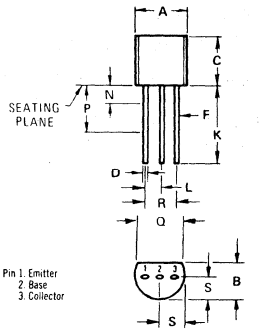


MAXIMUM RATINGS

Rating	Symbol	MPS-A62	MPS-A63 MPS-A64	Unit
Collector-Emitter Voltage	V_{CES}	20	30	Vdc
Collector-Base Voltage	V_{CB}	20	30	Vdc
Emitter-Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous	I_C	300		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.450	5.200	0.175	0.205
B	3.180	4.190	0.125	0.165
C	4.320	5.330	0.170	0.210
D	0.407	0.533	0.016	0.021
F	0.407	0.482	0.016	0.019
K	12.700	–	0.500	–
L	1.150	1.390	0.045	0.055
N	–	1.270	–	0.050
P	6.350	–	0.250	–
Q	3.430	–	0.135	–
R	2.410	2.670	0.095	0.105
S	2.030	2.670	0.080	0.105

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		BV_{CES}				Vdc
(I_C = 100 μAdc, V_{BE} = 0)	MPS-A62		20	–	–	
	MPS-A63, MPS-A64		30	–	–	
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 15 Vdc, I_E =0)	MPS-A62		–	–	100	
(V_{CB} = 30 Vdc, I_E =0)	MPS-A63, MPS-A64		–	–	100	
Emitter Cutoff Current		I_{EBO}	–	–	100	nAdc
(V_{BE} = 10 Vdc, I_C = 0)						
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63		5000	–	–	
	MPS-A64		10,000	–	–	
	MPS-A62		20,000	–	–	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63		10,000	–	–	
	MPS-A64		20,000	–	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mAdc, I_B = 0.01 mAdc)	MPS-A62		–	–	1.0	
(I_C = 100 mAdc, I_B = 0.1 mAdc)	MPS-A63, MPS-A64		–	0.8	1.5	
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPS-A62		–	–	1.4	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPS-A63, MPS-A64		–	1.25	2.0	
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (2)		f_T	125	–	–	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	MPS-A63, MPS-A64					
Output Capacitance		C_{ob}	–	4.0	–	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	MPS-A63, MPS-A64					
Small-Signal Current Gain		h_{fe}	–	35 k	–	–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)						
Noise Figure		NF	–	2.0	–	dB
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 100 kΩ, f = 1.0 kHz)						

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

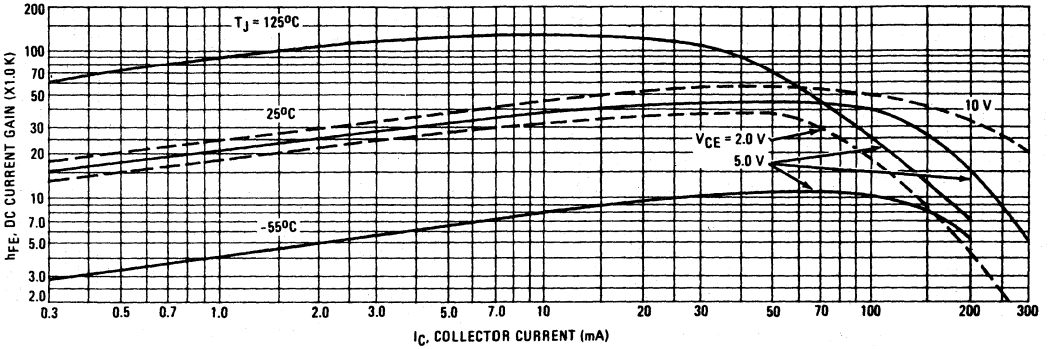


FIGURE 2 – "ON" VOLTAGE

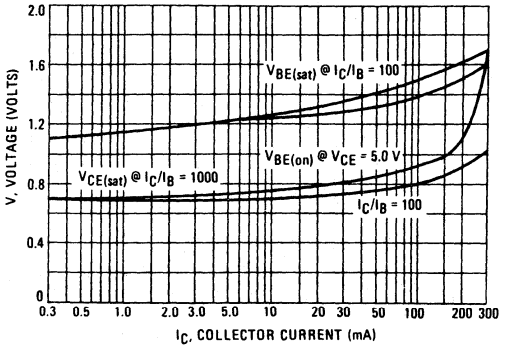


FIGURE 3 – COLLECTOR SATURATION REGION

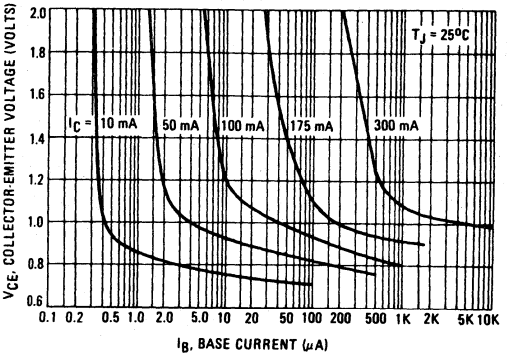


FIGURE 4 – TEMPERATURE COEFFICIENTS

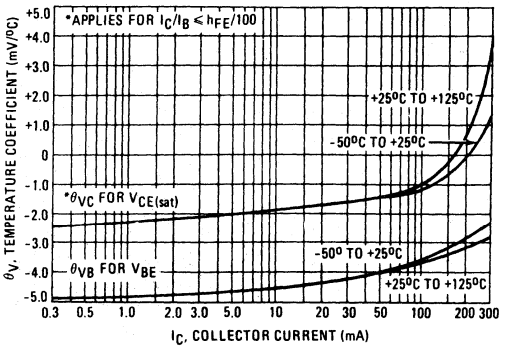
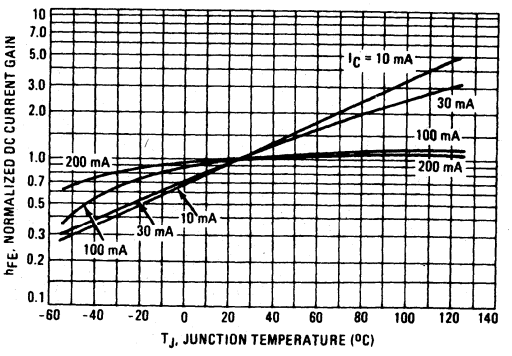


FIGURE 5 – NORMALIZED DC CURRENT GAIN



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

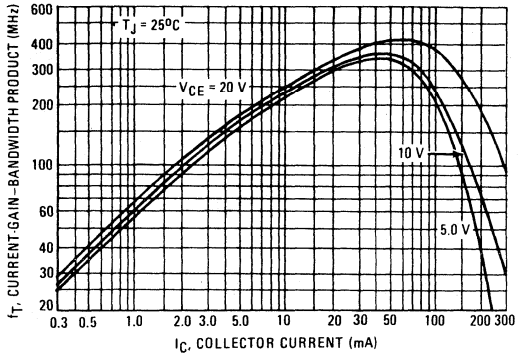


FIGURE 7 – CAPACITANCE

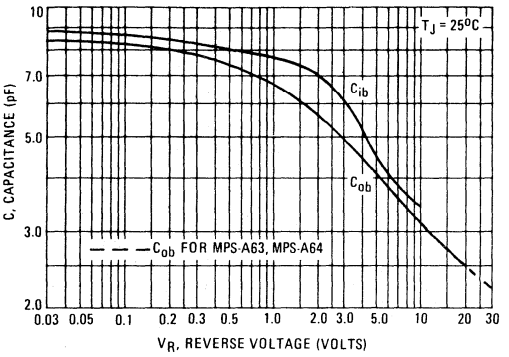


FIGURE 8 – ACTIVE-REGION SAFE OPERATING AREA

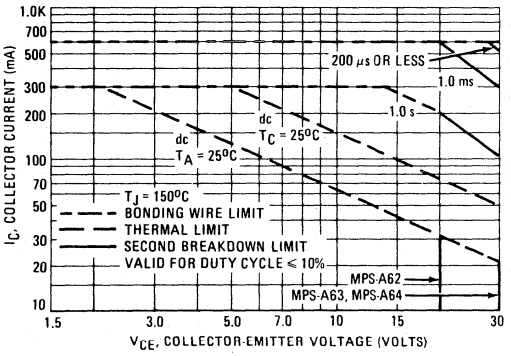


FIGURE 9 – WIDE-BAND NOISE FIGURE

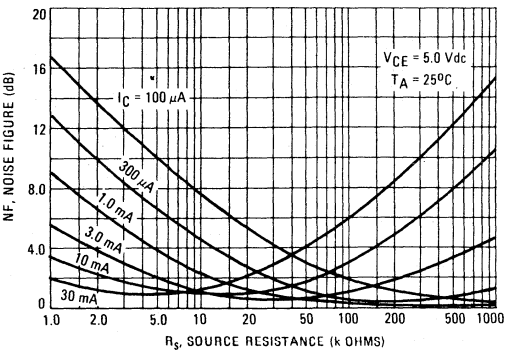


FIGURE 10 – NOISE FIGURE versus SOURCE RESISTANCE – 100 Hz

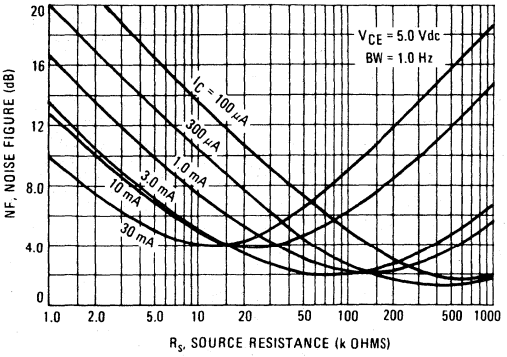
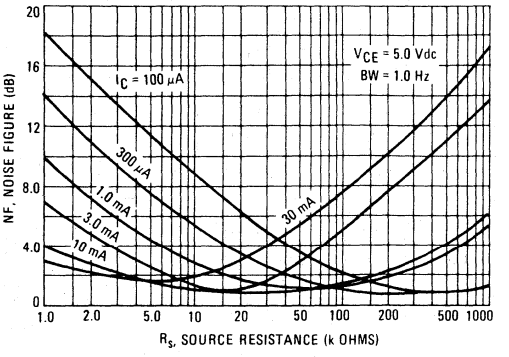


FIGURE 11 – NOISE FIGURE versus SOURCE RESISTANCE – 1000 Hz

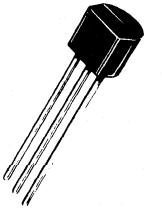


NPN SILICON ANNULAR♦ TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier applications.

- High Breakdown Voltages –
  BV_{CEO} = 120 Vdc (Min), BV_{CBO} = 140 Vdc (Min)
- Low Saturation Voltage
  $V_{CE(sat)}$ = 0.30 V (Max) @ I_C = 50 mA

HIGH VOLTAGE
NPN SILICON AMPLIFIER TRANSISTOR



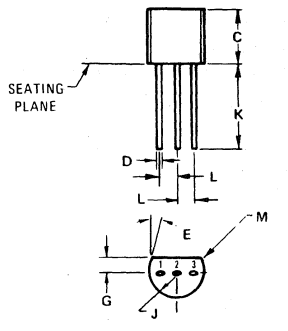
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	120	Vdc
Collector-Base Voltage	V_{CB}	140	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	150	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
C	4.450	4.700	0.175	0.185
D	0.407	0.482	0.016	0.019
E	5° NOM		5° NOM	
G	1.150	1.390	0.045	0.055
J	2.160	2.420	0.085	0.095
K	12.700	–	0.500	–
L	1.270 TP		0.050 TP	
M	0.076	0.330	0.003	0.013

CASE 29-01

♦Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	120	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	140	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 75 Vdc, I_E = 0)	I_{CBO}	–	1.0	μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	300	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.20	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)		–	0.30	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	–	1.2	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc) (1)		–	1.4	
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	60	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	8.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	30	–	–

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 1 – THERMAL RESPONSE

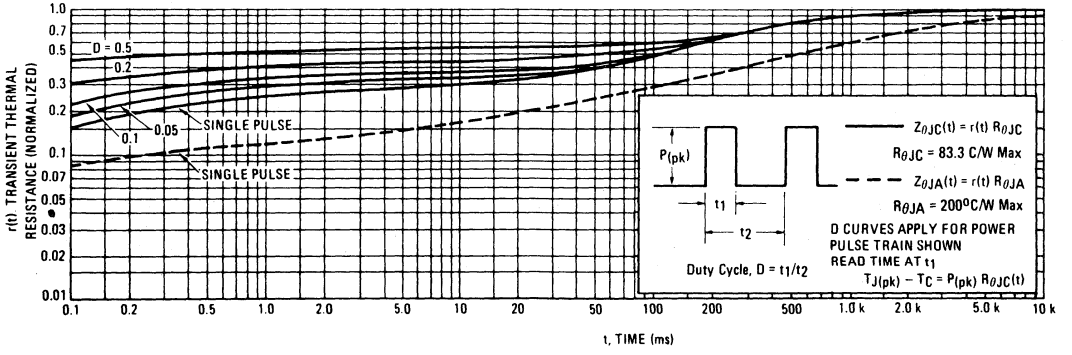


FIGURE 2 – DC CURRENT GAIN

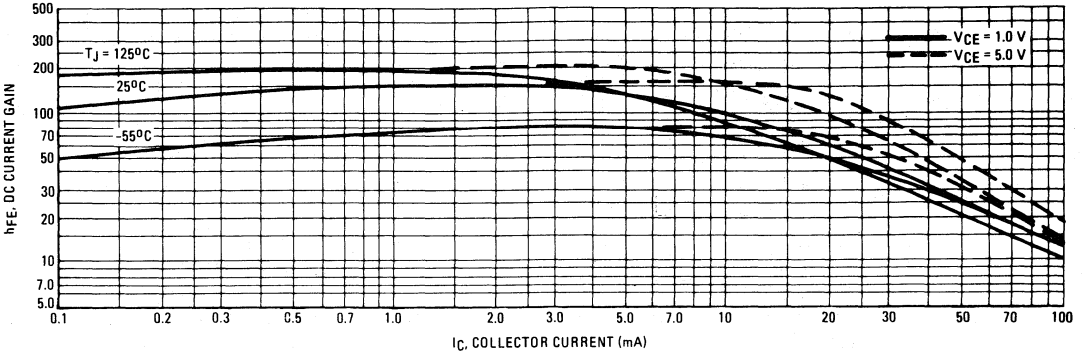


FIGURE 3 – COLLECTOR SATURATION REGION

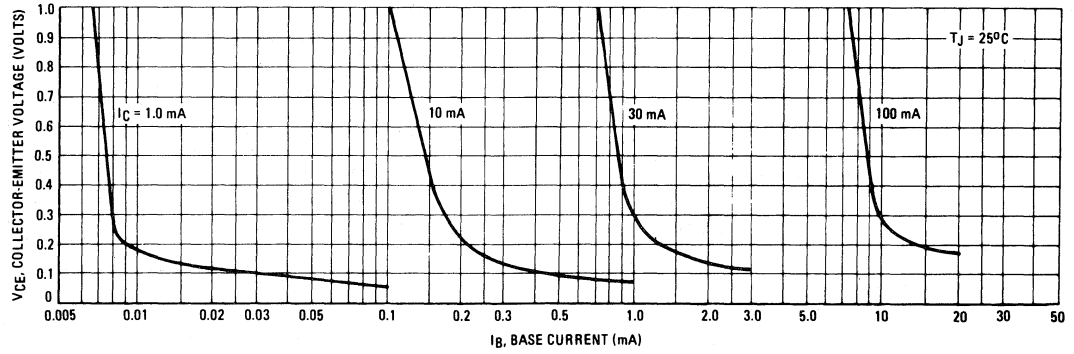
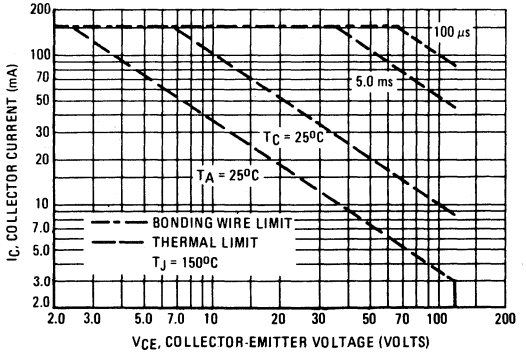


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 5 – "ON" VOLTAGES

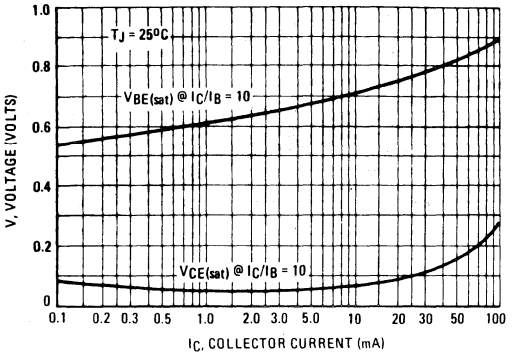


FIGURE 6 – TEMPERATURE COEFFICIENTS

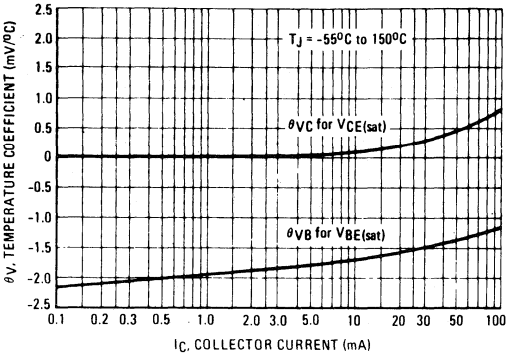


FIGURE 7 – SWITCHING TIME TEST CIRCUIT

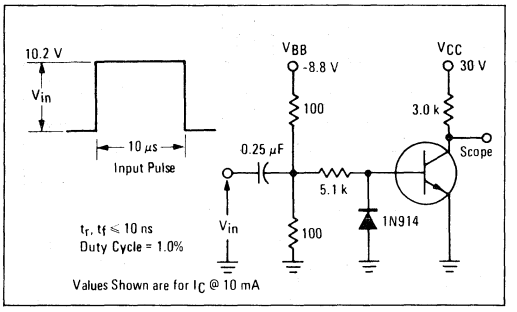


FIGURE 8 – CAPACITANCES

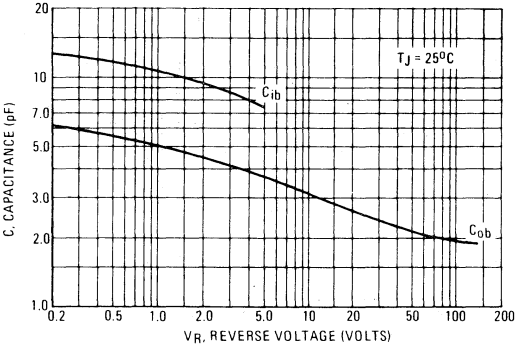


FIGURE 9 – TURN-ON TIME

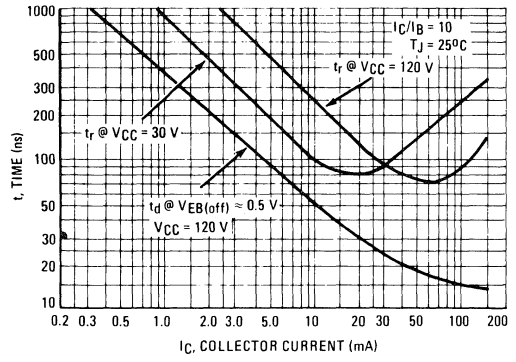
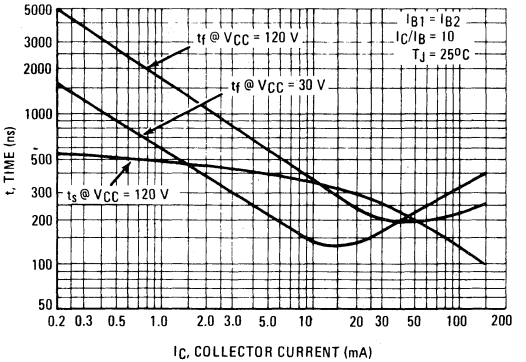


FIGURE 10 – TURN-OFF TIME



FIELD EFFECT TRANSISTORS

General Purpose Transistors		$\lvert Y_{fs} \rvert$ Min. mmho	$\lvert Y_{fs} \rvert$ Max. mmho	$V_{GS(off)}$ Min. V	$V_{GS(off)}$ Max. V	NF Max. dB	C_{RSS} Max. pF	BV_{GSS} Min. V	Technology	Package	Page
BF245	Wide Frequency Range from DC-VHF	3	6.5	0.4	7.5	1.5	1.1	30	N-ch. J	TO-92	5-1
MPF102	Amplifier and Mixers	2	7.5	–	8	–	3	25	N-ch. J	TO-92	5-17
2N4117	Low Input Current DC Amplifier	0.07	0.21	0.6	1.8	–	1.5	40	N-ch. J	TO-72	5-26
2N4118		0.08	0.25	1	3	–	1.5	40	N-ch. J	TO-72	5-26
2N4119		0.10	0.33	2	6	–	1.5	40	N-ch. J	TO-72	5-26
2N5457	Audio and Switching	1	5	0.5	6	–	3	25	N-ch. J	TO-92	5-44
2N5458		1.5	5.5	1	7	–	3	25	N-ch. J	TO-92	5-44
2N5459		2	6	2	8	–	3	25	N-ch. J	TO-92	5-44
2N5460	Amplifier Applications	1	4	0.75	6.0	2.5	2	40	P-ch. J	TO-92	5-45
2N5461		1.5	5	1.0	7.5	2.5	2	40	P-ch. J	TO-92	5-45
2N5462		2	6	1.8	9.0	2.5	2	40	P-ch. J	TO-92	5-45
2N5463		1	4	0.75	6.0	2.5	2	60	P-ch. J	TO-92	5-45
2N5464		1.5	5	1.0	7.5	2.5	2	60	P-ch. J	TO-92	5-45
2N5465		2	6	1.8	9	2.5	2	60	P-ch. J	TO-92	5-45

Switching Transistors		$r_{DS(on)}$ Max. Ω	$V_{GS(off)}$ Min. V	$V_{GS(off)}$ Max. V	$I_{D(off)}$ Max. nA	I_{DSS} Min. mA	I_{DSS} Max. mA	C_{RSS} Max. pF	BV_{GSS} Min. V	Technology	Package	Page
MPF4391	Chopper and H Speed Switching	30	4	10	1	60	130	3.5	30	N-ch. J	TO-92	5-22
MPF4392		60	2	5	1	25	75	3.5	30	N-ch. J	TO-92	5-22
MPF4993		100	0.5	3	1	5	30	3.5	30	N-ch. J	TO-92	5-22
2N4351	Enhancement Mode, Low Power	300	1	5	10	3	–	1.3	25	N-ch. MOS	TO-72	5-28
2N4352		600	1	5	10	3	–	1.3	25	P-ch. MOS	TO-72	5-32
2N5457	Audio and Switching	–	0.5	6	–	1	5	3	25	N-ch. J	TO-92	5-44
2N5458		–	1	7	–	2	9	3	25	N-ch. J	TO-92	5-44
2N5459		–	2	8	–	4	16	3	25	N-ch. J	TO-92	5-44
2N5638	Chopper and H Speed Switching	30	–	12	1	50	–	4	30	N-ch. J	TO-92	5-50
2N5639		60	–	8	1	25	–	4	30	N-ch. J	TO-92	5-50
2N5640		100	–	6	1	5	–	4	30	N-ch. J	TO-92	5-50

5

High Frequency Transistors		$\lvert Y_{fs} \rvert$ Min.	$\lvert Y_{fs} \rvert$ Max.	C_{RSS} Max.	NF Max.	@ F	Technology	Package	Page
		mmho		pF	dB	MHz			
BF245	Wide Frequency Range to VHF	3	6.5	1.1	1.5	100	N-ch. J	TO-92	5-1
BF256	VHF/UHF Applications	4.5	–	0.7 (typ)	7.5 (typ)	800	N-ch. J	TO-92	5-5
J308	VHF/UHF Amplifier and Mixer	–	20	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-9
J309		–	20	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-9
J310		–	18	2.5	1.5 (typ)	100	N-ch. J	TO-92	5-9
MFE140	Dual Gate, FM Amplifiers and Mixers	10	20	0.05	3.5	100	N-ch. MOS	TO-72	5-11
MPF102	VHF Amplifiers and Mixers	1.6	–	3	–	–	N-ch. J	TO-92	5-17
MPF/MFE130	Dual Gate, Amplifiers and Mixers	8	20	0.05	5	105	N-ch. MOS	262/TO-72	5-18
MPF/MFE131		8	20	0.05	5	60	N-ch. MOS	262/TO-72	5-18
MPF/MFE132		8	20	0.05	5	200	N-ch. MOS	262/TO-72	5-18
2N4416	VHF/UHF Amplifiers	4.5	7.5	0.8	4	400	N-ch. J	TO-72	5-38
2N5484	VHF/UHF Amplifiers	3	6	1	3	100	N-ch. J	TO-92	5-48
2N5485		3.5	7	1	2	100	N-ch. J	TO-92	5-48
2N5486		4	8	1	4	400	N-ch. J	TO-92	5-48
3N201	Dual Gate, VHF Amplifiers and Mixers	8	20	0.03	4.5	200	N-ch. MOS	TO-72	5-52
3N202		8	20	0.03	–	–	N-ch. MOS	TO-72	5-52
3N203		7	15	0.03	6	45	N-ch. MOS	TO-72	5-52
3N211	Dual Gate, VHF Amplifiers and Mixers	17	40	0.05	4	45	N-ch. MOS	TO-72	5-58
3N212		17	40	0.05	–	–	N-ch. MOS	TO-72	5-58
3N213		15	35	0.05	4	45	N-ch. MOS	TO-72	5-58

BF245 • BF245A
BF245B • BF245C

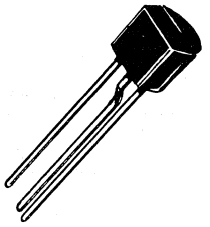
SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for a wide range of fequency Applications from DC to VHF.

- Low cost TO-92 type package
- High forward transfer admittance, $|Y_{fs}| = 3$ mmhos (min.)
- Low transfer capacitance, $C_{rss} = 3$ pF (typ.)
- Low input capacitance, $C_{iss} = 0.7$ pF (typ.)
- Three I_{dss} subgroups available:
  BF245 A: $I_{dss} = 2$ mA to 6.5 mA
  BF245 B: $I_{dss} = 6$ mA to 15 mA
  BF245 C: $I_{dss} = 12$ mA to 25 mA

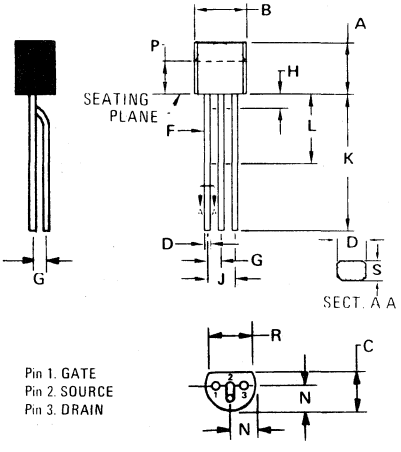
N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS

(TYPE A)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ $T_A = 25$ °C Derate above 25 °C	P_D	360 2.88	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	−65 to +150	°C



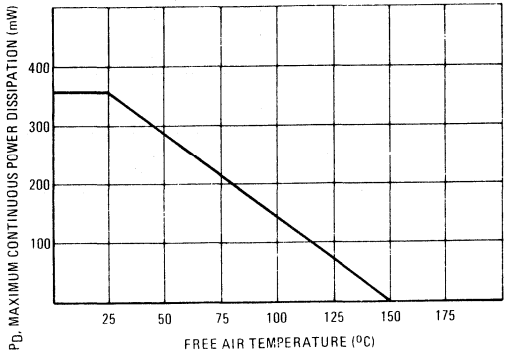
Pin 1. GATE
Pin 2. SOURCE
Pin 3. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

(TO-18 Pin configuration)

FIGURE 1 – POWER DERATING CURVE



5

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($-I_G$ = 1.0 μAdc, V_{DS} = 0)		$-V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 200 μA)	BF245[2]	$-V_{GS}$	0.4	–	7.5	Vdc
	BF245A		0.4	–	2.2	
	BF245B		1.6	–	3.8	
	BF245C		3.2	–	7.5	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nA)		$-V_{GS(Off)}$	0.5	–	8	Vdc
Gate Reverse Current ($-V_{GS}$ = 20 Vdc, V_{DS} = 0)		$-I_{GSS}$	–	–	5	nAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current[1] (V_{DS} = 15 Vdc, V_{GS} = 0)	BF245[2]	I_{DSS}	2		25	mAdc
	BF245A		2		6.5	
	BF245B		6		15	
	BF245C		12		25	
SMALL SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz))		$\|Y_{fs}\|$	3.0		6.5	mmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz)		$\|Y_{os}\|$		40		μmhos
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 200 MHz)		$\|Y_{fs}\|$		5.6		mmhos
Reverse Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 200 MHz)		$\|Y_{rs}\|$		1.0		mmhos
Input Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc)		C_{iss}		3		pf
Reverse Transfer Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{Rss}		0.7		pf
Output Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{oss}		0.9		pf
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1 KΩ, f = 100 MHz)		N_F		1.5		db
Cut-off Frequency[3] (V_{DS} = 15 Vdc, V_{GS} = 0)		f_{gfs}		700		MHz

[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
[2] On orders against the BF245, any or all subgroups might be shipped.
[3] The frequency at which gfs is 0.7 of its value at 1 KHz.

TYPICAL CHARACTERISTICS

FIGURE 2 – CORRELATION BETWEEN $-V_{GS(off)}$ AND I_{DSS}

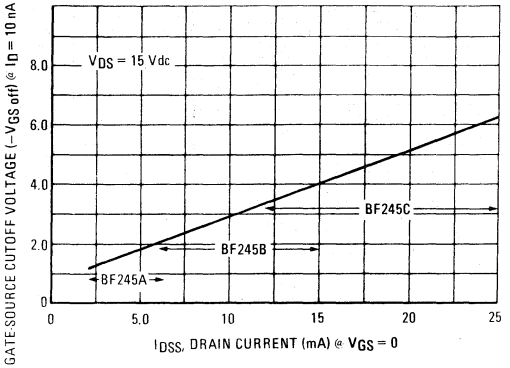


FIGURE 3 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

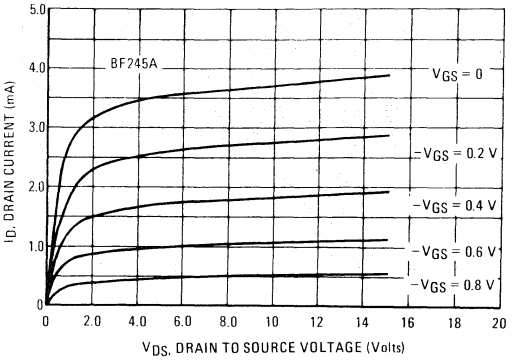
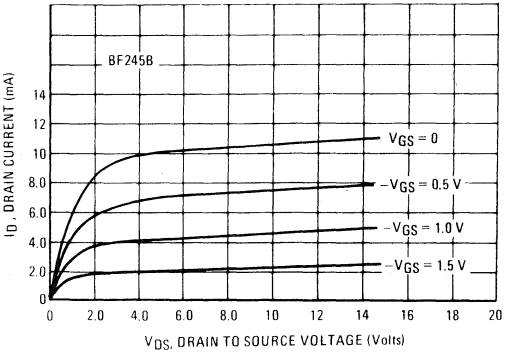


FIGURE 4 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE



FIGUR 5 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

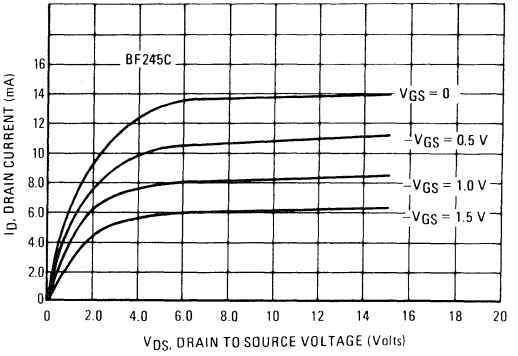


FIGURE 6 – INPUT ADMITTANCE VERSUS FREQUENCY

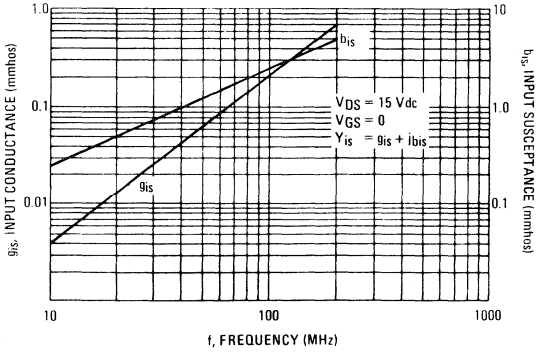
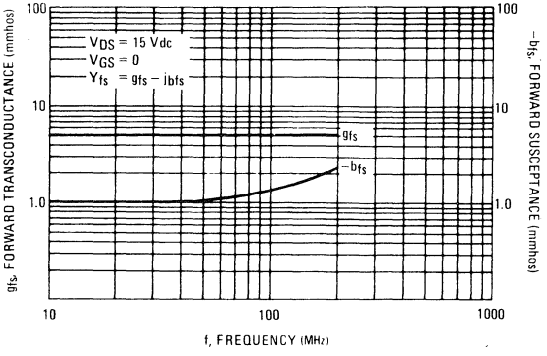


FIGURE 7 – FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



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TYPICAL CHARACTERISTICS

FIGURE 8 – REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY

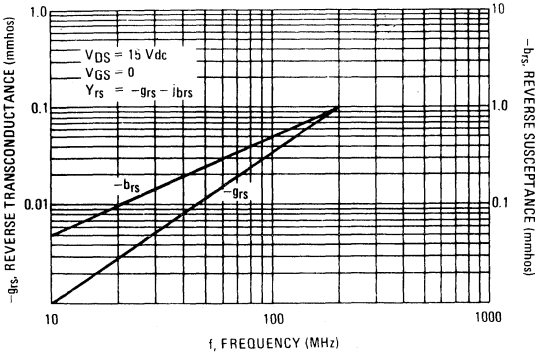


FIGURE 9 – OUTPUT ADMITTANCE VERSUS FREQUENCY

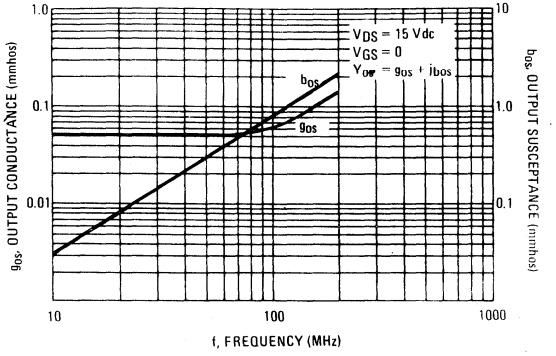


FIGURE 10 – INPUT CAPACITANCE VERSUS GATE-SOURCE VOLTAHE

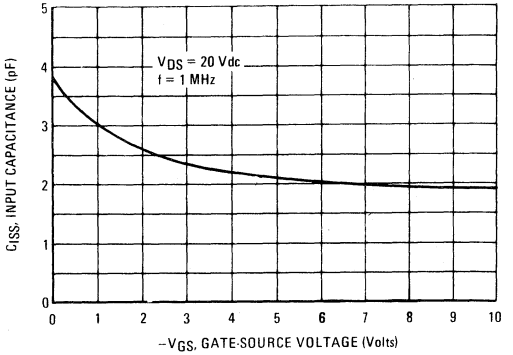
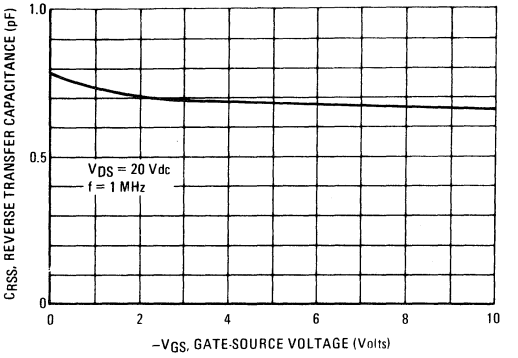


FIGURE 11 – REVERSE TRANSFER CAPACITANCE VERSUS GATE-SOURCE VOLTAGE



5

BF256 • BF256A
BF256B • BF256C

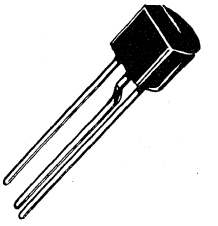
SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for VHF and UHF Applications.

- Low cost TO-92 type package
- Forward transfer admittance, Y_{fs} = 4,5 mmhos (min.)
- Transfer capacitance, C_{rss} = 0,7 (typ.)
- Power gain at f = 800 MHz, typ. = 11dB
- Three I_{dss} subgroups available:
  BF256A : I_{dss} = 3 mA to 7 mA
  BF256B : I_{dss} = 6 mA to 13 mA
  BF256C : I_{dss} = 11 mA to 18 mA

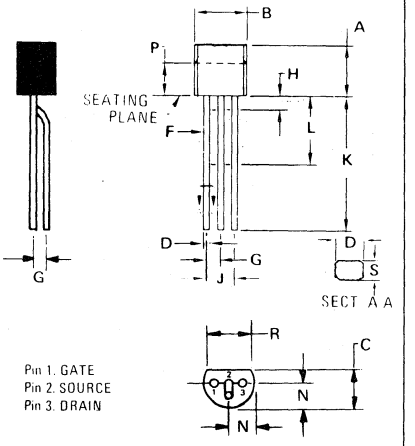
N-CHANNEL
JUNCTION FIELD-EFFECT
TRANSISTORS

(TYPE A)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	360 2.88	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	−65 to +150	°C

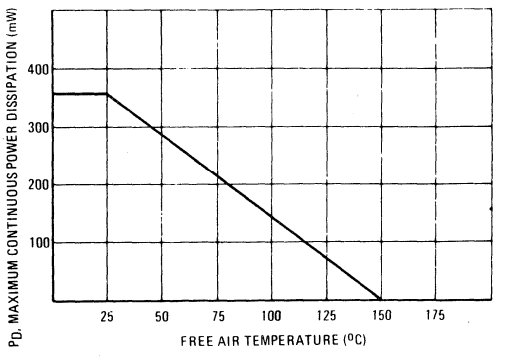


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H		2.54		0.100
J	2.41	2.67	0.095	0.105
K	12.70		0.500	
L	6.35		0.250	
N	2.03	2.92	0.080	0.115
P	2.92		0.115	
R	3.43		0.135	
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

(TO-18 Pin configuration)

FIGURE 1 – POWER DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($-I_G$ = 1.0 μAdc, V_{DS} = 0)		$-V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 200 μA)		$-V_{GS}$	0.5	–	7.5	Vdc
Gate Reverse Current ($-V_{GS}$ = 20 Vdc, V_{DS} = 0)		$-I_{GSS}$	–	–	5	nAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current[1] (V_{DS} = 15 Vdc, V_{GS} = 0)	BF256[2]	I_{DSS}	3	–	18	mAdc
	BF256A		3	–	7	
	BF256B		6	–	13	
	BF256C		11	–	18	
SMALL SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 KHz)		$\|Y_{fs}\|$	4.5	5	–	mmhos
Reverse Transfer Capacitance (V_{DS} = 20 Vdc, $-V_{GS}$ = 1 Vdc, f = 1 MHz)		C_{rss}	–	0.7	–	pf
Output Capacitance (V_{DS} = 20 Vdc, V_{GS} = 0, f = 1 MHz)		C_{oss}	–	1.0	–	pf
Noise Figure (V_{DS} = 10 Vdc, Rs = 47 Ω, f = 800 MHz)		N_F	–	7.5	–	db
Cut-off Frequency[3] (V_{DS} = 15 Vdc, V_{GS} = 0)		f_{gfs}	–	1000	–	MHz
Power Gain (V_{DS} = 15 Vdc, Rs = 47 Ω, f = 800 MHz)		Gp	–	11	–	dB

1 Pulse Test: Pluse Width = 300 μs, Duty Cycle = 2.0%

2 On orders against the BF256, any or all subgroups might be shipped

3 The frequency at which gfs is 0.7 of its value at 1 KHz

TYPICAL CHARACTERISTICS

FIGURE 2 – CORRELATION BETWEEN $-V_{GS(off)}$ AND I_{DSS}

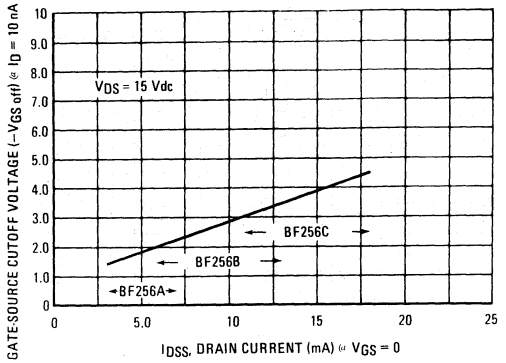


FIGURE 3 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

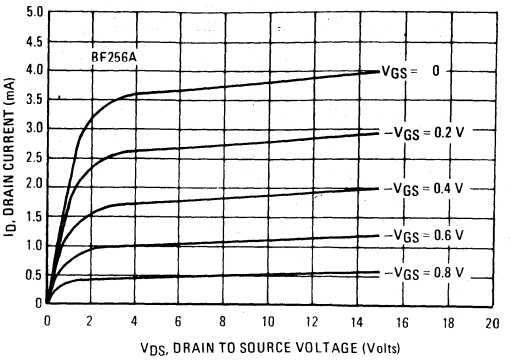


FIGURE 4 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

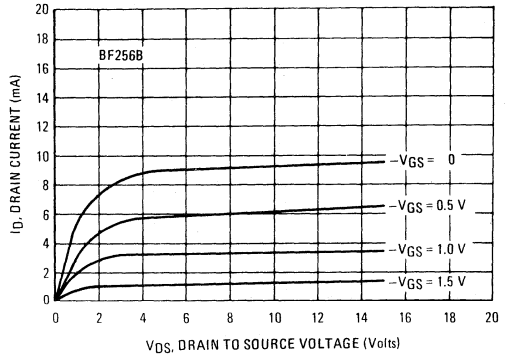


FIGURE 5 – DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE

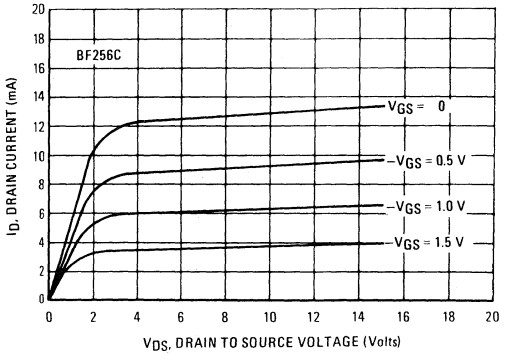


FIGURE 6 – INPUT ADMITTANCE VERSUS FREQUENCY

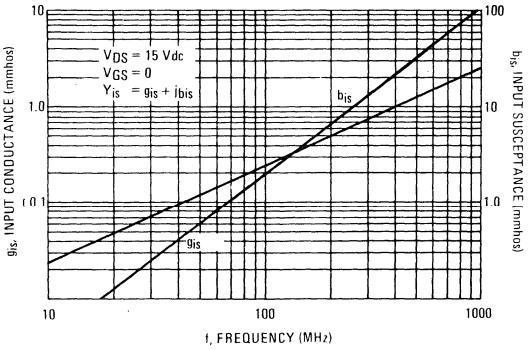
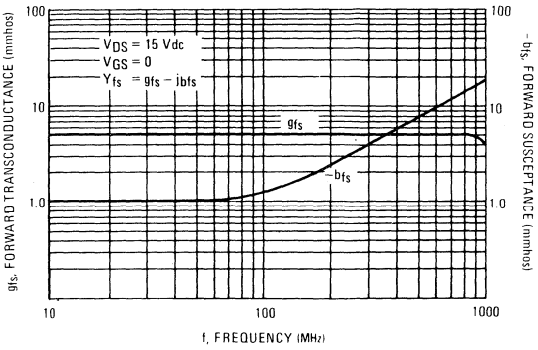


FIGURE 7 – FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



TYPICAL CHARACTERISTICS

FIGURE 8 – REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY

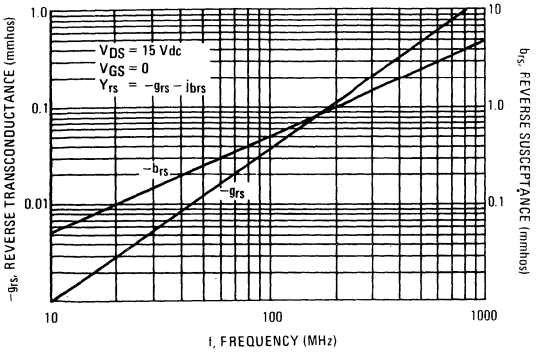


FIGURE 9 – OUTPUT ADMITTANCE VERSUS FREQUENCY

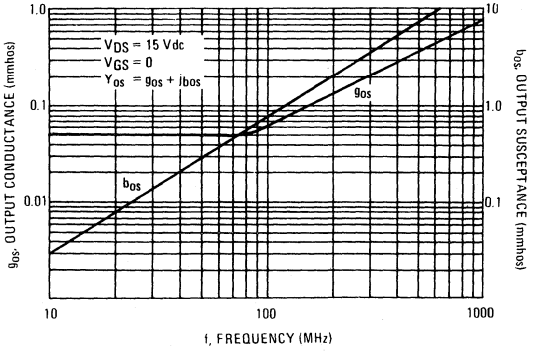


FIGURE 10 – INPUT CAPACITANCE VERSUS GATE-SOURCE VOLTAGE

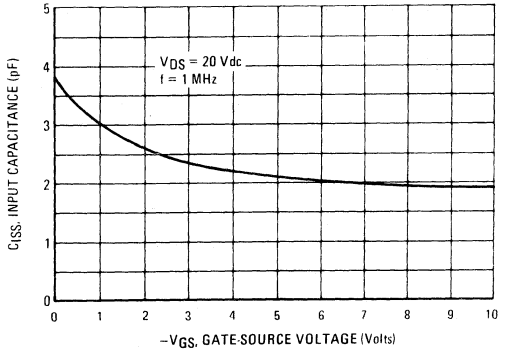
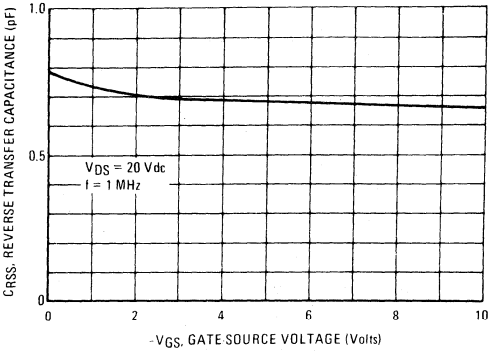


FIGURE 11 – REVERSE TRANSFER CAPACITANCE VERSUS GATE-SOURCE VOLTAGE



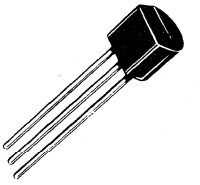
J308
J309 • J310

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . designed for VHF/UHF amplifier, mixer and oscillator applications.

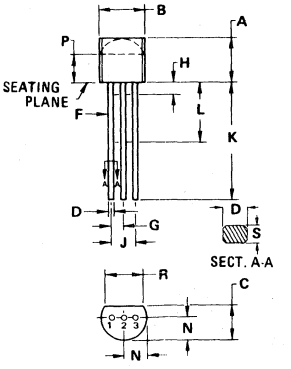
- High Power Gain –
  G_{pg} = 16 dB (Typ) @ f = 100 MHz
- Low Noise Figure –
  NF = 1.5 dB (Typ) @ 100 MHz
- High Forward Transfer Admittance
  $|g_{fs}|$ 8–20 mmhos – J308
  10–20 mmhos – J309
  8–18 mmhos – J310

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 3.5	mW mW/°C
Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

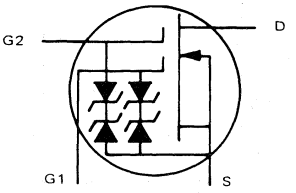
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -1.0 μA, V_{DS} = 0)		BV_{GSS}	-25	–	–	Vdc
Gate Reverse Current		I_{GSS}				
(V_{GS} = -15 V, V_{DS} = 0, T_A = 25°C)			–	–	-1.0	nA
(V_{GS} = -15 V, V_{DS} = 0, T_A = +125°C)			–	–	-1.0	μA
Gate-Source Cutoff Voltage		$V_{GS(off)}$				Vdc
(V_{DS} = 10 V, I_D = 1.0 nA)	J308		-1.0	–	-6.5	
	J309		-1.0	–	-4.0	
	J310		-2.0	–	-6.5	
ON CHARACTERISTICS						
Saturation Drain Current (1)		I_{DSS}				mA
(V_{DS} = 10 V, V_{GS} = 0)	J308		12	–	60	
	J309		12	–	30	
	J310		24	–	60	
Gate-Source Forward Voltage (V_{DS} = 0, I_G = 1.0 mA)		$V_{GS(f)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS						
Common-Source Forward Transconductance		g_{fs}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)						
	J308		8,000	–	20,000	
	J309		10,000	–	20,000	
	J310		8,000	–	18,000	
Common-Source Output Conductance		g_{os}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)						
	J308		–	–	200	
	J309		–	–	150	
	J310		–	–	200	
Common-Gate Forward Transconductance		g_{fg}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)						
	J308		–	13,000	–	
	J309		–	13,000	–	
	J310		–	12,000	–	
Common-Gate Output Conductance		g_{og}				μmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 1.0 kHz)						
	J308		–	150	–	
	J309		–	100	–	
	J310		–	150	–	
Gate-Drain Capacitance (V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz)		C_{gd}	–	1.8	2.5	pF
Gate-Source Capacitance (V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz)		C_{gs}	–	4.3	5.0	pF
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz)		$\bar{e}_n$	–	10	–	$nV/\sqrt{Hz}$
FUNCTIONAL CHARACTERISTICS						
Common-Source Forward Transconductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)		$Re_{(yfs)}$	–	12	–	mmhos
Common-Gate Input Conductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)		$Re_{(yig)}$	–	12	–	mmhos
Common-Source Input Conductance		$Re_{(yis)}$				mmhos
(V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)						
	J308		–	0.7	–	
	J309		–	0.7	–	
	J310		–	0.5	–	
Common-Source Output Conductance (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)		$Re_{(yos)}$	–	0.25	–	mmhos
Common-Gate Power Gain (V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz)		G_{pg}	–	16	–	dB
Noise Figure (V_{DS} = 10 V, I_D = 10 mA)		NF	–	1.5	–	dB

Note:
(1) Pulse test PW 300 μs, duty cycle ≤ 3%.

MFE140

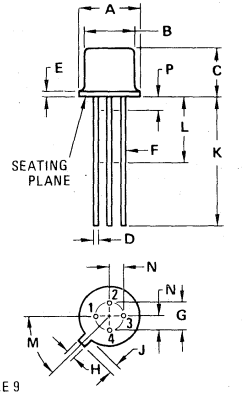


N-CHANNEL
DUAL GATE
MOS FIELD – EFFECT
TRANSISTOR

N-CHANNEL DUAL-GATE
SILICON-NITRIDE PASSIVATED
MOS FIELD-EFFECT TRANSISTOR

. . . depletion mode dual gate MOS FET transistor designed for FM amplifier and mixer applications.

- Silicon Nitride Passivation for Excellent Long Term Stability
- Diode Protected Gates
- Supplied in Metal Can – TO-72



STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain Current	I_D	30	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	300	mW
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +200	^oC
Gate Current	I_{GS}	10	mAdc
Gate-Source Voltage	V_{GS}	±7.0	Vdc

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted). Substrate Connected to Source

Characteristisc	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = -4.0 Vdc, V_{G2} = +4.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (I_{G1} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G1SO}$	±7.0	–	±20	Vdc
Gate 2 – Source Breakdown Voltage (I_{G2} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G2S0}$	±7.0	–	±20	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 1 Reverse Leakage Current (V_{G1S} = ±6.0 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	–	–	20	nAdc
Gate 2 Reverse Leakage Current (V_{G2S} = ±6.0 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	–	–	20	nAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{G2S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	3.0	10	30	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (Gate 1 connected to Drain) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\lvert y_{fs1} \rvert$	10	–	20	mmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f - 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	2.5	4.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{rss}	–	0.023	0.05	pF
Common-Source Noise Figure (Figure 8) (See Test Circuit in Figure 11)	NF	–	2.5	3.5	dB
Common-Source Power Gain (Figure 7) (See Test Circuit in Figure 11)	G_{ps}	20	23	–	dB
Level of Unwanted Signal for 1.0% Cross Modulation (Figure 10) (See Test Circuit in Figure 11)	–	–	45	–	mV
Common-Source Conversion Power Gain (Gate 1 or Gate 2 Injection, Figure 12) (See Test Circuit in Figure 13) (Signal Frequency = 100 MHz, Local Oscillator Frequency = 110.7 MHz)	G_c	15	18.5	–	dB
1/2 I. F. Rejection (See Test Circuit in Figure 13)	1/2 I_{FREJ}	–	50	–	dB

COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)

FIGURE 1 – INPUT ADMITTANCE

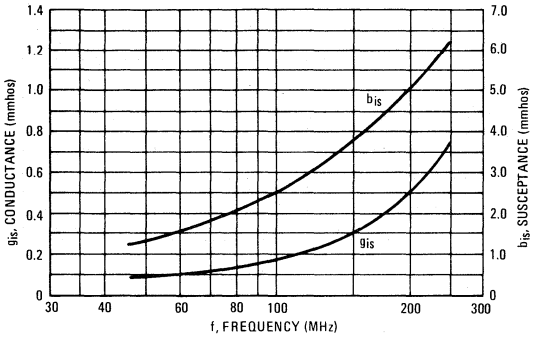


FIGURE 2 – REVERSE TRANSFER ADMITTANCE

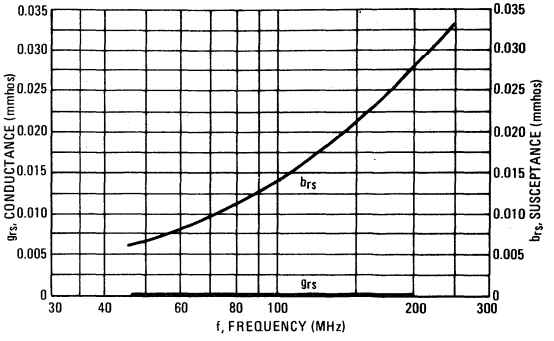


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

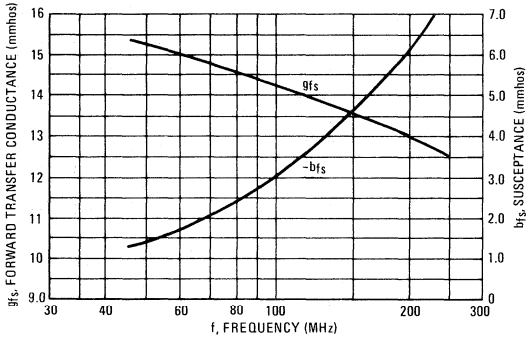
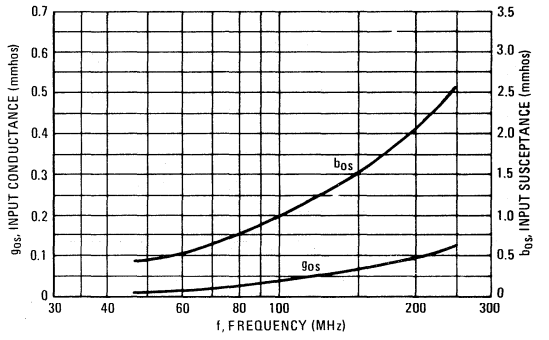


FIGURE 4 – OUTPUT ADMITTANCE



FORWARD TRANSFER ADMITTANCE

(V_{DS} = 15 Vdc, f = 1.0 kHz)

FIGURE 5 – GATE 1

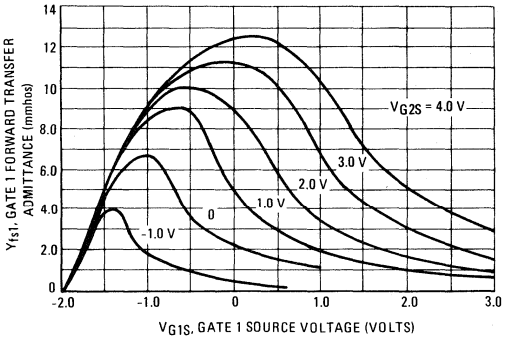


FIGURE 6 – GATE 2

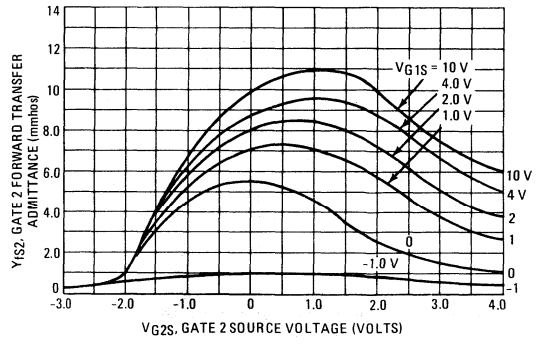


FIGURE 7 – POWER GAIN

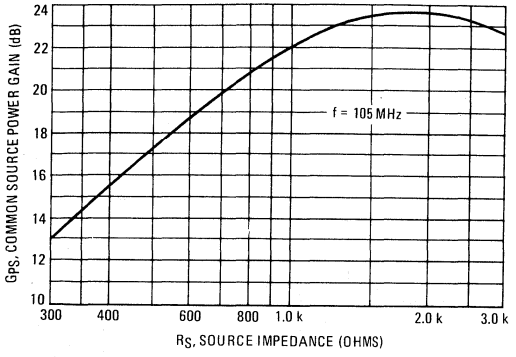


FIGURE 8 – NOISE FIGURE

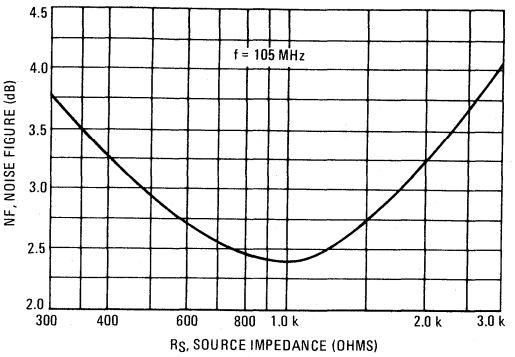


FIGURE 9 – GAIN REDUCTION

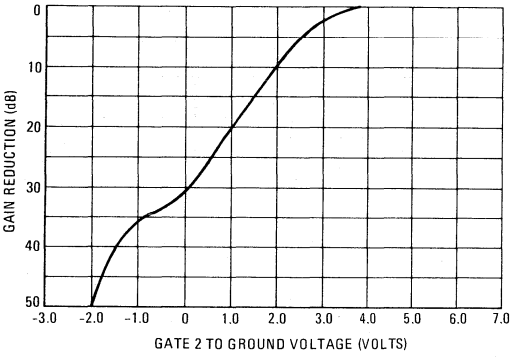


FIGURE 10 – CROSS MODULATION

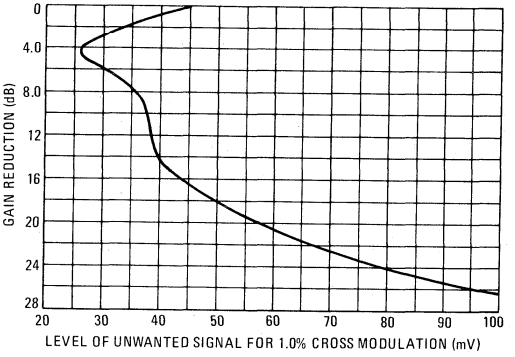
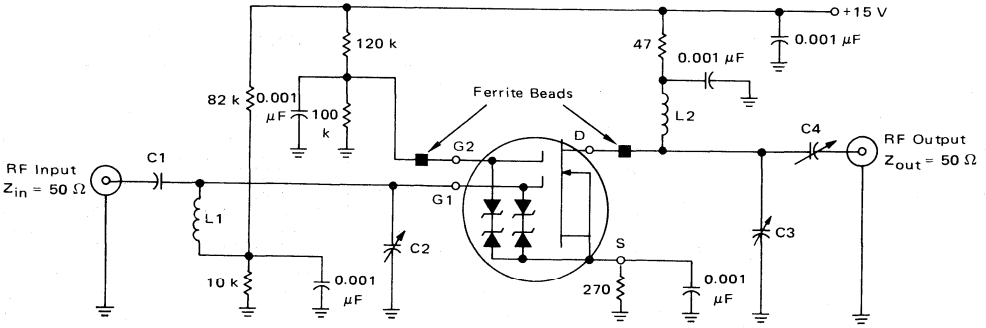


FIGURE 11 – 105 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



The following component values are for a stern stability factor = 2.0.

L1,L2 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)

C1 Nominal 7.0 pF Adjusted for source impedance of approximately 1000 Ω, JOHANSON JMC2951

C2 Nominal 4.0 pF ARCO 402

C3 Nominal 13.73 pF ARCO 403

C4 Nominal 4.36 pF JOHANSON JMC2951

All Decoupling Capacitors are Ceramic Discs.

FIGURE 12 – CONVERSION GAIN

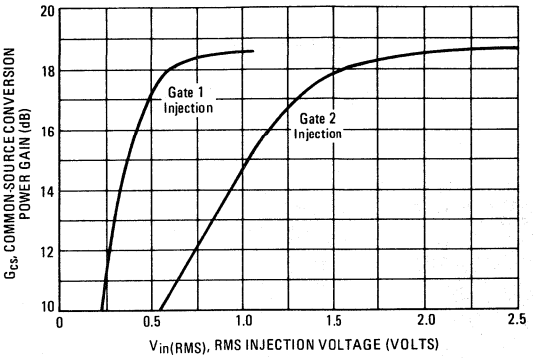
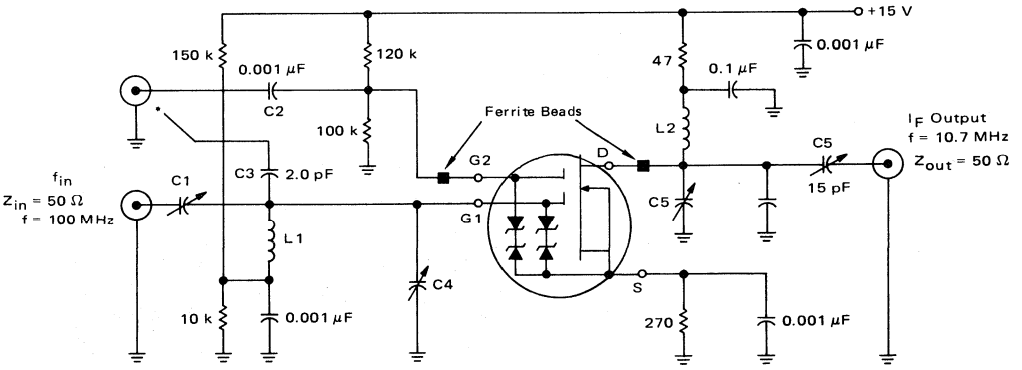


FIGURE 13 – CONVERSION GAIN TEST CIRCUIT

Local Oscillator Injection
$V_{in(RMS)} \approx 2.0$ V for G2
≈ 0.9 V for G1
f = 110.7 MHz



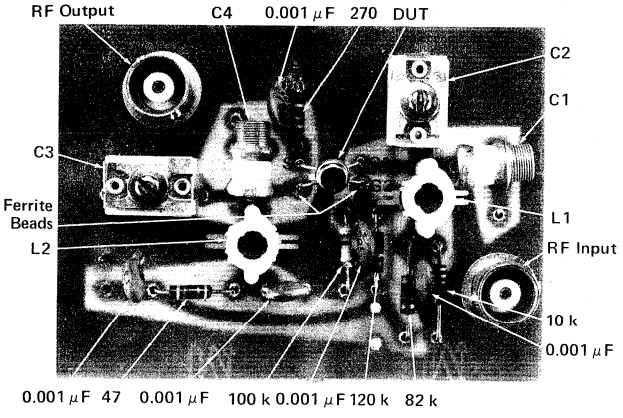
L1 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)
L2 2.73 µH High Unloaded Q
C1 JOHANSON JMC2951
C4,C5,C6 ARCO 402

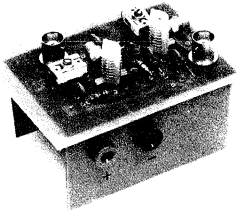
*For G1 injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input.

PRINTED CIRCUIT BOARD LAYOUT INFORMATION

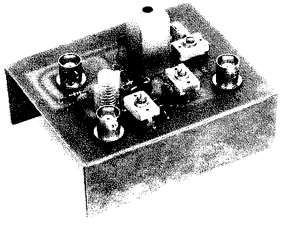
FIGURE 14 – TEST FIXTURES

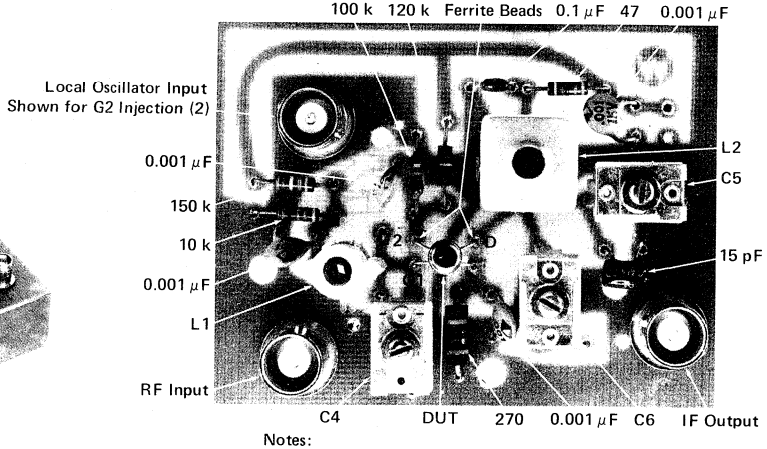
105 MHz POWER GAIN AND NOISE
FIGURE TEST CIRCUIT





100 MHz to 10.7 MHz CONVERSION
GAIN TEST CIRCUIT

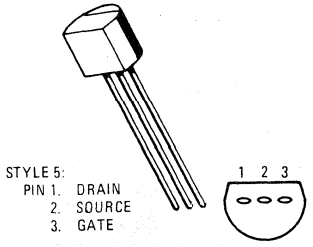




Notes:
1. C1 is on the bottom side of the board.
2. For G1 Injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input. See Figure 13.

MPF102

Silicon N-channel junction field-effect transistor designed for VHF amplifier and mixer applications.



STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 29
(TO-92)

Drain and Source may be interchanged

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (1)	125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	BV_{GSS}	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0) (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100 C)	I_{GSS}	— —	2.0 2.0	nAdc μAdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 2.0 nAdc)	$V_{GS(off)}$	—	8.0	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	V_{GS}	0.5	7.5	Vdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	2.0	20	mAdc
DYNAMIC CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	$\lvert y_{fs} \rvert$	2000	7500	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.0	pF
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$\lvert y_{fs} \rvert$	1600	—	μmhos
Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{is})$	—	800	μmhos
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{os})$	—	200	μmhos

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

MPF130 • MPF131 • MPF132
MFE130 • MFE131 • MFE132

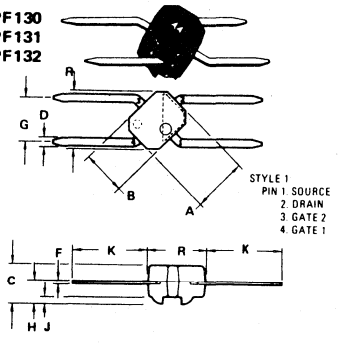
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type B) dual gate transistors designed for VHF amplifier and mixer applications. These types are specified as follows:

- MPF130/MFE130 – RF Amplifier @ 105 MHz
  MPF131/MFE131 – RF Amplifier @ 60 and 200 MHz
  MPF132/MFE132 – Mixer @ 60 and 200 MHz
- Silicon Nitride Passivation for Excellent Long Term Stability
- Diode Protected Gates
- Supplied in Metal Can or Plastic Packages –
  MFE130 Series – TO-72
  MPF130 Series – Case 262

N-CHANNEL
DUAL GATE
MOS FIELD – EFFECT TRANSISTORS

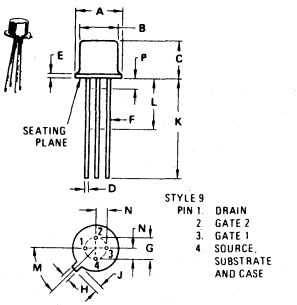
MPF130
MPF131
MPF132



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.95	5.21	0.195	0.205
B	3.94	4.19	0.155	0.165
C	2.67	2.92	0.105	0.115
D	0.64	0.89	0.025	0.035
F	0.20	0.30	0.008	0.012
G	4.06 BSC		0.160 BSC	
H	1.57	1.83	0.062	0.072
J	0.51	0.76	0.020	0.030
K	6.35	7.62	0.250	0.300
R	5.21	5.46	0.205	0.215

CASE 262-02

MFE130
MFE131
MFE132



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

CASE 20-03
TO-72

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Drain-Source Voltage	V_{DS}	25		Vdc
Drain Current	I_D	30		mAdc
		MPF130 Series	MFE130 Series	
Total Power Dissipation @ $T_A = 25^oC$ (Package Limitation)	P_D	350	300	mW
Derate above 25^oC		2.33	1.71	$mW/^oC$
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +175	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) Substrate Connected to Source

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = V_{G2} = -4.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (I_{G1} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G1SO}$	±7.0	–	±20	Vdc
Gate 2 – Source Breakdown Voltage (I_{G2} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G2SO}$	±7.0	–	±20	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)	$V_{G1S(off)}$	–	–	-4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)	$V_{G2S(off)}$	–	–	-4.0	Vdc
Gate 1 Reverse Leakage Current (V_{G1S} = ±6.0 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	–	–	20	nAdc
Gate 2 Reverse Leakage Current (V_{G2S} = ±6.0 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	–	–	20	nAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	3.0	10	30	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (Gate 1 connected to Drain) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\|y_{fs}\|$	8000	–	20,000	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	–	4.5	7.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	2.5	4.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, f = 1.0 MHz)	C_{rss}	–	0.023	0.05	pF
Common-Source Noise Figure (Figure 7) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, Z_S is optimized for NF)	NF				dB
(f = 105 MHz) MPF/MFE130		–	2.9	5.0	
(f = 60 MHz) MPF/MFE131		–	2.5	5.0	
(f = 200 MHz) MPF/MFE131		–	3.0	5.0	
Common-Source Power Gain (Figure 7) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc, Z_S is optimized for NF)	G_{ps}				dB
(f = 105 MHz) MPF/MFE130		17	23	–	
(f = 60 MHz) MPF/MFE131		20	27	–	
(f = 200 MHz) MPF/MFE131		17	20	–	
Level of Unwanted Signal for 1.0% Cross Modulation (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)	–	–	100	–	mV
Common-Source Conversion Power Gain (Gate 1 Injection, Figure 8). (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, Local Oscillator Voltage = 925 mVrms)	G_c				dB
(Signal Frequency = 60 MHz, Local Oscillator Frequency = 104 MHz) MPF/MFE132		15	16.5	–	
(Signal Frequency = 200 MHz, Local Oscillator Frequency = 244 MHz) MPF/MFE132		12	14	–	

COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)

FIGURE 1 – INPUT ADMITTANCE

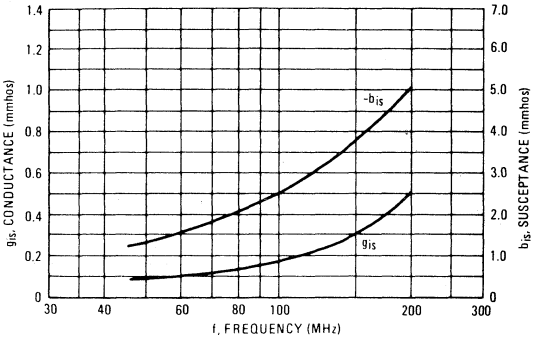


FIGURE 2 – REVERSE TRANSFER ADMITTANCE

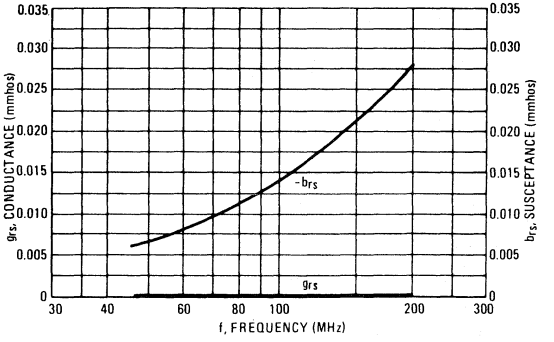


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

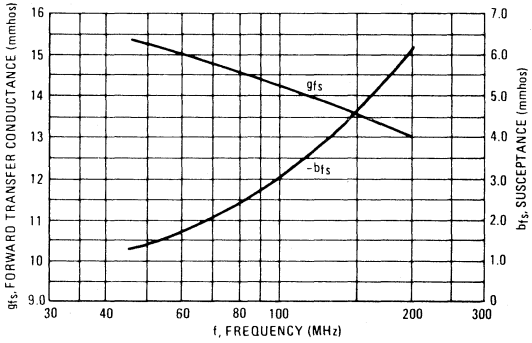


FIGURE 4 – OUTPUT ADMITTANCE

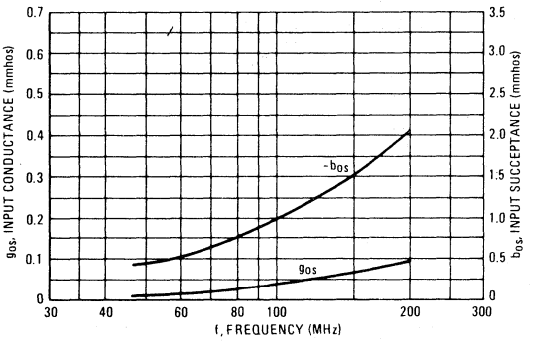


FIGURE 5 – GAIN REDUCTION

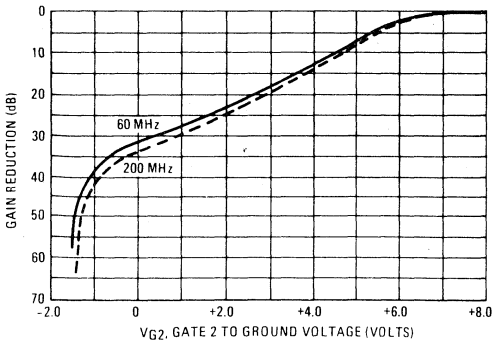


FIGURE 6 – CONVERSION POWER GAIN

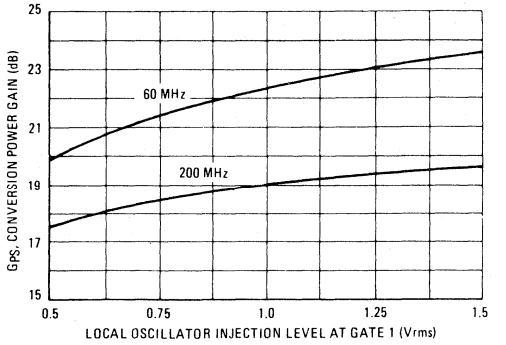
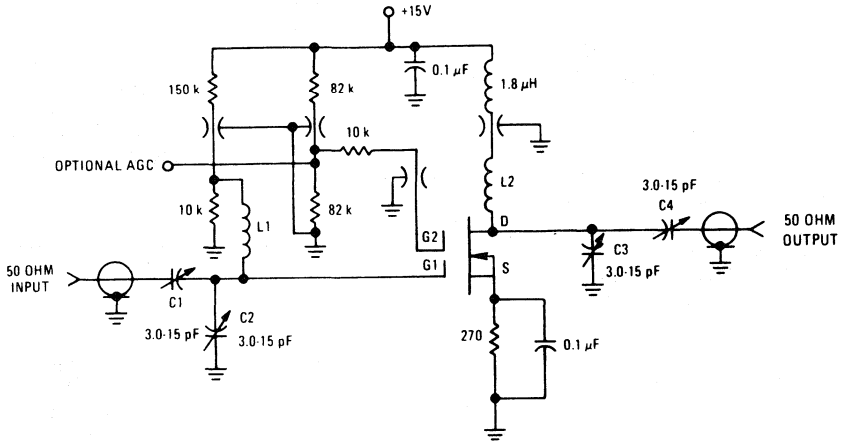


FIGURE 7 – 60, 105 AND 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT

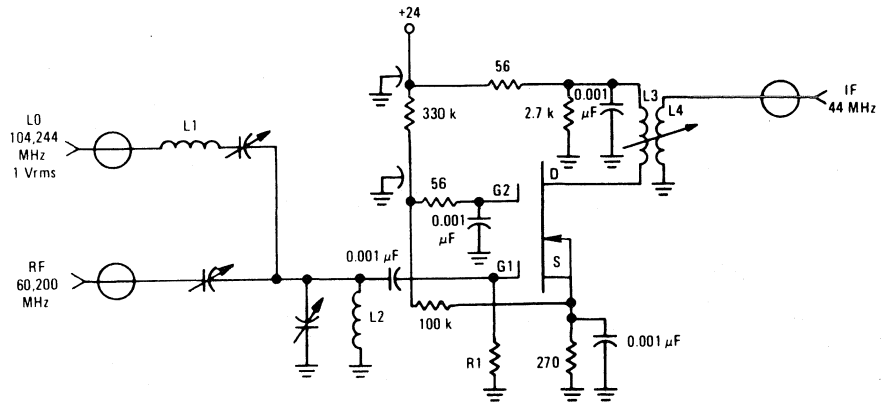


	L1	L2
60 MHz	0.33 μH	0.47 μH
105 MHz	#16 AWG, 6 1/2 Turns, 1" Long, 1/4" Dia.	#16 AWG, 5 1/4 Turns, 1" Long, 7/16" Dia.
200 MHz	#16 AWG, 3 1/2 Turns, 0.7" Long, 0.2" Dia.	#16 AWG, 4 1/2 Turns, 0.65" Long, 0.2" Dia.

All Feedthrough Capacitors 1000 pF

All Variable Capacitors JOHANSON JMC2951, 3.0-15 pF

FIGURE 8 – 60 AND 200 MHz CONVERSION GAIN TEST CIRCUIT



	R1	L1	L2	L3	L4
60 MHz	10 k	10 Turns #22 Enameled on MILLER 4500-4 Core	0.33 μH DELEVAN	15 Turns #26 Enameled on MILLER 4500-1 Core	4 Turns #26 Enameled on Same Core as L3
200 MHz	1.0 k	3 1/2 Turns #18, 1/4" Dia., 1/2" Long	2 1/2 Turns #18, 3/8" Dia., 1/2" Long	15 Turns #26 Enameled on MILLER 4500-1 Core	4 Turns #26 Enameled on Same Core as L3

All Feedthrough Capacitors 1000 pF.

All Variable Capacitors JOHANSON JMC2951, 3.0-15 pF.

MPF4391
MPF4392 • MPF4393

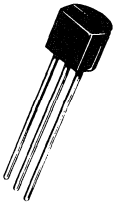
SILICON N-CHANNEL
JUNCTION FIELD–EFFECT TRANSISTORS

Depletion Mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 30 Ohms (Max) – MPF4391
  = 60 Ohms (Max) – MPF4392
  = 100 Ohms (Max) – MPF4393
- Low Reverse Transfer Capacitance –
  C_{rss} = 3.5 pF (Max)
- Guaranteed Fast Switching Times –
  t_{on} = 15 ns (Max) – All Types
  t_{off} = 20 ns (Max) – MPF4391
  = 35 ns (Max) – MPF4392
  = 55 ns (Max) – MPF4393

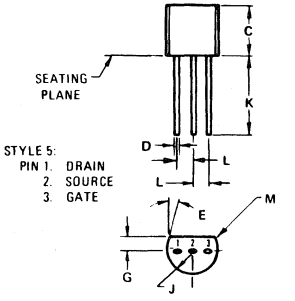
N-CHANNEL

JUNCTION FIELD-EFFECT TRANSISTORS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +150	°C



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
C	0.175	0.185	4.450	4.700
D	0.016	0.019	0.407	0.482
E	5° NOM		5° NOM	
G	0.045	0.055	1.150	1.390
J	0.085	0.095	2.160	2.420
K	0.500	–	12.700	–
L	0.050 TP		1.270 TP	
M	0.003	0.013	0.076	0.330

CASE 29(5)
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	–	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	MPF4391	V_{GS}	4.0	–	10	Vdc
	MPF4392		2.0	–	5.0	
	MPF4393		0.5	–	3.0	
Gate Reverse Current		I_{GSS}				
(V_{GS} = 15 Vdc, V_{DS} = 0)			–	–	1.0	nAdc
(V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100°C)			–	–	0.2	μAdc
Drain-Cutoff Current		$I_{D(off)}$				
(V_{DS} = 15 Vdc, V_{GS} = 12 Vdc)			–	–	1.0	nAdc
(V_{DS} = 15 Vdc, V_{GS} = 12 Vdc, T_A = 100°C)			–	–	0.1	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	MPF4391	I_{DSS}	60	–	130	mAdc
	MPF4392		25	–	75	
	MPF4393		5.0	–	30	
Drain-Source "ON" Voltage		$V_{DS(on)}$				Vdc
(I_D = 12 mAdc, V_{GS} = 0)	MPF4391		–	–	0.4	
(I_D = 6.0 mAdc, V_{GS} = 0)	MPF4392		–	–	0.4	
(I_D = 3.0 mAdc, V_{GS} = 0)	MPF4393		–	–	0.4	
Static Drain-Source "ON" Resistance (I_D = 1.0 mAdc, V_{GS} = 0)	MPF4391	$r_{DS(on)}$	–	–	30	Ohms
	MPF4392		–	–	60	
	MPF4393		–	–	100	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance		$\lvert Y_{fs} \rvert$				mmhos
(V_{DS} = 15 Vdc, I_D = 60 mAdc, f = 1.0 kHz)	MPF4391		–	20	–	
(V_{DS} = 15 Vdc, I_D = 25 mAdc, f = 1.0 kHz)	MPF4392		–	17	–	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 kHz)	MPF4393		–	12	–	
Drain-Source "ON" Resistance		$r_{ds(on)}$				Ohms
(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	MPF4391		–	–	30	
	MPF4392		–	–	60	
	MPF4393		–	–	100	
Input Capacitance (V_{GS} = 15 Vdc, V_{DS} = 0, f = 1.0 MHz)		C_{iss}	–	6.0	10	pF
Reverse Transfer Capacitance		C_{rss}				pF
(V_{GS} = 12 Vdc, V_{DS} = 0, f = 1.0 MHz)			–	2.5	3.5	
(V_{DS} = 15 Vdc, I_D = 10 mAdc, f = 1.0 MHz)			–	3.2	–	
SWITCHING CHARACTERISTICS (See Figure 5, R_K = 0)						
Turn-On Time (See Figures 1 and 2)		t_{on}				ns
($I_{D(on)}$ = 12 mAdc)	MPF4391		–	3.0	15	
($I_{D(on)}$ = 6.0 mAdc)	MPF4392		–	4.0	15	
($I_{D(on)}$ = 3.0 mAdc)	MPF4393		–	6.5	15	
Rise Time (See Figure 2)		t_r				ns
($I_{D(on)}$ = 12 mAdc)	MPF4391		–	1.2	5.0	
($I_{D(on)}$ = 6.0 mAdc)	MPF4392		–	2.0	5.0	
($I_{D(on)}$ = 3.0 mAdc)	MPF4393		–	2.5	5.0	
Turn-Off Time (See Figures 3 and 4)		t_{off}				ns
($V_{GS(off)}$ = 12 Vdc)	MPF4391		–	10	20	
($V_{GS(off)}$ = 7.0 Vdc)	MPF4392		–	20	35	
($V_{GS(off)}$ = 5.0 Vdc)	MPF4393		–	37	55	
Fall Time (See Figure 4)		t_f				ns
($V_{GS(off)}$ = 12 Vdc)	MPF4391		–	7.0	15	
($V_{GS(off)}$ = 7.0 Vdc)	MPF4392		–	15	20	
($V_{GS(off)}$ = 5.0 Vdc)	MPF4393		–	29	35	

(1) Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 1.0%.

TYPICAL SWITCHING CHARACTERISTICS

FIGURE 1 – TURN-ON DELAY TIME

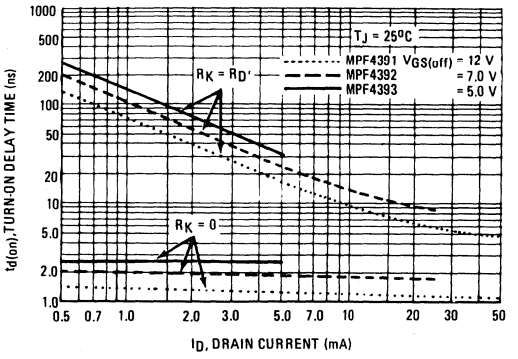


FIGURE 2 – RISE TIME

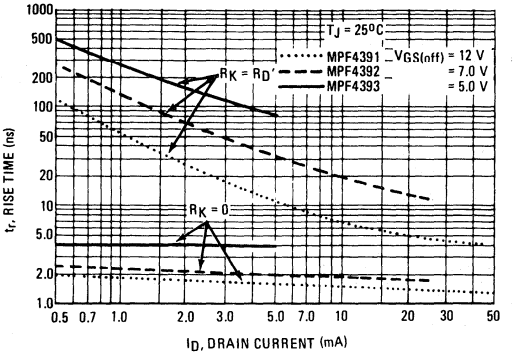


FIGURE 3 – TURN-OFF DELAY TIME

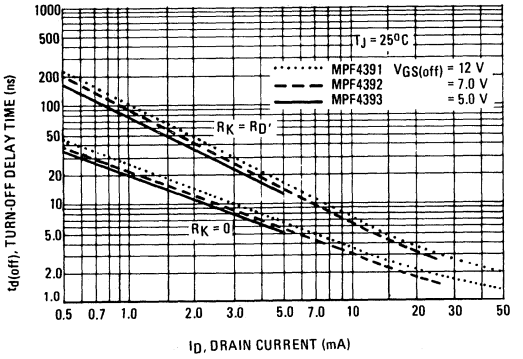


FIGURE 4 – FALL TIME

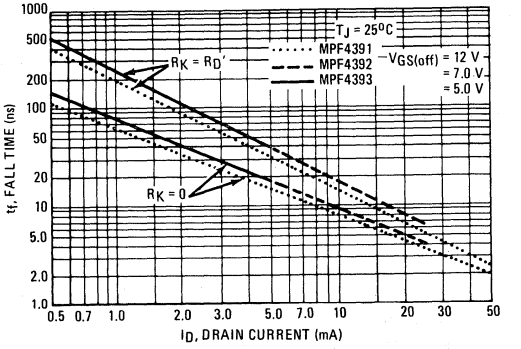
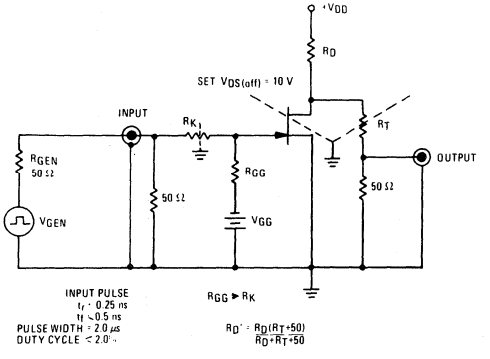


FIGURE 5 – SWITCHING TIME TEST CIRCUIT



NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain-Source Resistance (r_{ds}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds}, turn-on time is non-linear. During turn-off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D' which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

FIGURE 6 – TYPICAL FORWARD TRANSFER ADMITTANCE

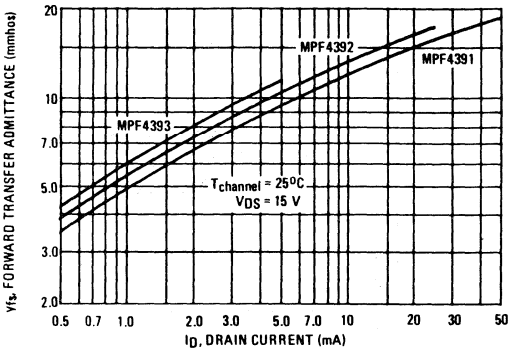


FIGURE 7 – TYPICAL CAPACITANCE

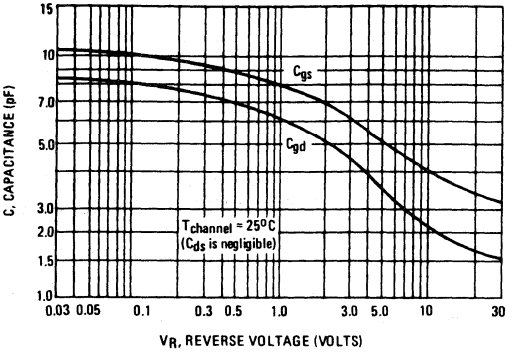


FIGURE 8 – EFFECT OF GATE-SOURCE VOLTAGE ON DRAIN-SOURCE RESISTANCE

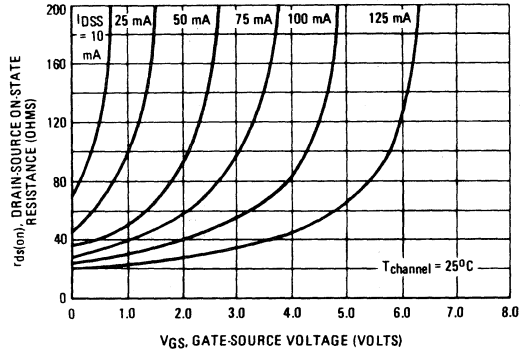


FIGURE 9 – EFFECT OF TEMPERATURE ON DRAIN–SOURCE ON-STATE RESISTANCE

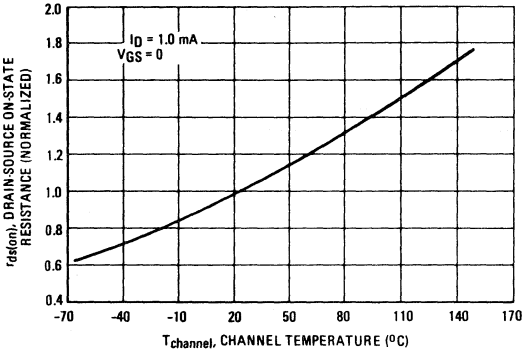
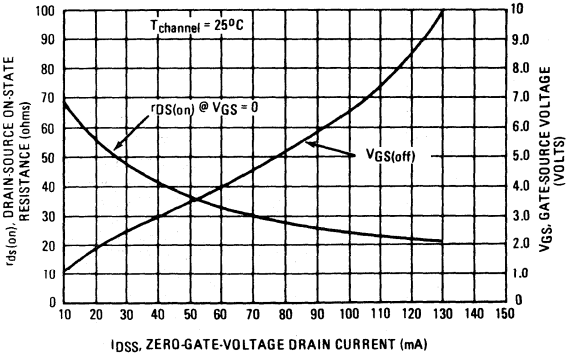


FIGURE 10 – EFFECT OF IDSS ON DRAIN-SOURCE RESISTANCE AND GATE-SOURCE VOLTAGE



NOTE 2

The Zero-Gate-Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ($V_{GS(off)}$) and Drain-Source On Resistance ($r_{ds(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

$r_{ds(on)}$ and V_{GS} range for an MPF4392

The electrical characteristics table indicates that an MPF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10, shows $r_{ds(on)}$ = 52 Ohms for I_{DSS} = 25 mA and 30 Ohms for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 volts and 4.8 volts.

2N4117,A
2N4118,A • 2N4119,A

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

These devices are designed for very low input current DC amplifier applications.

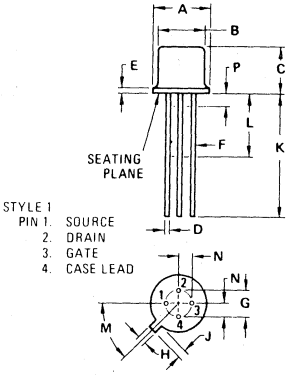
- Ultra-Low Input Leakage Current –
  I_{GSS} = 1.0 pAdc (Max) – 2N4117A, 18A, 19A
  = 10 pAdc (Max) – 2N4117, 18, 19

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

***MAXIMUM RATINGS**

Rating	Symbol	Max	Unit
Gate-Source Voltage	V_{DS}	-40	Vdc
Gate-Drain Voltage	V_{DG}	-40	Vdc
Gate Current	I_G	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +175	°C
Lead Temperature (1/16" from case for 10 s)	T_{LEAD}	255	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		BV_{GSS}	-40	–	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = 20 Vdc, V_{DS} = 0)	2N4117, 4118, 4119		–	-10	pAdc
	2N4117A, 4118A, 4119A		–	-1.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 150°C)	2N4117, 4118, 4119		–	-25	nAdc
	2N4117A, 4118A, 4119A		–	-2.5	
Gate-Source Cutoff Voltage		$V_{GS(off)}$			Vdc
(I_D = 1.0 nAdc, V_{DS} = 10 Vdc)	2N4117, A		-0.6	-1.8	
	2N4118, A		-1.0	-3.0	
	2N4119, A		-2.0	-6.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = 10 Vdc, V_{GS} = 0)	2N4117, A		0.03	0.09	
	2N4118, A		0.08	0.24	
	2N4119, A		0.20	0.60	
DYNAMIC CHARACTERISTICS					
Small-Signal Common-Source Forward Transconductance		g_{fs}			μmhos
(V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N4117, A		70	210	
	2N4118, A		80	250	
	2N4119, A		100	330	
Small-Signal Common-Source Output Conductance		g_{os}			μmhos
(V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N4117, A		–	3.0	
	2N4118, A		–	5.0	
	2N4119, A		–	10	
Input Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	3.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	pF

*Indicates JEDEC Registered Data.

(1) I_{DSS} is measured during a 2.0-ms interval 100 ms after power is applied. (NOT a JEDEC condition.)

FIGURE 1 – TRANSFER CHARACTERISTICS

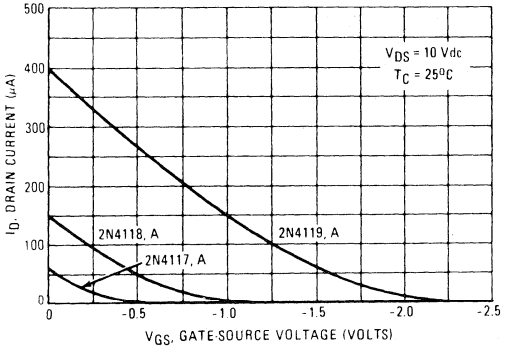
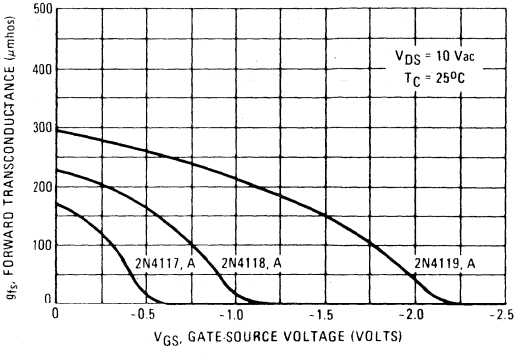
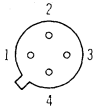


FIGURE 2 – TRANSCONDUCTANCE CHARACTERISTICS



2N4351

CASE 20-02
(TO-72)



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

Silicon N-channel MOS field effect transistors, designed for enhancement-mode operation in low power switching applications. The 2N4351 is complementary with type 2N4352 .

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation at T_C = 25°C Derate about 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±30 Vdc, V_{DS} = 0)	—	I_{GSS}	—	10	pAdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	—	$V_{GS(TH)}$	1.0	5.0	Vdc
"ON" Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	3	$I_{D(on)}$	3.0	—	mAdc
Drain-Source "ON" Voltage (I_D = 2 mA, V_{GS} = 10 V)	—	$V_{DS(on)}$	—	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	300	ohms
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz)	1	$\lvert y_{fs} \rvert$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	1.3	pF
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	2	C_{iss}	—	5.0	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	—	$C_{d(sub)}$	—	5.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay	I_D = 2.0 mAdc, V_{DS} = 10 Vdc, V_{GS} = 10 Vdc (See Figure 10; Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	60	ns
Fall Time		9, 10	t_f	—	100	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

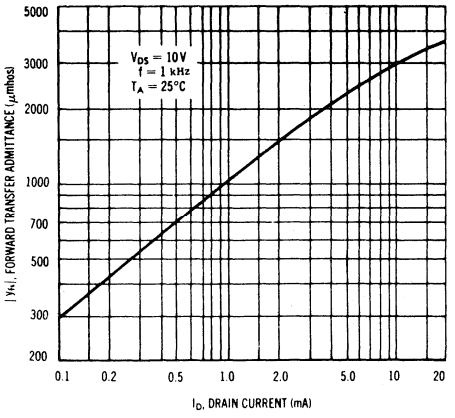


FIGURE 2 — CAPACITANCE

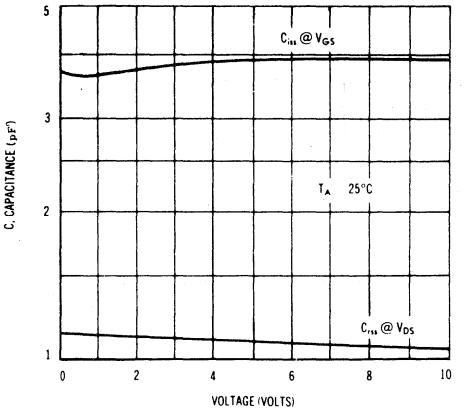


FIGURE 3 — TRANSFER CHARACTERISTICS

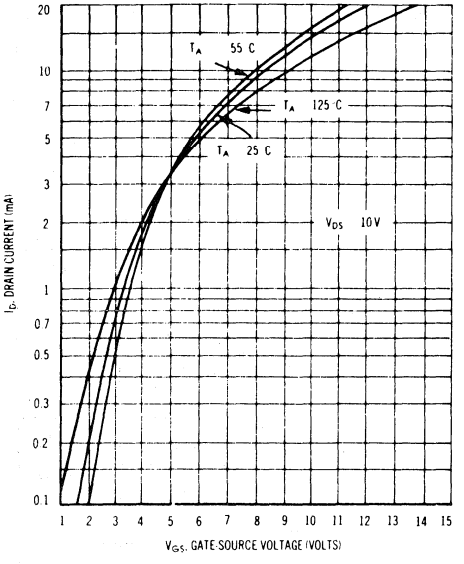


FIGURE 4 — DRAIN SOURCE "ON" RESISTANCE

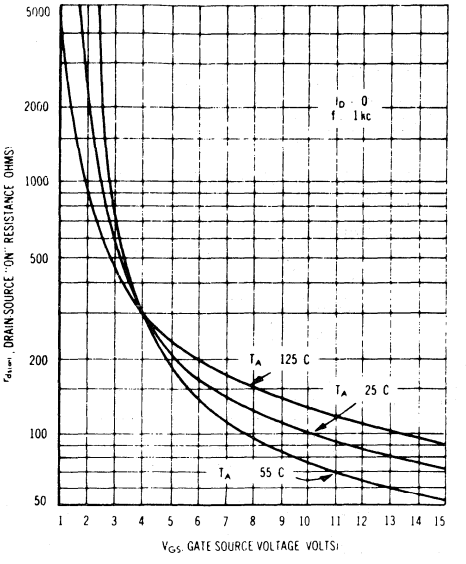
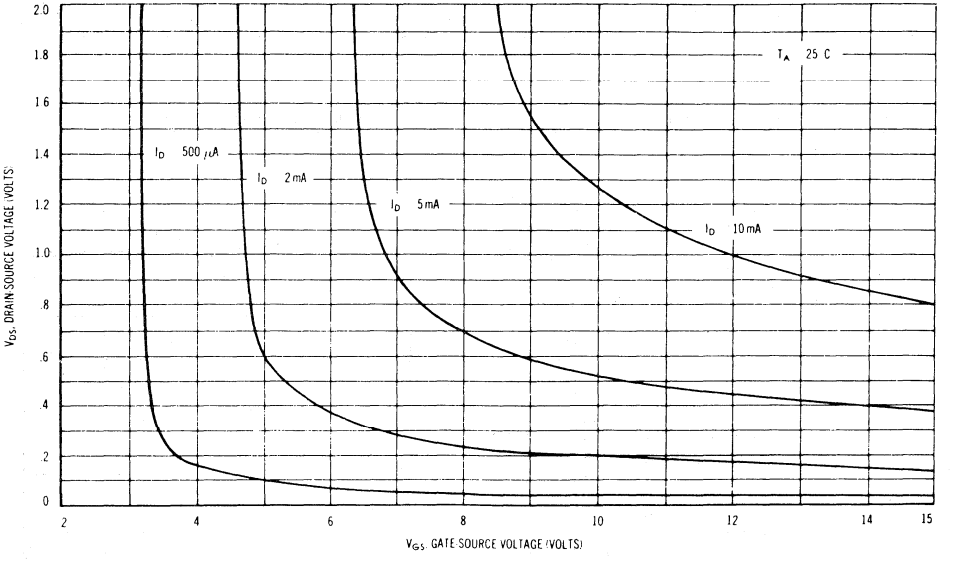


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

(T_A = 25°C)

FIGURE 6 — TURN-ON DELAY TIME

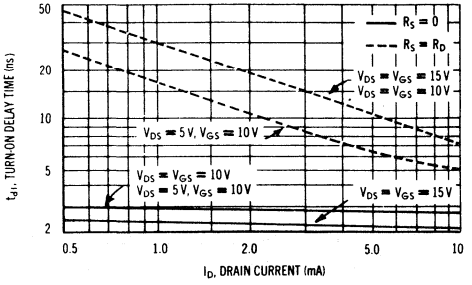


FIGURE 7 — RISE TIME

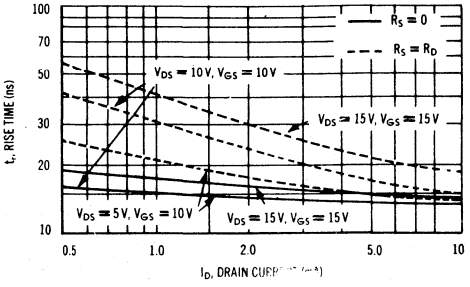


FIGURE 8 — TURN-OFF DELAY TIME

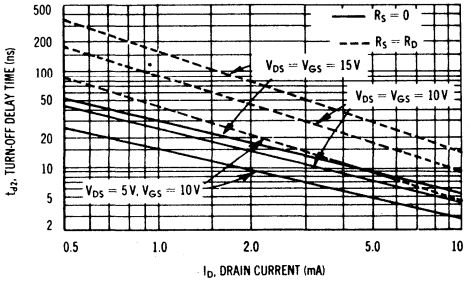


FIGURE 9 — FALL TIME

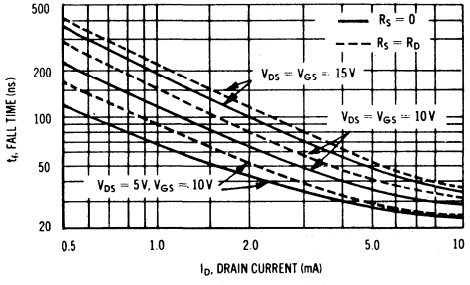
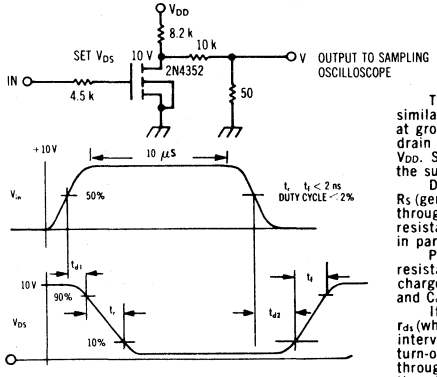


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{rss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

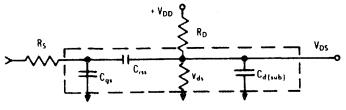
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

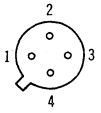
The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



2N4352

CASE 20-02
(TO-72)



STYLE 2
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SUBSTRATE AND CASE LEAD

Silicon P-channel MOS field-effect transistor designed for enhancement-mode operation in low-power switching applications. The 2N4352 is complementary with type 2N4351.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = -10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±30 V, V_{DS} = 0)	—	I_{GSS}	—	10	pAdc
Zero-Gate Voltage Drain Current (V_{DS} = -10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = -10 V, I_D = -10 μA)	—	$V_{GS(TH)}$	1.0	5.0	Vdc
"ON" Drain Current (V_{GS} = -10 V_{DS} = -10 V)	3	$I_{D(on)}$	3.0	—	mA
Drain-Source "ON" Voltage (I_D = -2.0 mA, V_{GS} = -10 V)	5	$V_{DS(on)}$	—	1.0	V
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = -10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	600	ohms
Forward Transfer Admittance (V_{DS} = -10 V, I_D = 2 mA, f = 1 kHz)	1	$\lvert y_{fs} \rvert$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	1.3	pF
Input Capacitance (V_{DS} = -10 V, V_{GS} = 0, f=140 kHz)	2	C_{iss}	—	5.0	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$= -10 V, f=140 kHz)	—	$C_{d(sub)}$	—	4.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay	I_D = -2.0 mAdc, V_{DS} = -10 Vdc, V_{GS} = -10 V (See Figure 10, Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	60	ns
Fall Time		9, 10	t_f	—	100	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

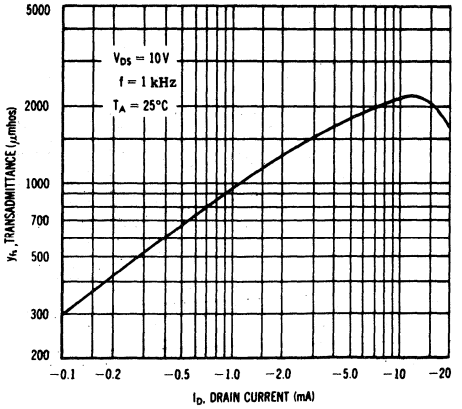


FIGURE 2 — CAPACITANCE

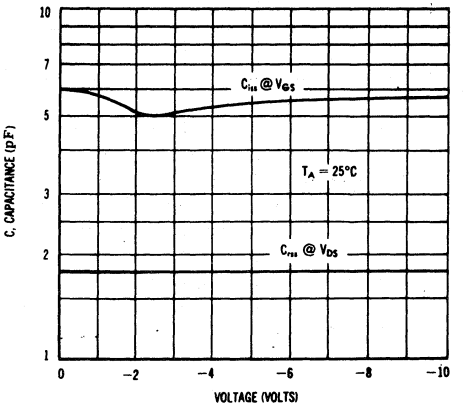


FIGURE 3 — TRANSFER CHARACTERISTICS

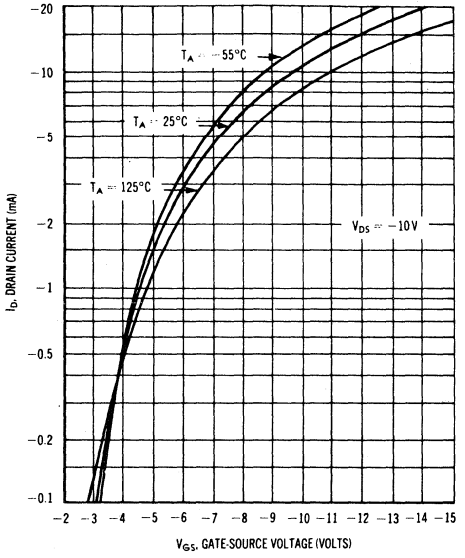


FIGURE 4 — DRAIN SOURCE "ON" RESISTANCE

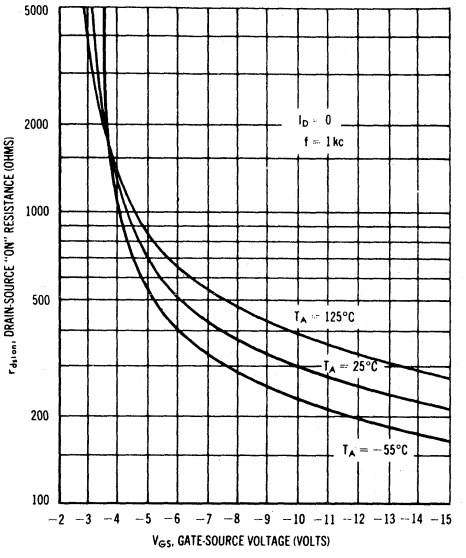
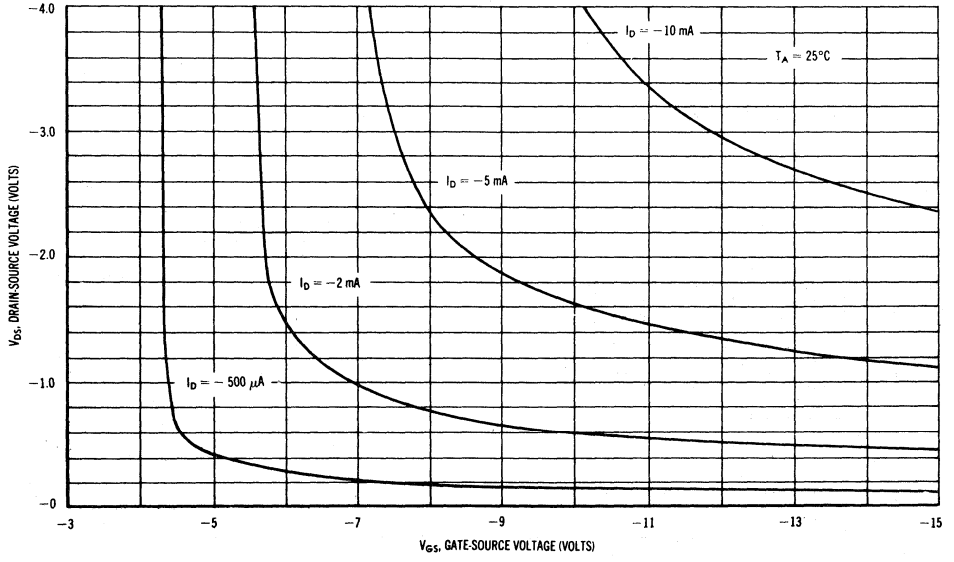


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

($T_A = 25°C$)

FIGURE 6 — TURN-ON DELAY TIME

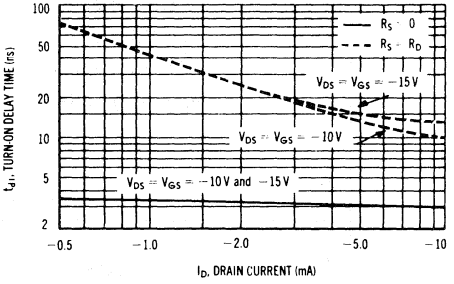


FIGURE 7 — RISE TIME

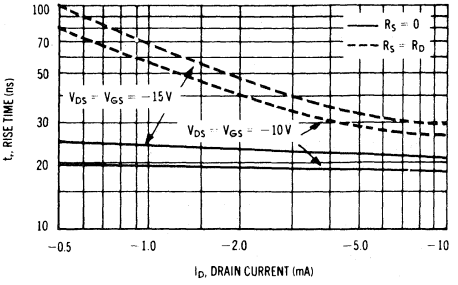


FIGURE 8 — TURN-OFF DELAY TIME

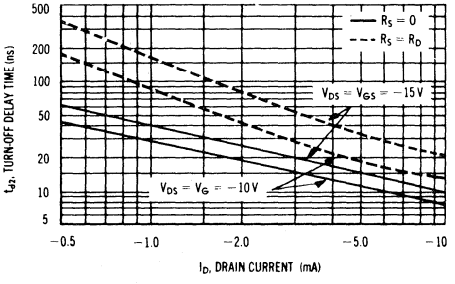


FIGURE 9 — FALL TIME

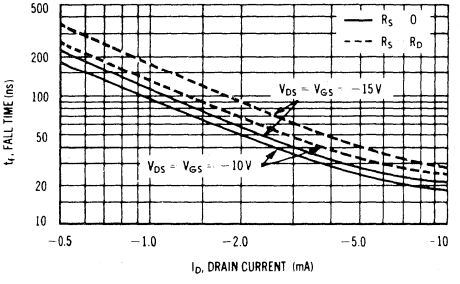
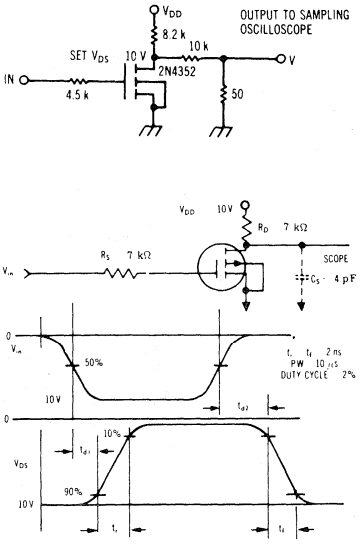


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

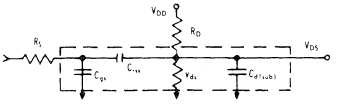
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



2N4416

SILICON N-CHANNEL
JUNCTION FIELD-EFFECT TRANSISTOR

. . . designed for VHF/UHF amplifier applications.

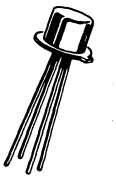
- Low Noise Figure –
  NF = 2.0 dB (Max) @ 100 MHz
  = 4.0 dB (Max) @ 400 MHz
- Low Feedback Capacitance –
  C_{rss} = 0.8 pF (Max)
- Low Output Capacitance –
  C_{oss} = 2.0 pF (Max)
- High Transfer Admittance –
  $Y_{fs(real)}$ = 4000 μmho (Min)
- High Power Gain –
  G_{ps} = 18 dB (Min) @ 100 MHz
  = 10 dB (Min) @ 400 MHz
- S and Y Parameter Curves Provided

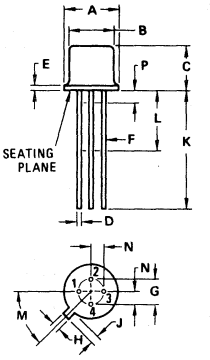
***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	30	Vdc
Gate Current	I_G	10	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

N-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTOR





STYLE 1
PIN 1. SOURCE
2. DRAIN
3. GATE
4. CASE LEAD

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTIC				
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	30	–	Vdc
Gate-Source Cutoff Voltage (I_D = 1.0 nAdc, V_{DS} = 15 Vdc)	$V_{GS(off)}$	–	6.0	Vdc
Gate-Source Voltage (I_D = 0.5 mAdc, V_{DS} = 15 Vdc)	V_{GS}	1.0	5.5	Vdc
Gate-Source Forward Voltage (I_G = 1.0 mAdc, V_{DS} = 0)	$V_{GS(F)}$	–	1.0	Vdc
Gate Reverse Current	I_{GSS}			pAdc
(V_{GS} = 20 Vdc, V_{DS} = 0)		–	100	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = +150°C)		–	200	
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	5.0	15	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{fs}\|$	4500	7500	μmhos
Real Part of Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	$y_{fs(real)}$	4000	–	μmhos
Real Part of Input Admittance	$y_{is(real)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	100	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	1000	
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	–	50	μmhos
Real Part of Output Admittance	$y_{os(real)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	75	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	100	
Imaginary Part of Input Admittance	$y_{is(imag)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	2500	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	10,000	
Imaginary Part of Output Admittance	$y_{os(imag)}$			μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)		–	1000	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)		–	4000	
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	4.0	pF
Common-Source Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	–	2.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	–	0.8	pF
Common-Source Spot Noise (Figures 3 and 4)	NF			dB
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx$ 1000 Ohms, f = 100 MHz)		–	2.0	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, $R_g \approx$ 1000 Ohms, f = 400 MHz)		–	4.0	
Small-Signal Power Gain (Figure 1)	G_{ps}			dB
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 100 MHz)		18	–	
(V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 400 MHz)		10	–	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1.0%.

*Indicates JEDEC Registered Data.

POWER GAIN

FIGURE 1 – EFFECTS OF DRAIN CURRENT

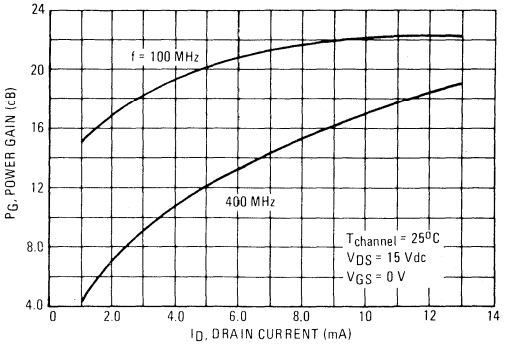
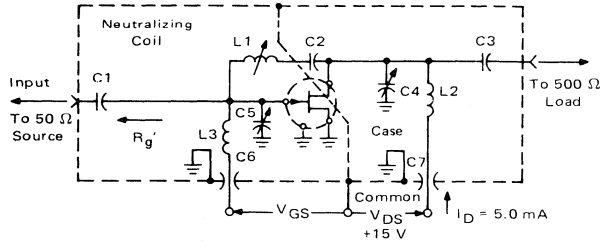


FIGURE 2 – 100 MHz and 400 MHz NEUTRALIZED TEST CIRCUIT



Adjust V_{GS} for I_D = 50 mA
V_{GS} < 0 Volts

NOTE: The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	17 pF
C3	3.0 pF	1.0 pF
C4	1-12 pF	0.8-8.0 pF
C5	1-12 pF	0.8-8.0 pF
C6	0.0015 μF	0.001 μF
C7	0.0015 μF	0.001 μF
L1	3.0 μH*	0.2 μH**
L2	0.15 μH*	0.03 μH**
L3	0.14 μH*	0.022 μH**

*L1 17 turns, (approx. – depends upon circuit layout) AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L2 4-1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I.D. (AIR CORE).

L3 3-1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I.D. (AIR CORE).

**L1 6 turns, (approx. – depends upon circuit layout) AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L2 1 turn, AWG #16 enameled copper wire, 3/8" I.D. (AIR CORE).

L3 1/2 turn, AWG #16 enameled copper wire, 1/4" I.D. (AIR CORE).

NOISE FIGURE

($T_{channel}$ = 25°C)

FIGURE 3 – EFFECTS OF DRAIN-SOURCE VOLTAGE

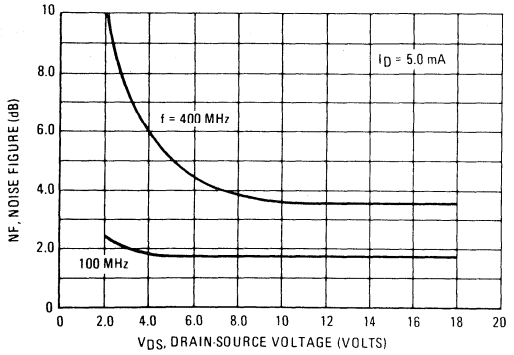
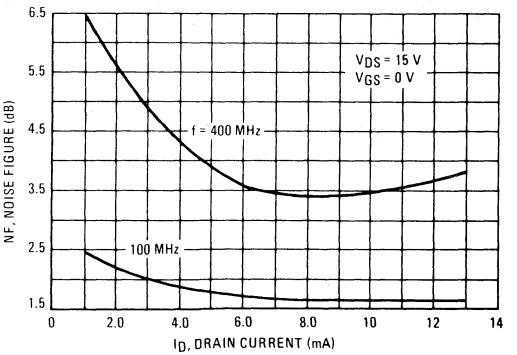
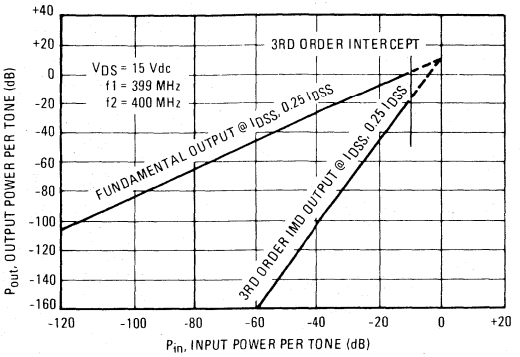


FIGURE 4 – EFFECTS OF DRAIN CURRENT



INTERMODULATION CHARACTERISTICS

FIGURE 5 – THIRD ORDER INTERMODULATION DISTORTION



COMMON SOURCE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C)

FIGURE 6 – INPUT ADMITTANCE (y_{is})

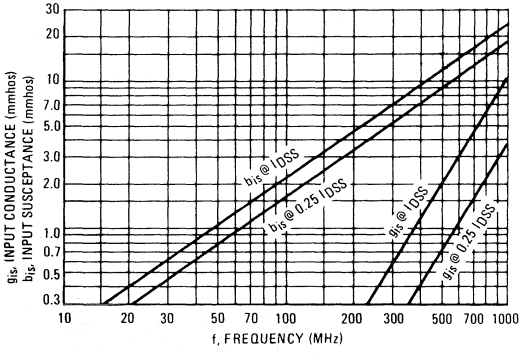


FIGURE 7 – REVERSE TRANSFER ADMITTANCE (y_{rs})

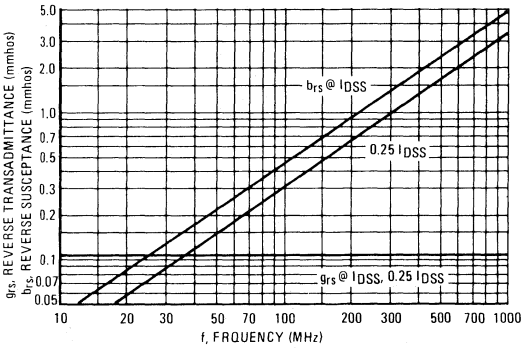


FIGURE 8 – FORWARD TRANSADMITTANCE (y_{fs})

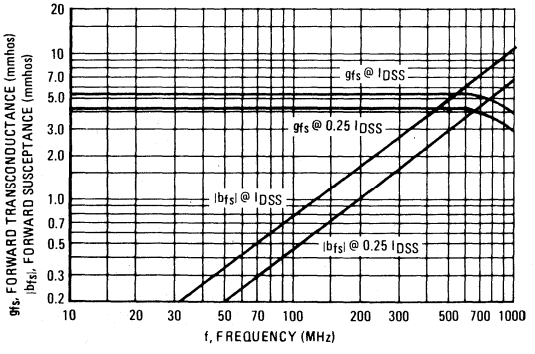
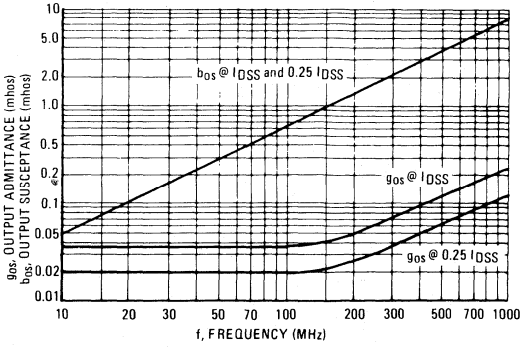


FIGURE 9 – OUTPUT ADMITTANCE (y_{os})



COMMON SOURCE CHARACTERISTICS

S-PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

FIGURE 10 – S_{11s}

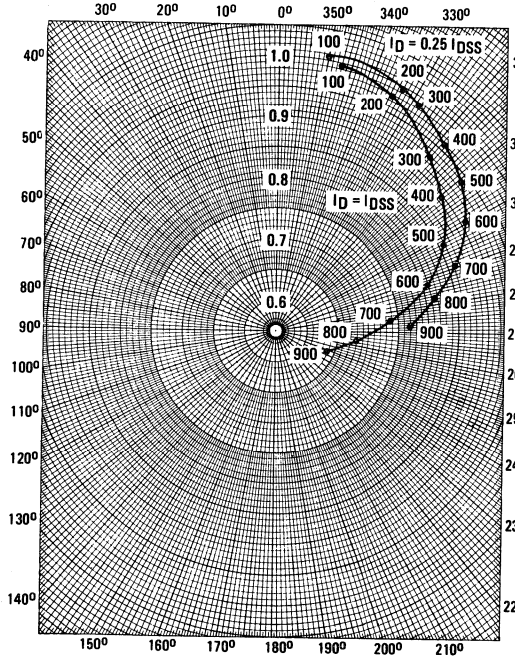


FIGURE 11 – S_{12s}

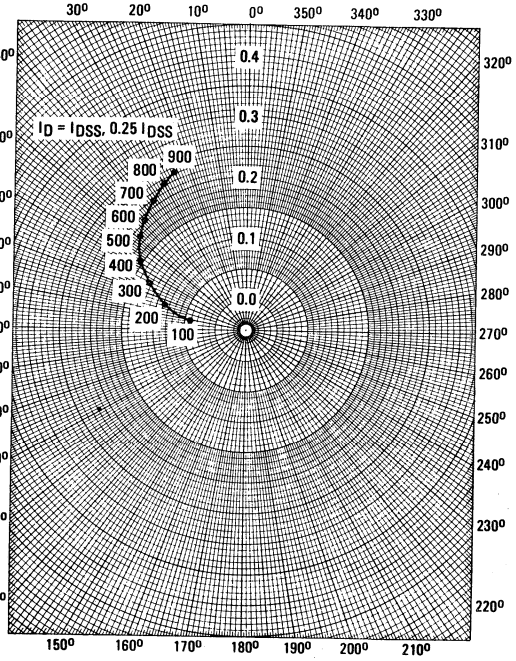


FIGURE 12 – S_{21s}

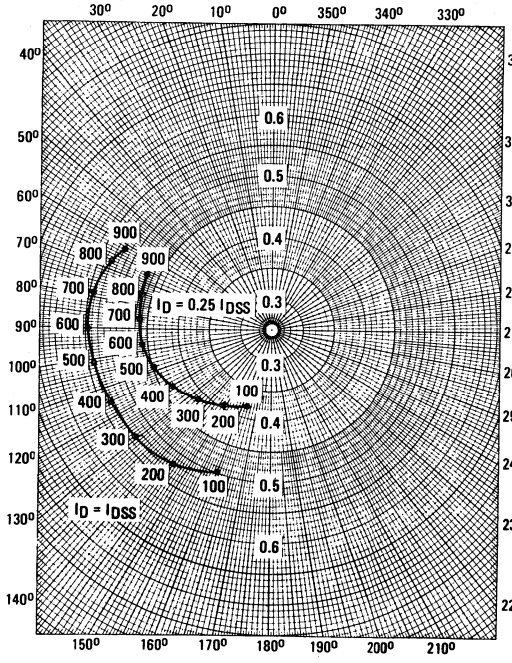
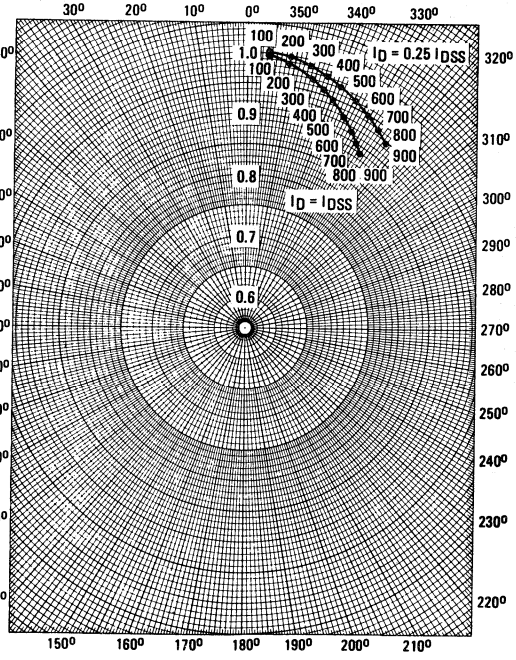


FIGURE 13 – S_{22s}



COMMON GATE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DG} = 15 Vdc, $T_{channel}$ = 25°C)

FIGURE 14 – INPUT ADMITTANCE (y_{ig})

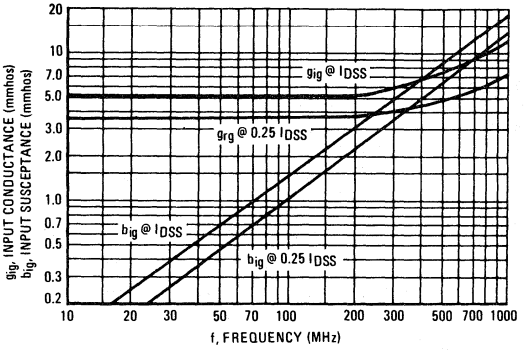


FIGURE 15 – REVERSE TRANSFER ADMITTANCE (y_{rg})

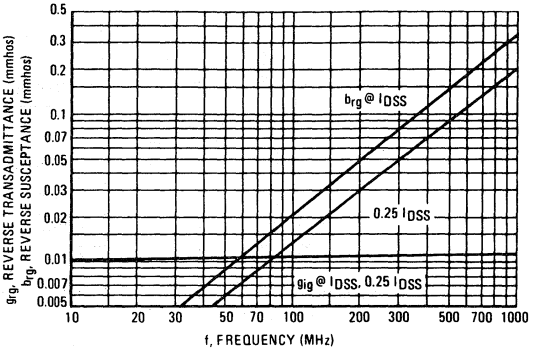


FIGURE 16 – FORWARD TRANSFER ADMITTANCE (y_{fg})

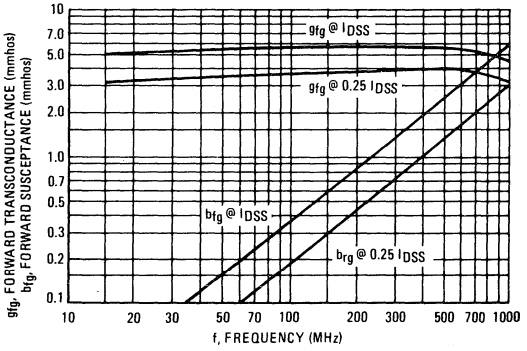
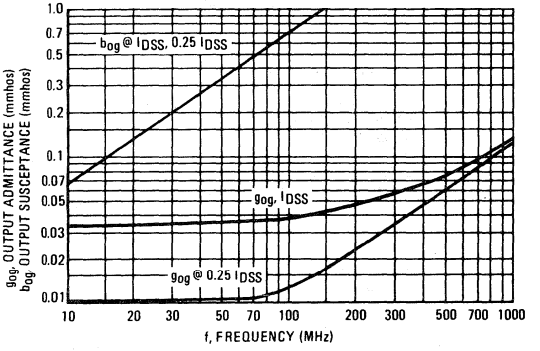
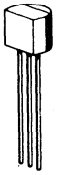


FIGURE 17 – OUTPUT ADMITTANCE (y_{og})



2N5457
2N5458 • 2N5459

Silicon N-channel junction field-effect transistors depletion mode (Type A) designed for general-purpose audio and switching applications.



STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 29
(TO-92)

Drain and source may be interchanged.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (2)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (2)	135	°C
Storage Temperature Range	T_{stg} (2)	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

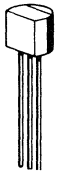
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)		BV_{GSS}	25	—	—	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	1.0	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			—	—	200	
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	0.5	—	6.0	Vdc
	2N5458		1.0	—	7.0	
	2N5459		2.0	—	8.0	
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	—	2.5	—	Vdc
(V_{DS} = 15 Vdc, I_D = 200 μAdc)	2N5458		—	3.5	—	
(V_{DS} = 15 Vdc, I_D = 400 μAdc)	2N5459		—	4.5	—	
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
	2N5458		2.0	6.0	9.0	
	2N5459		4.0	9.0	16	
DYNAMIC CHARACTERISTICS						
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	2N5457	$\|y_{fs}\|$	1000	3000	5000	μmhos
	2N5458		1500	4000	5500	
	2N5459		2000	4500	6000	
Output Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)		$\|y_{os}\|$	—	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	1.5	3.0	pF

(1) **Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%**

(2) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

2N5460 thru 2N5465

P-channel depletion mode (Type A) junction field-effect transistors designed for use in general-purpose amplifier applications.



CASE 29
(TO-92)

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82		mW mW/°C
Storage Temperature Range	T_{stg} (1)	-65 to +150		°C
Operating Junction Temperature Range	T_J (1)	-65 to +135		°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125°C/W.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	$V_{(BR)GSS}$	40 60	- -	- -	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$V_{GS(off)}$	0.75 1.0 1.8	- - -	6.0 7.5 9.0	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	I_{GSS}	-	-	5.0	nAdc
(V_{GS} = 30 Vdc, V_{DS} = 0)	2N5463, 2N5464, 2N5465		-	-	5.0	
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462		-	-	1.0	μAdc
(V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	2N5463, 2N5464, 2N5465		-	-	1.0	
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	I_{DSS}	1.0 2.0 4.0	- - -	5.0 9.0 16	mAdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc)	2N5460, 2N5463	V_{GS}	0.5	-	4.0	Vdc
(V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	2N5461, 2N5464		0.8	-	4.5	
(V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5462, 2N5465		1.5	-	6.0	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$\lvert y_{fs} \rvert$	1000 1500 2000	- - -	4000 5000 6000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os} \rvert$	-	-	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	-	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	-	1.0	2.0	pF
Common-Source Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	-	1.0	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	-	60	115	$nV/\sqrt{Hz}$

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 – 2N5460 and 2N5463

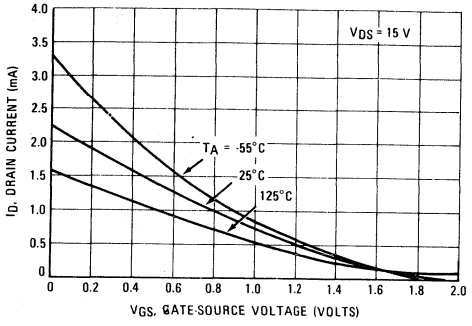


FIGURE 2 – 2N5461 and 2N5464

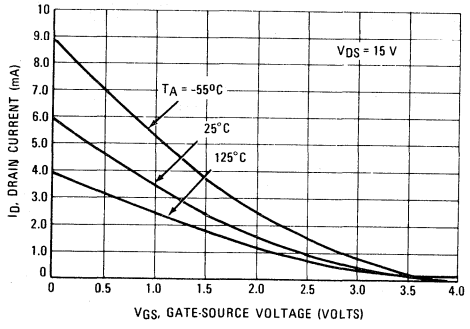
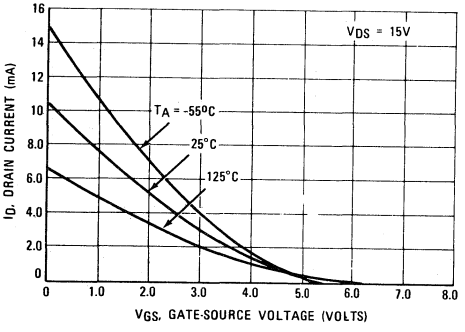


FIGURE 3 – 2N5462 and 2N5465



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 4 – 2N5460 and 2N5463

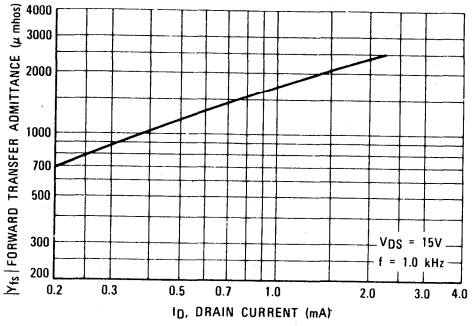


FIGURE 5 – 2N5461 and 2N5464

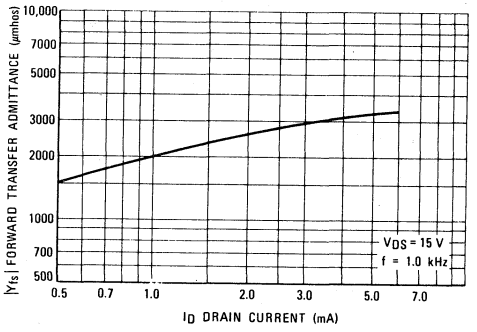


FIGURE 6 – 2N5462 and 2N5465

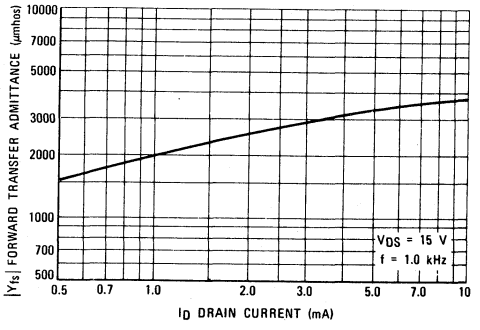


FIGURE 7 – OUTPUT RESISTANCE VERSUS DRAIN CURRENT

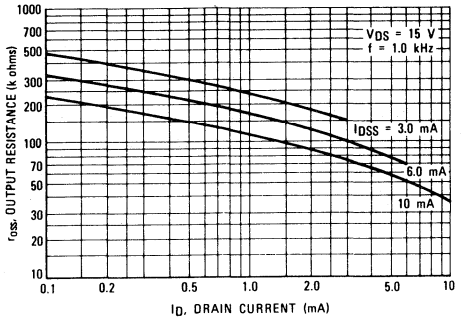


FIGURE 8 – CAPACITANCE VERSUS DRAIN-SOURCE VOLTAGE

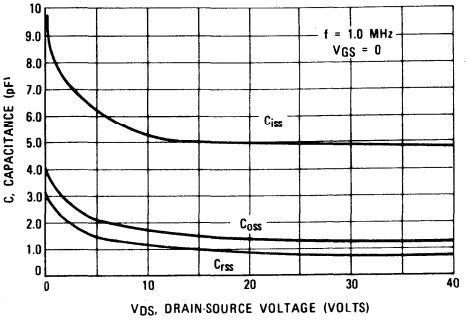


FIGURE 9 – NOISE FIGURE VERSUS FREQUENCY

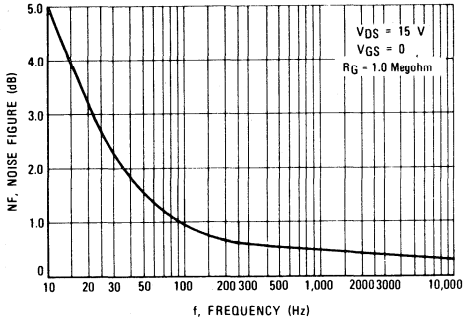


FIGURE 10 – NOISE FIGURE VERSUS SOURCE RESISTANCE

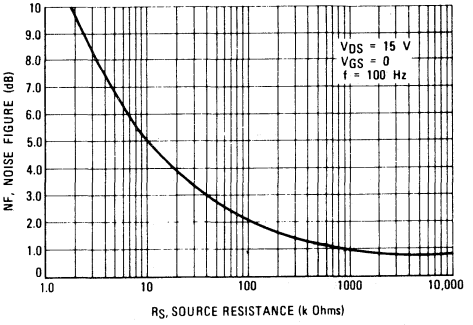
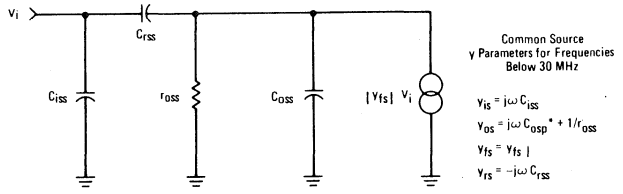


FIGURE 11 – EQUIVALENT LOW FREQUENCY CIRCUIT



*Cosp is Coss in parallel with Series Combination of Ciss and Crss.

NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

2N5484 thru 2N5486

N-channel depletion mode (Type A) junction field-effect transistors designed for VHF/UHF amplifier applications.

CASE 29
(TO-92)

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-65 to +150	°C

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

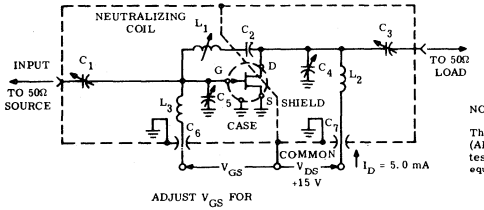
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	25	-	-	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484	$V_{GS(off)}$	0.3	-	3.0	Vdc
	2N5485		0.5	-	4.0	
	2N5486		2.0	-	6.0	
Gate Reverse Current (V_{GS} = -20 Vdc, V_{DS} = 0)		I_{GSS}	-	-	1.0	nAdc
(V_{GS} = -20 Vdc, V_{DS} = 0, T_A = 100°C)			-	-	0.2	μAdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5484	I_{DSS}	1.0	-	5.0	mAdc
	2N5485		4.0	-	10	
	2N5486		8.0	-	20	

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance		$\|y_{fs}\|$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		3000	-	6000	
	2N5485		3500	-	7000	
	2N5486		4000	-	8000	
Forward Transconductance		$Re(y_{fs})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		2500	-	-	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485		3000	-	-	
	2N5486		3500	-	-	
Output Admittance		$\|y_{os}\|$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		-	-	50	
	2N5485		-	-	60	
	2N5486		-	-	75	
Output Conductance		$Re(y_{os})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		-	-	75	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	100	
Input Conductance		$Re(y_{is})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		-	-	100	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		-	-	1000	
Input Capacitance		C_{iss}				pF
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)			-	-	5.0	
Reverse Transfer Capacitance		C_{rss}				pF
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)			-	-	1.0	
Output Capacitance		C_{oss}				pF
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)			-	-	2.0	
Common-Source Noise Figure		NF				dB
(V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 1.0 kHz)	All Types		-	-	2.5	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, R_G ≈ 1.0 k ohm, f = 100 MHz)	2N5484		-	-	3.0	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, R_G ≈ 1.0 k ohm, f = 200 MHz)	2N5484		-	4.0	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, R_G ≈ 1.0 k ohm, f = 100 MHz)	2N5485, 2N5486		-	-	2.0	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, R_G ≈ 1.0 k ohm, f = 400 MHz)	2N5485, 2N5486		-	-	4.0	
Insertion Power Gain		G_{ps}				dB
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 100 MHz)	2N5484		16	-	25	
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 200 MHz)	2N5484		-	14	-	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 100 MHz)	2N5485, 2N5486		18	-	30	
(V_{DS} = 15 Vdc, I_D = 4.0 mAdc, f = 400 MHz)	2N5485, 2N5486		10	-	20	

FIGURE 1 – 100 MHz AND 400 MHz NEUTRALIZED AMPLIFIER



ADJUST V_{GS} FOR
I_D = 5.0 mA
V_{GS} < 0 VOLTS

NOTE:

The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

Reference Designation	VALUE 100 MHz	VALUE 400 MHz
C_1	1-12 pF	0.8-8.0 pF
C_2	1000 pF	27 pF
C_3	1-12 pF	0.8-8.0 pF
C_4	1-12 pF	0.8-8.0 pF
C_5	1-12 pF	0.8-8.0 pF
C_6	0.0015 μF	0.001 μF
C_7	0.0015 μF	0.001 μF
L_1	3.0 μH*	0.2 μH**
L_2	0.25 μH*	0.03 μH**
L_3	0.14 μH*	0.022 μH**

* L_1 17 turns (approximately - depending upon circuit layout), AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.

L_2 4 1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I. D. (AIR CORE).

L_3 3 1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I. D. (AIR CORE).

** L_1 6 turns (approximately - depending upon circuit layout), AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.

L_2 1 turn, AWG #16 enameled copper wire, 3/8" I. D. (AIR CORE).

L_3 1/2 turn, AWG #16 enameled copper wire, 1/4" I. D. (AIR CORE).

2N5638
2N5639 • 2N5640

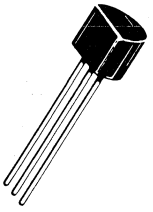
N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

. . . depletion mode (Type A) Junction Field-Effect Transistors designed for chopper and high-speed switching applications.

- Low Drain-Source "ON" Resistance –
  $r_{ds(on)}$ = 30 Ohms (2N5638)
  60 Ohms (2N5639)
  100 Ohms (2N5640)
- Low Reverse Transfer Capacitance –
  C_{rss} = 4.0 pF (Max) @ f = 1.0 MHz
- Fast Switching Characteristics –
  t_r = 5.0 ns (Max) (2N5638)

N-CHANNEL
JUNCTION
FIELD-EFFECT
TRANSISTORS

TYPE A

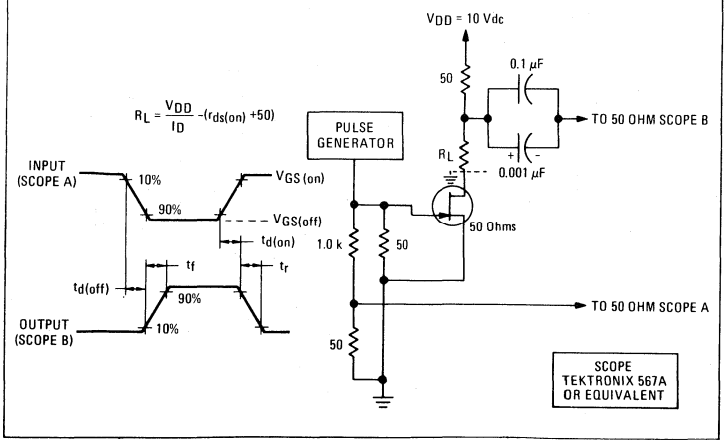


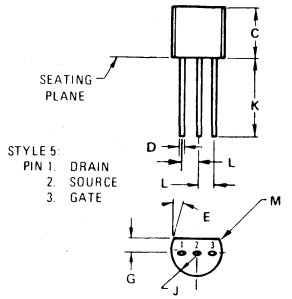
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
*Drain-Gate Voltage	V_{DG}	30	Vdc
*Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
*Forward Gate Current	I_{GF}	10	mAdc
*Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	-65 to +135	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
C	0.175	0.185	4.450	4.700
D	0.016	0.019	0.407	0.482
E	5° NOM		5° NOM	
G	0.045	0.055	1.150	1.390
J	0.085	0.095	2.160	2.420
K	0.500	–	12.700	–
L	0.050 TP		1.270 TP	
M	0.003	0.013	0.076	0.330

CASE 29(5)
TO-92

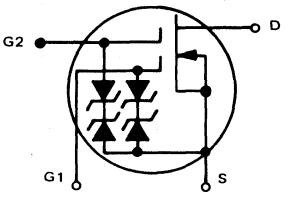
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	–	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = -15 Vdc, V_{DS} = 0)			–	1.0	nAdc
(V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)			–	1.0	μAdc
Drain Cutoff Current		$I_{D(off)}$			
(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc)	2N5638		–	1.0	μAdc
(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -6.0 Vdc)	2N5640		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -12 Vdc, T_A = 100°C)	2N5638		–	1.0	μAdc
(V_{DS} = 15 Vdc, V_{GS} = -8.0 Vdc, T_A = 100°C)	2N5639		–	1.0	
(V_{DS} = 15 Vdc, V_{GS} = -6.0 Vdc, T_A = 100°C)	2N5640		–	1.0	
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (Note 1)		I_{DSS}			mAdc
(V_{DS} = 20 Vdc, V_{GS} = 0)	2N5638		50	–	
	2N5639		25	–	
	2N5640		5.0	–	
Drain-Source "ON" Voltage		$V_{DS(on)}$			Vdc
(I_D = 12 mAdc, V_{GS} = 0)	2N5638		–	0.5	
(I_D = 6.0 mAdc, V_{GS} = 0)	2N5639		–	0.5	
(I_D = 3.0 mAdc, V_{GS} = 0)	2N5640		–	0.5	
Static Drain-Source "ON" Resistance		$r_{DS(on)}$			Ohms
(I_D = 1.0 mAdc, V_{GS} = 0)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
SMALL-SIGNAL CHARACTERISTICS					
Static Drain-Source "ON" Resistance		$r_{ds(on)}$			Ohms
(V_{GS} = 0, I_D = 0, f = 1.0 kHz)	2N5638		–	30	
	2N5639		–	60	
	2N5640		–	100	
Input Capacitance (V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{iss}	–	10	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = -12 Vdc, f = 1.0 MHz)		C_{rss}	–	4.0	pF
SWITCHING CHARACTERISTICS (Figure 1)					
Turn-On Delay Time	V_{DD} = 10 Vdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -10 Vdc, R_G' = 50 ohms	$I_{D(on)}$ = 12 mAdc 2N5638	$t_{d(on)}$	–	4.0	ns
		6.0 mAdc 2N5639		–	6.0	
		3.0 mAdc 2N5640		–	8.0	
Rise Time		$I_{D(on)}$ = 12 mAdc 2N5638	t_r	–	5.0	ns
		6.0 mAdc 2N5639		–	8.0	
		3.0 mAdc 2N5640		–	10	
Turn-Off Delay Time		$I_{D(on)}$ = 12 mAdc 2N5638	$t_{d(off)}$	–	5.0	ns
		6.0 mAdc 2N5639		–	10	
		3.0 mAdc 2N5640		–	15	
Fall Time		$I_{D(on)}$ = 12 mAdc 2N5638	t_f	–	10	ns
		6.0 mAdc 2N5639		–	20	
		3.0 mAdc 2N5640		–	30	

*Indicates JEDEC Registered Data.

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 3.0%.

3N201
3N202 • 3N203

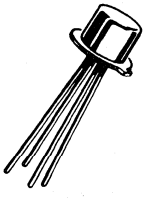


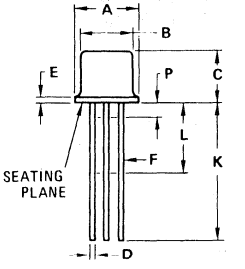
N-CHANNEL
DUAL GATE
MOS FIELD-EFFECT
TRANSISTORS

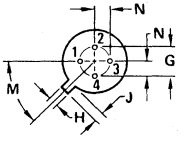
N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . depletion mode dual gate transistors designed for VHF amplifier and mixer applications.

- 3N201 – VHF Amplifier
  3N202 – VHF Mixer
  3N203 – IF Amplifier
- Low Reverse Transfer Capacitance –
  C_{rss} = 0.03 pF (Max)
- High Forward Transfer Admittance –
  $|y_{fs}|$ = 8.0 - 20 mmhos – 3N201, 3N202
  = 7.0 - 15 mmhos – 3N203
- Diode Protected Gates







STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain – Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG1} V_{DG2}	30 30	Vdc Vdc
Gate Current	I_{G1} I_{G2}	±10 ±10	mAdc mAdc
Drain Current – Continuous	I_D	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	360 2.4	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 8.0	Watt mW/°C
Storage Channel Temperature Range	T_{stg}	-65 to +200	°C
Junction Temperature Range	T_J	-65 to +175	°C
Lead Temperature, 1/16" From Seated Surface for 10 Seconds	T_L	300	°C

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1S} = V_{G2S} = -5.0 Vdc)	$V_{(BR)DSX}$	25	–	–	Vdc
Gate 1 – Source Breakdown Voltage (1) (I_{G1} = ±10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SO}$	±6.0	–	±30	Vdc
Gate 2 – Source Breakdown Voltage (1) (I_{G2} = ± 10 mAdc, V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SO}$	±6.0	–	±30	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 20 μAdc)	$V_{G1S(off)}$	-0.5	-1.5	-5.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 20 μAdc)	$V_{G2S(off)}$	-0.2	-1.4	-5.0	Vdc
Gate 1 Leakage Current	I_{G1SS}				
(V_{G1S} = ±5.0 Vdc, V_{G2S} = V_{DS} = 0)		–	±.040	±10	nAdc
(V_{G1S} = -5.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)		–	–	-10	μAdc
Gate 2 Leakage Current	I_{G2SS}				
(V_{G2S} = ±5.0 Vdc, V_{G1S} = V_{DS} = 0)		–	±.050	±10	nAdc
(V_{G2S} = -5.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)		–	–	-10	μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (2)	I_{DSS}				mAdc
(V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc) 3N201,3N202		6.0	13	30	
3N203		3.0	11	15	
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (3)	$\|Y_{fs}\|$				mmhos
(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, V_{G1S} = 0, f = 1.0 kHz)					
3N201,3N202		8.0	12.8	20	
3N203		7.0	12.5	15	
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	–	4.3	–	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	–	1.7	–	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)	C_{rss}	0.005	0.014	0.03	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure	NF				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		–	1.8	4.5	dB
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		–	5.3	6.0	
Common Source Power Gain	G_{ps}				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		15	20	25	dB
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		20	25	30	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2) 3N202	G_c(5)	15	19	25	
Bandwidth	BW				
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201		5.0	–	9.0	MHz
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2) 3N202		4.5	–	7.5	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203		3.0	–	6.0	
Gain Control Gate-Supply Voltage (4)	$V_{GG(GC)}$				
(V_{DD} = 18 Vdc, $\pm G_{ps}$ = -30 dB, f = 200 MHz) (Figure 1) 3N201		0	-1.0	-3.0	Vdc
(V_{DD} = 18 Vdc, $\pm G_{ps}$ = -30 dB, f = 45 MHz) (Figure 3) 3N203		0	-0.6	-3.0	

* Indicates JEDEC Registered Data.

(1) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

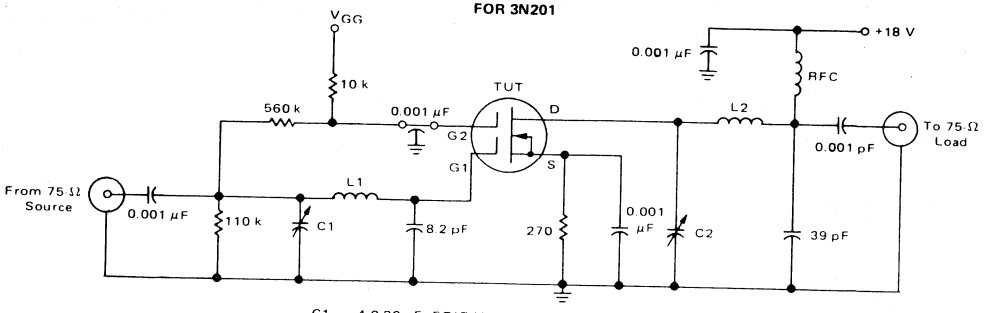
(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

(3) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

(4) $\pm G_{ps}$ is defined as the change in G_{ps} from the value at V_{GG} = 7.0 volts (3N201) and V_{GG} = 6.0 volts (3N203).

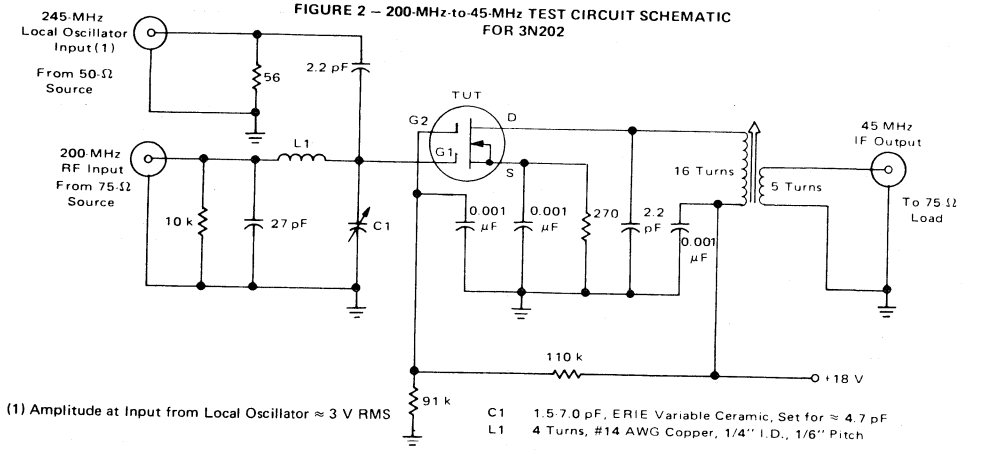
(5) Power Gain Conversion

FIGURE 1 – 200-MHz TEST CIRCUIT SCHEMATIC FOR 3N201



C1 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 22 pF
C2 4.0-30 pF, ERIE Variable Ceramic, Set for ≈ 10 pF
L1 4 Turns, #14 AWG Cooper, 1/4" I.D., 1/6" Pitch
L2 3 Turns, #14 AWG Cooper, 1/4" I.D., 1/8" Pitch
RFC DELEVAN No. 153712, 1.0 µH

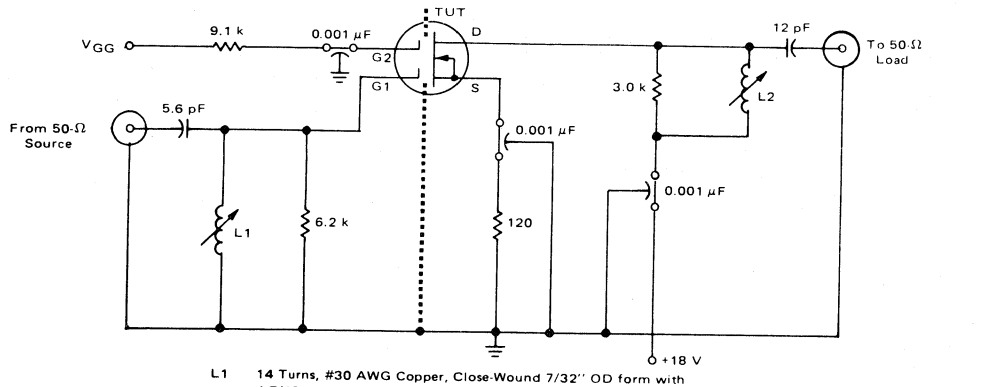
FIGURE 2 – 200-MHz-to-45-MHz TEST CIRCUIT SCHEMATIC FOR 3N202



(1) Amplitude at Input from Local Oscillator ≈ 3 V RMS

C1 1.5-7.0 pF, ERIE Variable Ceramic, Set for ≈ 4.7 pF
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch

FIGURE 3 – 45-MHz TEST CIRCUIT SCHEMATIC 3N203



L1 14 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core
L2 10 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core

TYPICAL CHARACTERISTICS

FIGURE 4 – DRAIN CURRENT versus DRAIN to SOURCE VOLTAGE

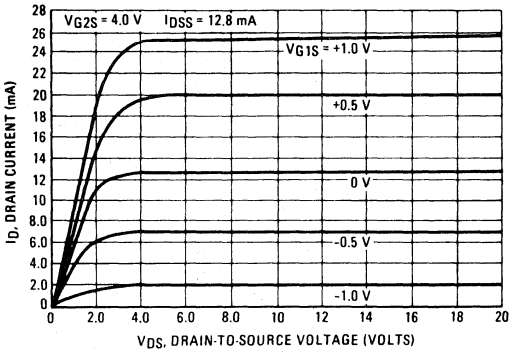


FIGURE 5 – DRAIN CURRENT versus GATE-ONE to SOURCE VOLTAGE

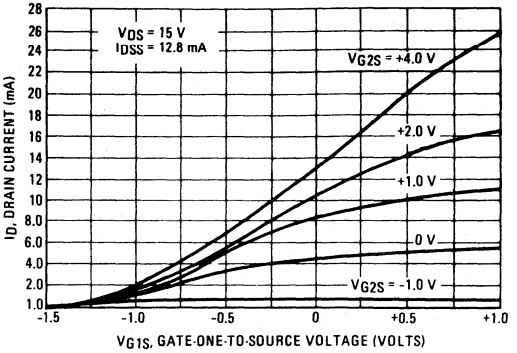


FIGURE 6 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

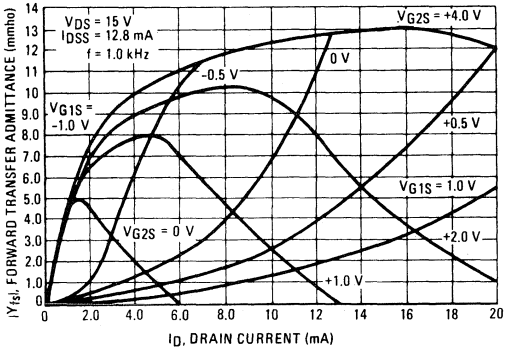


FIGURE 7 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-ONE to SOURCE VOLTAGE

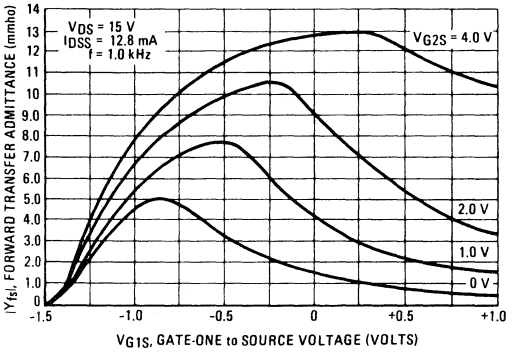


FIGURE 8 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-TWO to SOURCE VOLTAGE

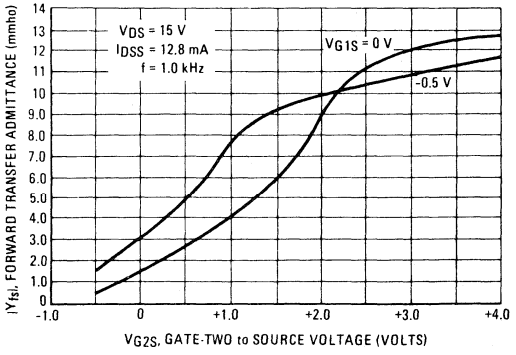
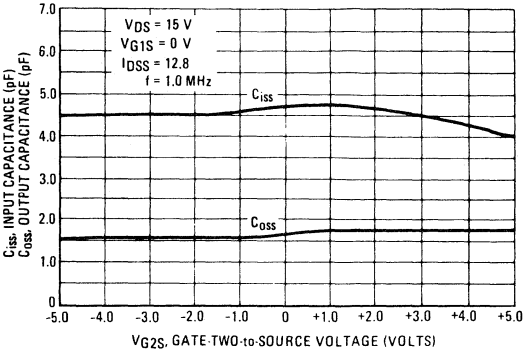


FIGURE 9 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE INPUT AND OUTPUT CAPACITANCE versus GATE-TWO-to-SOURCE VOLTAGE



TYPICAL CHARACTERISTICS

FIGURE 10 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus DRAIN CURRENT

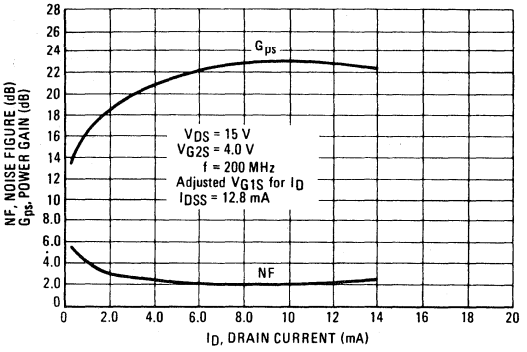


FIGURE 11 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N201

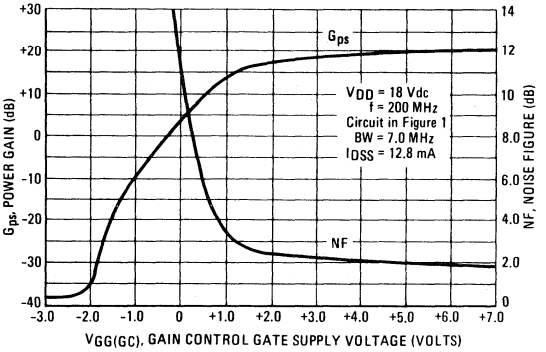


FIGURE 12 – COMMON-SOURCE POWER GAIN versus DRAIN SUPPLY CURRENT – 3N201

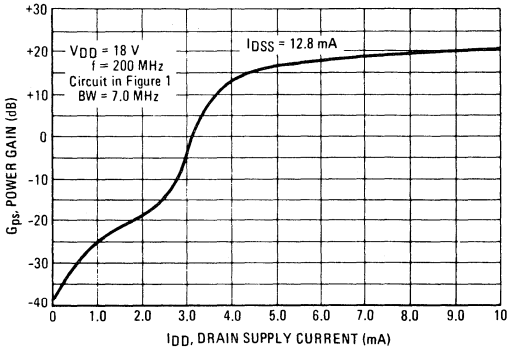


FIGURE 13 – SMALL-SIGNAL COMMON-SOURCE CONVERSION POWER GAIN versus LOCAL OSCILLATOR INPUT VOLTAGE – 3N202

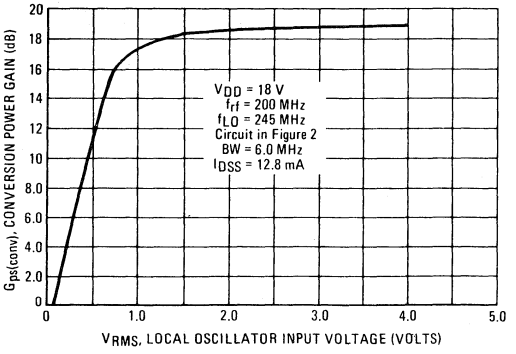
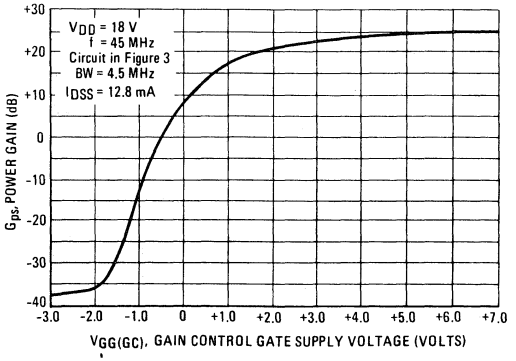


FIGURE 14 – SMALL-SIGNAL COMMON SOURCE INSERTION POWER GAIN versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N203



TYPICAL CHARACTERISTICS

FIGURE 15 – SMALL-SIGNAL GATE ONE FORWARD TRANSFER ADMITTANCE versus FREQUENCY

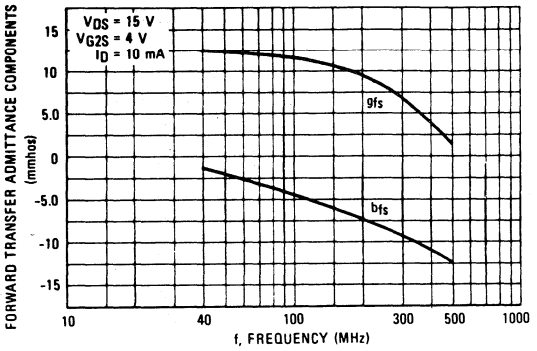


FIGURE 16 – SMALL-SIGNAL GATE ONE INPUT ADMITTANCE versus FREQUENCY

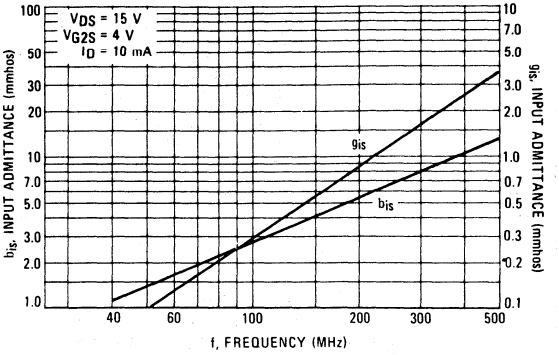
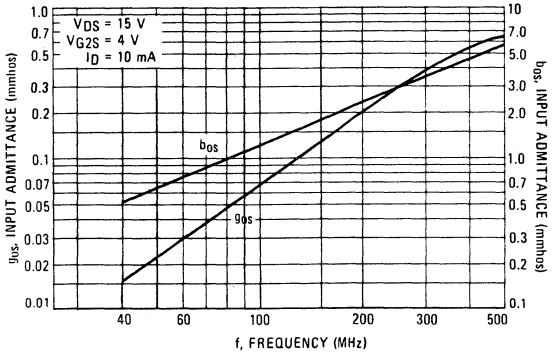
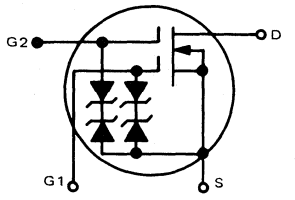


FIGURE 17 – SMALL-SIGNAL GATE ONE OUTPUT ADMITTANCE versus FREQUENCY



3N211
3N212 • 3N213



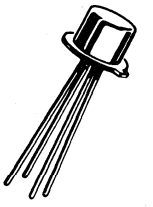
N-CHANNEL

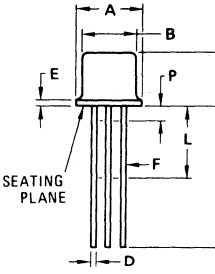
DUAL GATE MOS FIELD-EFFECT TRANSISTORS

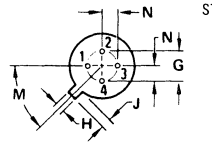
N-CHANNEL DUAL GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTORS

. . . high Y_{fs} depletion mode dual gate transistors designed for VHF amplifier and mixer applications.

- 3N211 – VHF Amplifier/IF Amplifier
  3N212 – VHF Mixer
  3N213 – IF Amplifier
- High Forward Transfer Admittance –
  $|Y_{fs}|$ = 17-40 mmhos – 3N211, 3N212
  = 15-35 mmhos – 3N213
- Low Reverse Transfer Capacitance –
  C_{rss} = 0.03 pF (Max)
- Diode Protected Gates







STYLE 9
PIN 1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE, SUBSTRATE AND CASE

***MAXIMUM RATINGS**

Rating	Symbol	3N211 3N212	3N213	Unit
Drain – Source Voltage	V_{DS}	27	35	Vdc
Drain – Gate Voltage	V_{DG1}	35	40	Vdc
	V_{DG2}	35	40	Vdc
Gate Current	I_{G1}	±10		mAdc
	I_{G2}	±10		mAdc
Drain Current – Continuous	I_D	50		mAdc
Total Power Dissipation @ T_A = 25°C	P_D	360		mW
Derate above 25°C		2.4		mW/°C
Total Power Dissipation @ T_C = 25°C	P_D	1.2		Watt
Derate above 25°C		8.0		mW/°C
Storage Channel Temperature Range	T_{stg}	-65 to +200		°C
Junction Temperature Range	T_J	-65 to +175		°C
Lead Temperature, 1/16" From Seated Surface for 10 Seconds	T_L	300		°C

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Instantaneous Drain-Source Breakdown Voltage(1) (I_D = 10 μAdc, V_{G1S} = V_{G2S} = -4.0 Vdc)	3N211, 212 3N213	$V_{(BR)DSX}$	27 35	–	Vdc
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_{G1S} = V_{G2S} = -4.0 Vdc)	3N211, 212 3N213	$V_{(BR)DSX}$	25 30	–	Vdc
Gate 1 – Source Breakdown Voltage (2) (I_{G1} = ±10 mAdc, V_{G2S} = V_{DS} = 0)		$V_{(BR)G1SO}$	±6.0	–	Vdc
Gate 2 – Source Breakdown Voltage(2) (I_{G2} = ±10 mAdc, V_{G1S} = V_{DS} = 0)		$V_{(BR)G2SO}$	±6.0	–	Vdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 20 μAdc)	3N211, 213 3N212	$V_{G1S(off)}$	-0.5 -0.5	-5.5 -4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 20 μAdc)	3N211 3N212, 213	$V_{G2S(off)}$	-0.2 -0.2	-2.5 -4.0	Vdc
Gate 1 Leakage Current (V_{G1S} = ±5.0 Vdc, V_{G2S} = V_{DS} = 0) (V_{G1S} = -5.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)		I_{G1SS}	– –	±10 -10	mAdc μAdc
Gate 2 Leakage Current (V_{G2S} = ±5.0 Vdc, V_{G1S} = V_{DS} = 0) (V_{G2S} = -5.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)		I_{G2SS}	– –	±10 -10	nAdc μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current(3) (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc)		I_{DSS}	6.0	40	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance(4) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, V_{G1S} = 0, f = 1.0 kHz)	3N211, 212 3N213	$\|Y_{fs}\|$	17 15	40 35	mmhos
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)		C_{rss}	0.005	0.05	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211, 13		NF	– –	3.5 4.0	dB
Common Source Power Gain (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N213 (V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 3) 3N212		G_{ps} G_c (6)	24 29 27 21	35 37 35 28	dB
Bandwidth (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 3) 3N212 (V_{DD} = 24 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 2) 3N211, 213		BW	5.0 4.0 3.5	12 7.0 6.0	MHz
Gain Control Gate-Supply Voltage(5) (V_{DD} = 18 Vdc, ΔG_{ps} = -30 dB, f = 200 MHz) (Figure 1) 3N211 (V_{DD} = 24 Vdc, ΔG_{ps} = -30 dB, f = 45 MHz) (Figure 2) 2N211, 213		$V_{GG(GC)}$	– –	-2.0 ±1.0	Vdc

* Indicates JEDEC Registered Data.

(1) Measured after five seconds of applied voltage

(2) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.

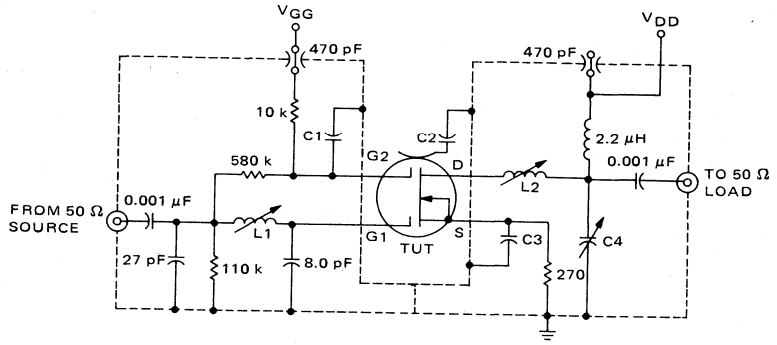
(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

(4) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate 1 with gate 2 at ac ground.

(5) ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 Volts (3N211) and V_{GG} = 6.0 Volts (3N213).

(6) Power Gain Conversion. Amplitude at input from local oscillator is adjusted for maximum G_c.

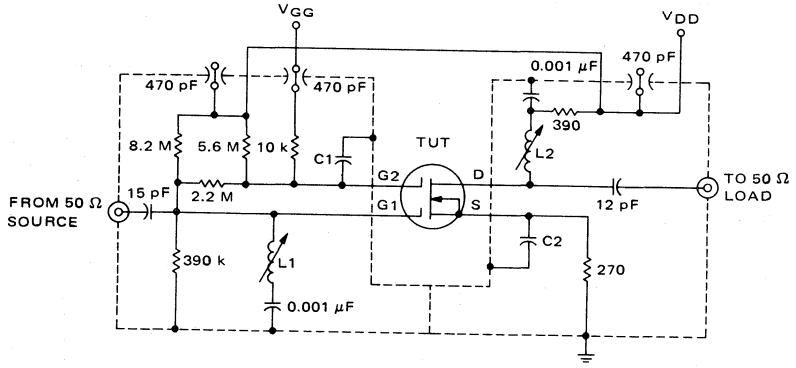
FIGURE 1 – 200 MHz POWER GAIN, GAIN CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N211*



C1, C2 & C3: Leadless disc ceramic, 0.001 μF
C4: ARCO 462, 5-80 pF, or equivalent

L1: 3 Turns #18, 3/16" diameter aluminum slug
L2: 8 Turns #20, 3/16" diameter aluminum slug

FIGURE 2 – 45-MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT FOR 3N211 AND 3N213*

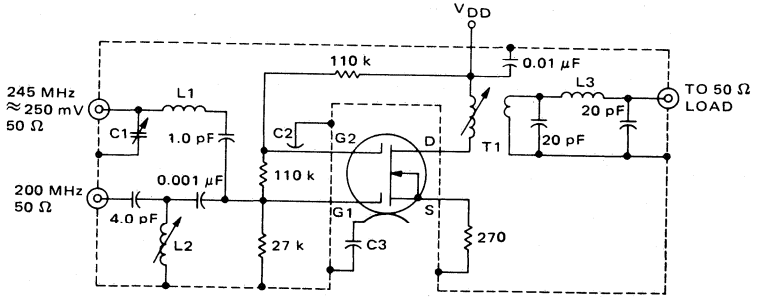


C1: Leadless disc ceramic, 0.001 μF
C2: Leadless disc ceramic, 0.01 μF

L1: 8 Turns #28, 5/32" diameter form, type "J" slug
L2: 9 Turns #28, 5/32" diameter form, type "J" slug

*JEDEC registered data

FIGURE 3 – 200-MHz-to-45-MHz CIRCUIT FOR CONVERSION POWER GAIN FOR 3N212*



L1: 7 Turns #34, 1/4" diameter aluminum slug
L2: 5-1/2 Turns #20, 1/4" diameter aluminum slug
L3: 7 Turns #24, 1/4" diameter air core

C1: Arco type 462, 5-80 pF
C2: 0.001 μF leadless disc
C3: 0.01 μF leadless disc

T1: Pri: 25 Turns #30, close wound on 1/4" diameter form, type "J" slug
Sec: 4 Turns #30, centered over primary

TYPICAL CHARACTERISTICS

FIGURE 4 – DRAIN CURRENT versus DRAIN TO SOURCE VOLTAGE

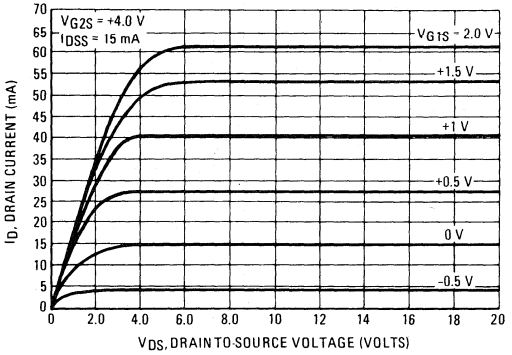
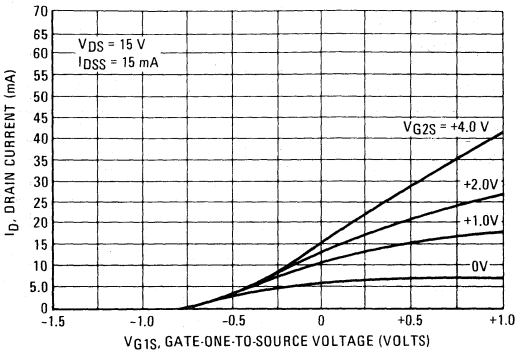


FIGURE 5 – DRAIN CURRENT versus GATE ONE TO SOURCE VOLTAGE



SMALL-SIGNAL COMMON-SOURCE PARAMETER

FIGURE 6 – FORWARD TRANSFER ADMITTANCE versus GATE-TWO TO SOURCE VOLTAGE

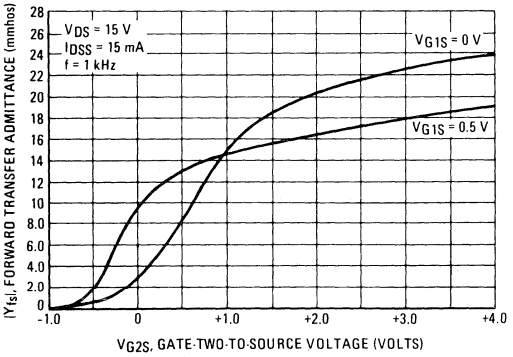


FIGURE 7 – FORWARD TRANSFER ADMITTANCE versus GATE-ONE TO SOURCE VOLTAGE

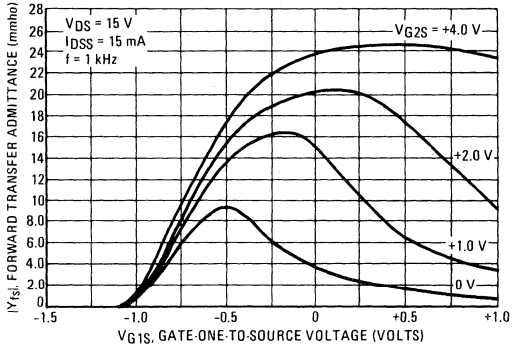


FIGURE 8 – FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

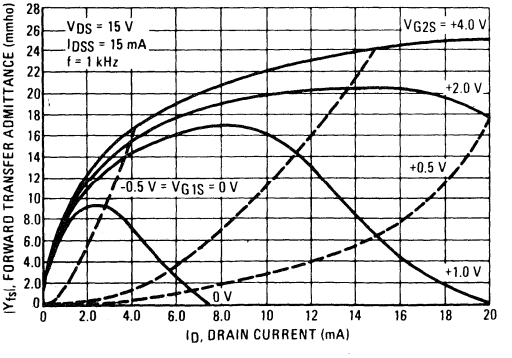
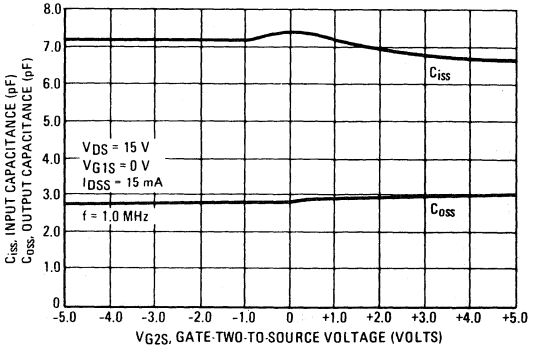


FIGURE 9 – INPUT AND OUTPUT CAPACITANCE versus GATE-TWO TO SOURCE VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – SMALL-SIGNAL GATE-ONE INPUT ADMITTANCE versus FREQUENCY

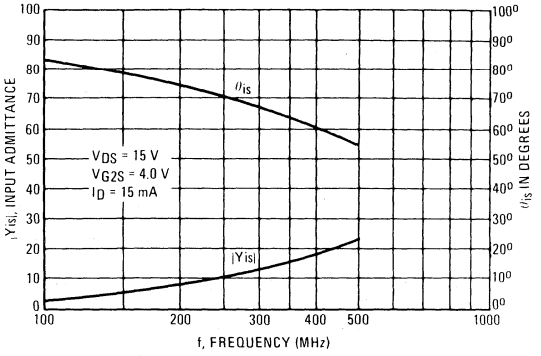


FIGURE 11 – SMALL-SIGNAL FORWARD TRANSFER ADMITTANCE versus FREQUENCY

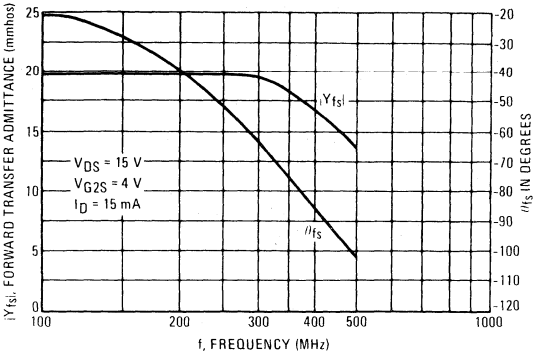


FIGURE 12 – SMALL-SIGNAL GATE-ONE REVERSE TRANSFER ADMITTANCE versus FREQUENCY

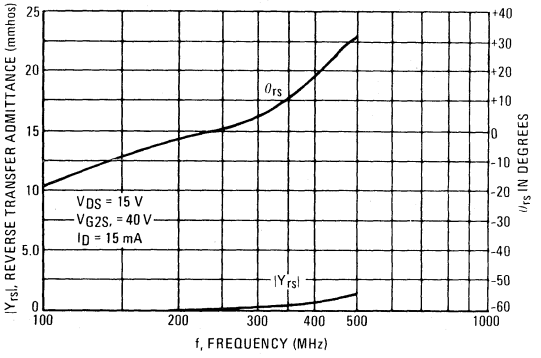


FIGURE 13 – SMALL-SIGNAL GATE-ONE OUTPUT ADMITTANCE versus FREQUENCY

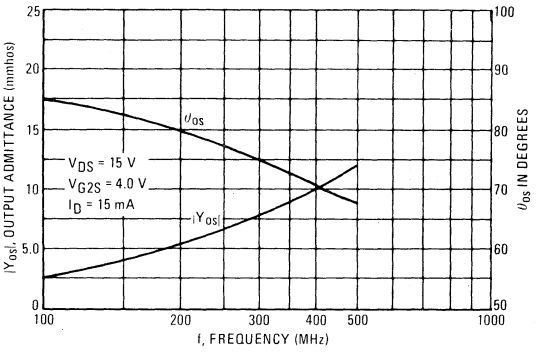


FIGURE 14 – RELATIVE SMALL-SIGNAL POWER GAIN versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211

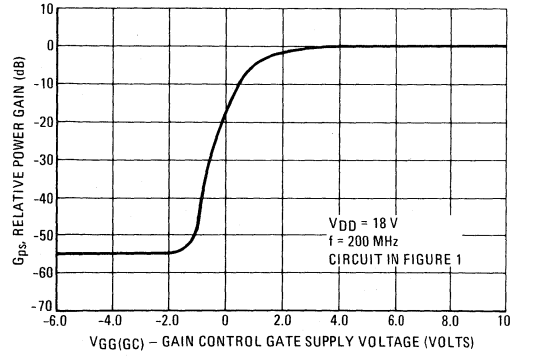
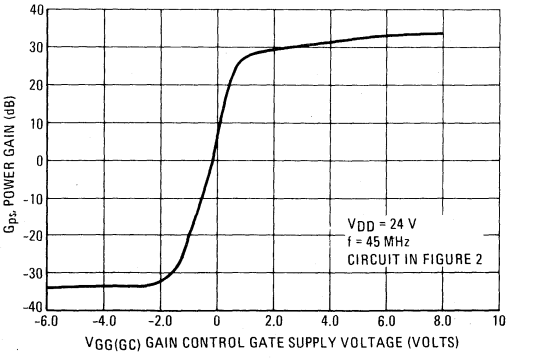


FIGURE 15 – SMALL-SIGNAL COMMON-SOURCE INSERTION POWER GAIN versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211, 213



TYPICAL CHARACTERISTICS (continued)

FIGURE 16 – COMMON SOURCE SPOT NOISE FIGURE versus GAIN CONTROL GATE SUPPLY VOLTAGE 3N211

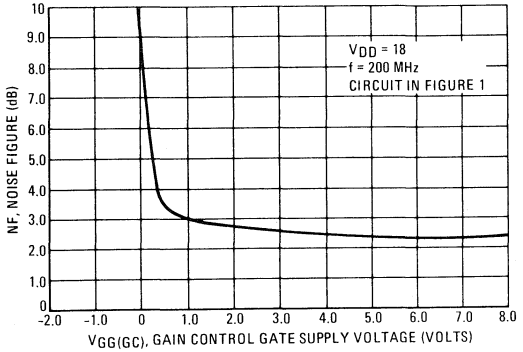
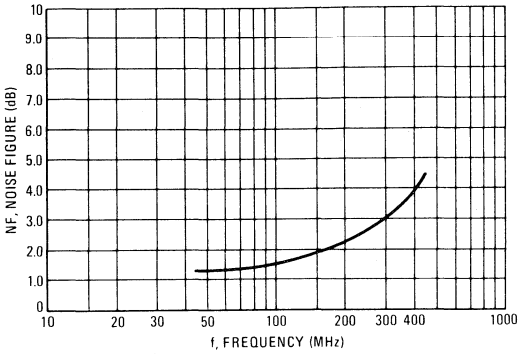


FIGURE 17 – OPTIMUM SPOT NOISE FIGURE versus FREQUENCY



THYRISTORS and TRIGGER DEVICES

Silicon Controlled Rectifiers		V_{DRM} Max. A	$I_{T(RMS)}$ Max. A	I_{TSM} Max. A	I_{GT} Max. mA	V_{GT} Max. V	I_H Max. mA	Package	Page
MCR100 Series (3-8)	General Line Powered Applications	100-600	0,8	6	0.2	0.8	5	TO-92	6-9
MCR106 (1-4, 6, 8)	General Temp. Light, Speed control	30-600	4	25	0.2	1	5	77	6-11
2N4441, 42, 43, 44	Phase Control Applications	50-600	8	80	3	1.5	40	90	6-15
2N5060-5064	General Relay, Lamp, Motor Applications	30-200	0.8	6	0.2	0.8	5	TO-92	6-23
2N6236-6241	General Temp. Light, Speed control	30-600	4	25	0.2	1	5	77	6-35
2N6394-6399 (MCR220)	General Half Wave Control	50-800	12	100	30	1-5	40	TO-220	6-45
2N6400-6405 (MCR221)	General Half Wave Control	50-800	16	160	30	1.5	40	TO-220	6-49

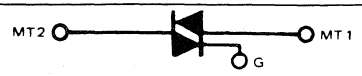
Triacs		V_{DRM} Max. V	$I_{T(RMS)}$ Max. A	I_{GT} (Max.) mA				V_{GT} (Max.) V				I_H Max. mA	Package	Page
				MT2− G−	MT2+ G−	MT2− G+	MT2+ G+	MT2− G−	MT2+ G−	MT2− G+	MT2+ G+			
BT162	For ZVS Applications	400-600	12	40	40	–	–	1.5	1.5	–	–	30	TO-220	6-1
MAC15, A	General Full Wave Control	200-800	15	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-5
2N6068,A,B-6075,	Sensitive Gate Triggering	25-600	4	3	3	5	3	2.5	2.5	2.5	2.5	15	77	6-31
2N6342-49 A, B	General Full Wave Control	200-800	8	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-37
2N6342A-49A	General Full Wave Control	200-800	12	50	75	75	50	2	2.5	2.5	2	40	TO-220	6-41

Unijunction Transistors (UJT)		$V_{B_2B_1}$ Max. V	η ($V_{B_2B_1}$ = 10 V)		I_P ($V_{B_2B_1}$ = 25 V) Max. μA	$I_{EB_{2O}}$ (V_{B_2E} = 30 V) Max. μA	I_V ($V_{B_2B_1}$ = 20 V, R_{B_2} = 100 Ω) Min. mA	Package	Page
			Min.	Max.					
2N2646	Timing and Thyristor Trigger	35	0.56	0.75	5	12	4	22A	6-13
2N2647		35	0.68	0.82	2	0.2	8	22A	6-13
2N4870	Timing and Thyristor Trigger	35	0.56	0.75	5	1	2	TO-92	6-19
2N4871		35	0.7	0.85	5	1	4	TO-92	6-19

Programmable Unijunction Transistors (PUT)		V_{AK} Max. V	I_T Max. mA	I_P V_S = 10 V R_G = 10K μA Max.	I_V V_S = 10 V R_G = 10K Ω μA Max.	Package	Page
2N6027	Oscillator, Timing and Thyristor Trigger	±40	200	5	70	TO-92	6-27
2N6028		±40	200	1	25	TO-92	6-27

6

BT162-400
BT162-600



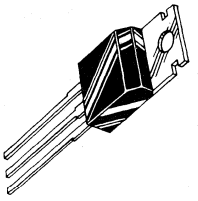
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for consumer and industrial applications of power control using the zero voltage switching technique, such as heater controls, hot plate controls and static switches. These devices are characterized in the second and third quadrants (negative pulse triggering) and permit the design of most circuits entirely from the information presented.

- Low gate trigger current
- Low latching current
- All diffused and glass passivated junctions for greater parameter uniformity and stability
- Small, rugged, Thermowatt▲ construction for low thermal resistance, high heat dissipation and durability
- 8 Amp. devices available as BT158-400, BT158-600.

TRIACS
(THYRISTORS)
12 AMPERES RMS

400-600 VOLTS

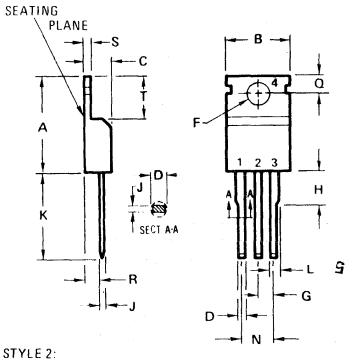


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = −40 to +110 °C) Half Sine Wave 50 to 60 Hz, Gate Open BT162-400 BT162-600	V_{DRM}	400 600	Volts
Non Repetitive Peak Off-State Voltage[1] (T_J = −40 to +110 °C) t ≤ 10 ms, Gate Open BT162-400 BT162-600	V_{DSM}	500 700	Volts
On-State Current RMS (T_C = +80 °C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95 °C)	$I_{T(RMS)}$	12.0 6.0	Amp
Peak Surge Current (One Full Cycle, T_C = 80 °C) 60 Hz 50 Hz preceded and followed by rated current	I_{TSM}	120 110	Amp
Rate of Rise of ON-State Current (Non Repetitive), Gate Open	$\frac{dI_T}{dt}$	10	Amp/μs
Circuit Fusing Considerations (T_J = −40 to +110 °C, t = 1.0 to 10 ms)	I^2t	40	A^2s
Peak Gate Voltage	V_{GM}	10	Volts
Peak Gate Current	I_{GM}	2.0	Amp
Peak Gate Power (T_C = +80 °C, Pulse Width = 2,0 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +80 °C, t = 10 ms)	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB

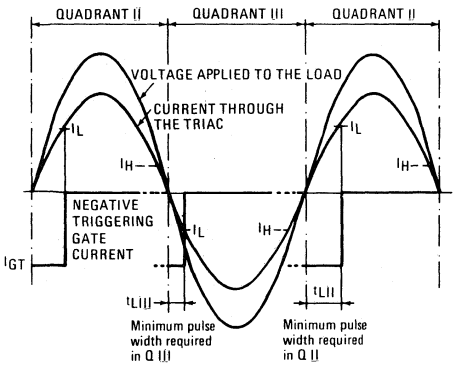
▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25 ° unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C; Gate Open	I_{DRM}			2.0	mA
Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2.0 °/o	V_{TM}		1.3	1.75	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs MT2 (+), G (−) MT2 (−), G (−) MT2 (+), G (−); MT2 (−), G (−), T_C = −40 °C	I_{GT}		 25 20	 40 40 75	mA
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 µs MT2 (+), G (−) MT2 (−), G (−) MT2 (+), G (−); MT2 (−), G (−), T_C = −40 °C Main Terminal Voltage = Rated V_{DRM}, R_L = 10 K, T_J = 110 °C MT2 (+), G (−); MT2 (−), G (−)	V_{GT}	 0.2	 0.9 1.1	 1.5 1.5 2.0	Volts
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open } T_C = 25 °C Initiating Current = 200 mA } T_C = −40 °C	I_H		6.0	30 50	mA
Latching Current Main Terminal Voltage = 12 Vdc; R_L = variable Gate Pulse Width = 20 µs, Duty Cycle ≤ 2 °/o MT2 (+), G (−) } @ I_{GT} = 40 mA MT2 (−), G (−) } MT2 (+), G (−) } @ I_{GT} = 75 mA; T_C = −40 °C MT2 (−), G (−) }	I_L		 30 6.0	 60 40 100 60	mA
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open T_C = 110 °C	dV/dt		100		V/µs

[1] Off-State Voltage up to 800 V may be applied, but triac may switch into the On-State. In that case, the Rate of Rise of On-State current should not exceed its specified maximum rating.

ZERO VOLTAGE SWITCHING MAIN CHARACTERISTICS



RECOMMENDED ZERO VOLTAGE SWITCH INTEGRATED CIRCUITS

Part Nr.	Usage	Package
UAA1004	On-Off Applications, high volume	DIL 8 pin
UAA1006	Proportional Applications; variable duty cycle modulator	DIL 16 pin

See separate Data Sheets for complete information.

FIGURE 1 – RMS CURRENT DERATING

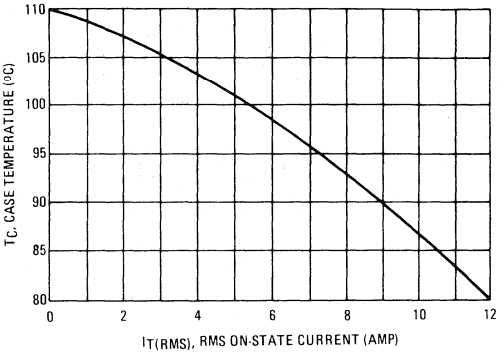


FIGURE 2 – ON-STATE POWER DISSIPATION

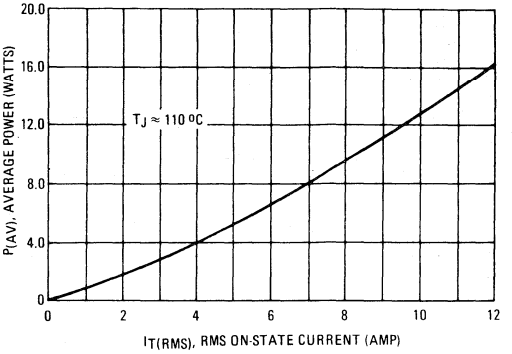


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

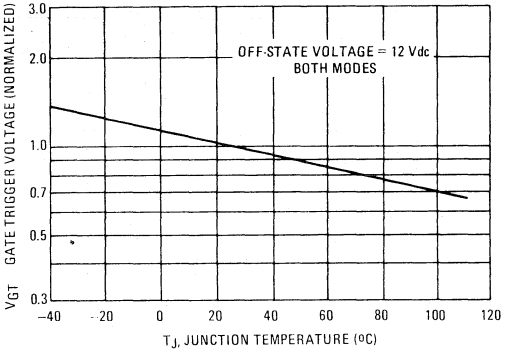


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

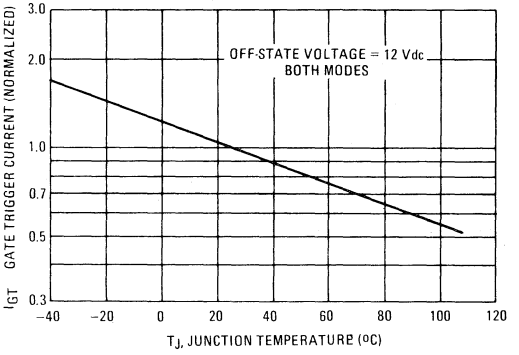


FIGURE 5 – TYPICAL HOLDING CURRENT

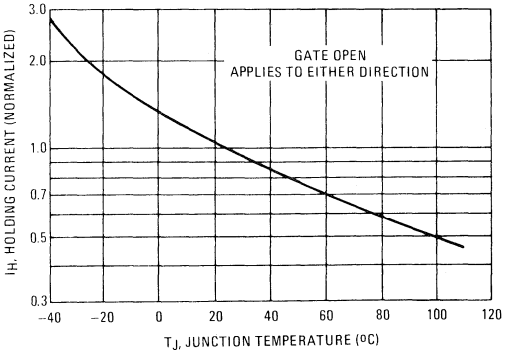


FIGURE 6 – TYPICAL LATCHING CURRENT

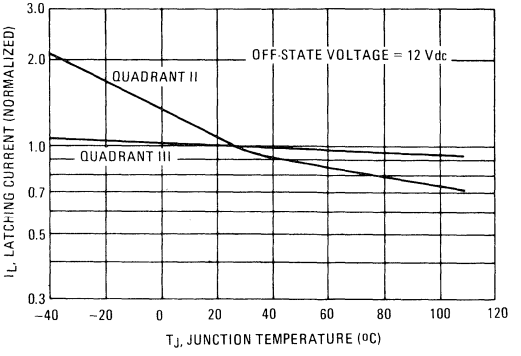


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FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

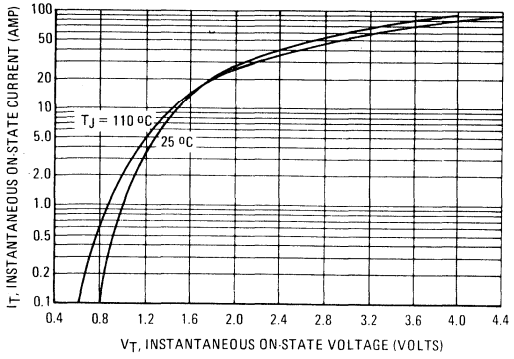


FIGURE 8 – MAXIMUM NON-REPETITIVE SURGE CURRENT

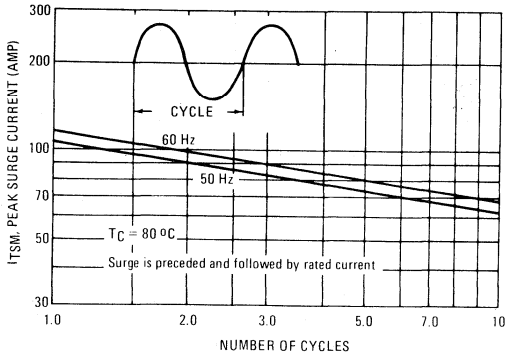
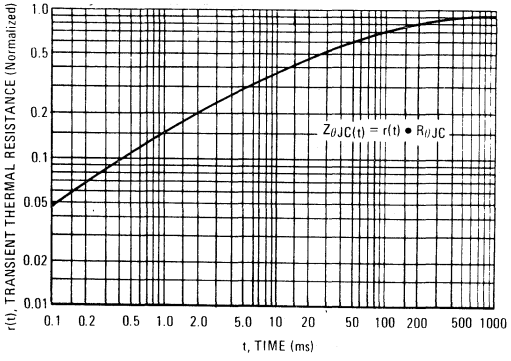


FIGURE 9 – TYPICAL THERMAL RESISTANCE FROM MOUNTING BASE TO HEATSINK

Metal to Metal:	Dry	0,9 °C/W
Metal to Metal:	Lubed	0,3 °C/W
With Insulator:	Dry	Not recommended
With Insulator:	Lubed	1,3 °C/W

These values are available when using the rectangular washer and mica insulator furnished with the kit MK221-2. The recommended mounting torque is 8 Kg. cm.

FIGURE 10 – THERMAL RESPONSE



6

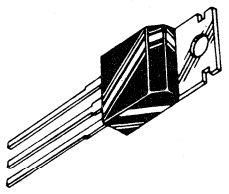
MAC15
MAC15A

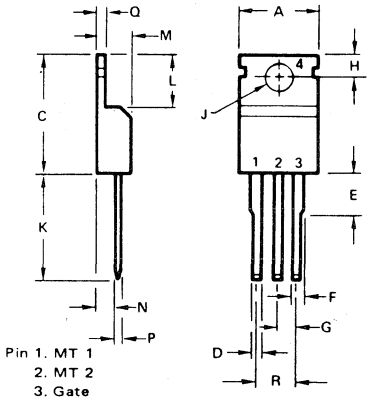
TRIACS
(THYRISTORS)
15 AMPERES RMS
200 – 800 VOLTS

SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (MAC15)
  Four Modes (MAC15A)





All JEDEC dimensions and notes apply

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.380	0.420	9.660	10.66
C	0.560	0.625	14.23	15.87
D	0.020	0.045	0.510	1.140
E		0.250		6.350
F	0.045	0.070	1.140	1.770
G	0.090	0.110	2.290	2.790
H	0.100	0.120	2.540	3.040
J	0.139	0.147	3.531	3.733
K	0.500	0.562	12.70	14.27
L	0.230	0.270	5.850	6.820
M	0.140	0.190	3.560	4.820
N	0.080	0.115	2.040	2.920
P	0.012	0.045	0.310	1.140
Q	0.020	0.055	0.510	1.390
R	0.190	0.210	4.830	5.330

CASE 221-02
TO-220 AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC15-4, MAC15A-4		200	
MAC15-6, MAC15A-6		400	
MAC15-8, MAC15A-8		600	
MAC15-10, MAC15A-10		800	
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	15 12	Amp
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

▲Trademark of Motorola Inc.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 125°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage (Either Direction) I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	1.3	1.6	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GTM}				mA
MT2 (+), G(+) – MAC15, MAC15A		–	–	50	
MT2 (+), G(–) – MAC15A		–	–	75	
MT2 (–), G(–) – MAC15, MAC15A		–	–	50	
MT2 (–), G(+) – MAC15A		–	–	75	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GTM}				Volts
MT2 (+), G(+) – MAC15, MAC15A		–	0.9	2	
MT2 (+), G(–) – MAC15A		–	0.9	2.5	
MT2 (–), G(–) – MAC15, MAC15A		–	1.1	2	
MT2 (–), G(+) – MAC15A		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) – MAC15, MAC15A		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) – MAC15A		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H	–	6	40	mA
Turn-On Time Rated V_{DRM}, I_{TM} = 17 A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	tgt	–	1.5	2	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(C)	–	5	–	V/μs

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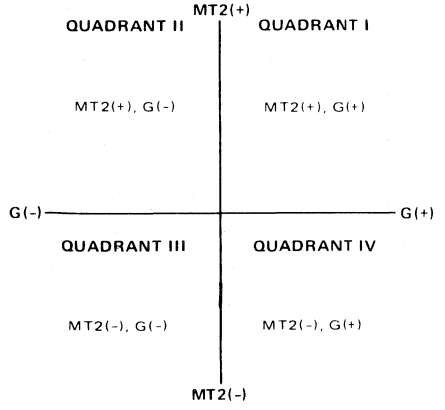
NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6–10 V	7.5–9 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – RMS CURRENT DERATING

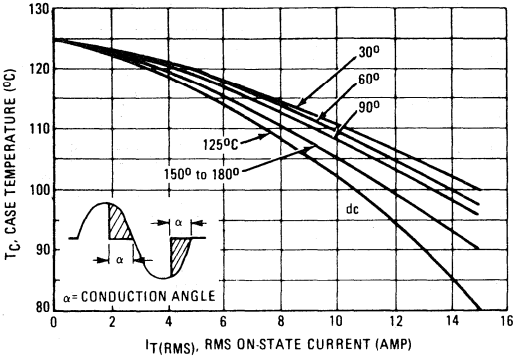


FIGURE 2 – ON-STATE POWER DISSIPATION

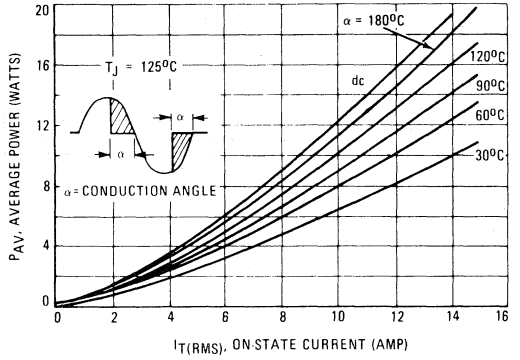


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

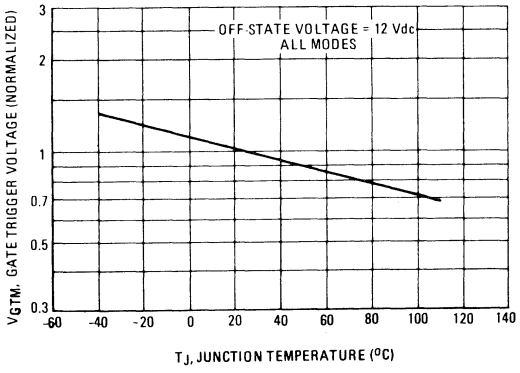


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

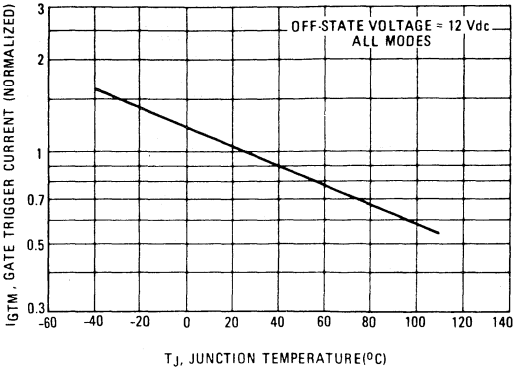


FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

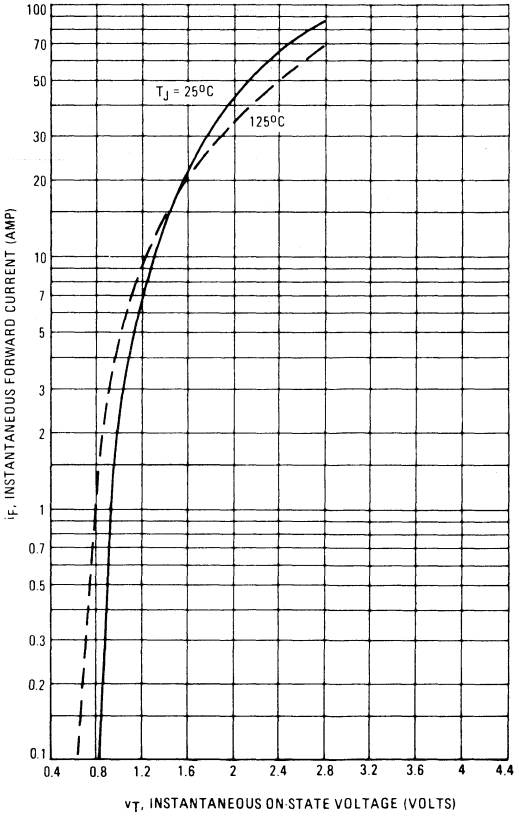


FIGURE 6 – TYPICAL HOLDING CURRENT

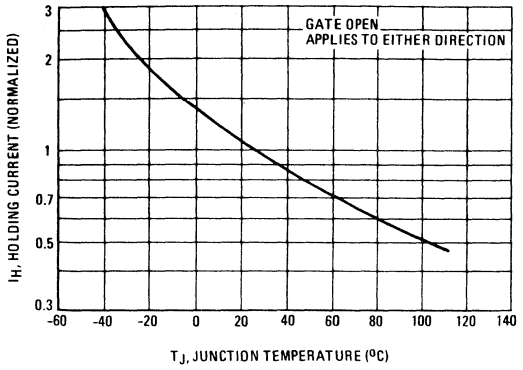


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

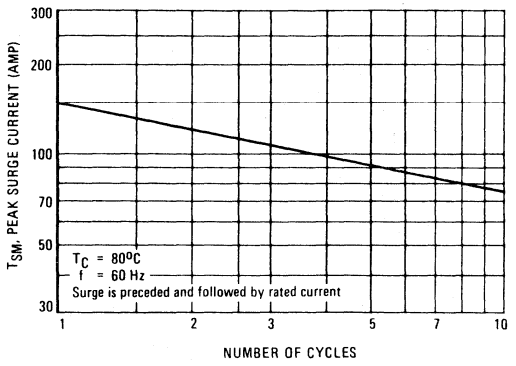
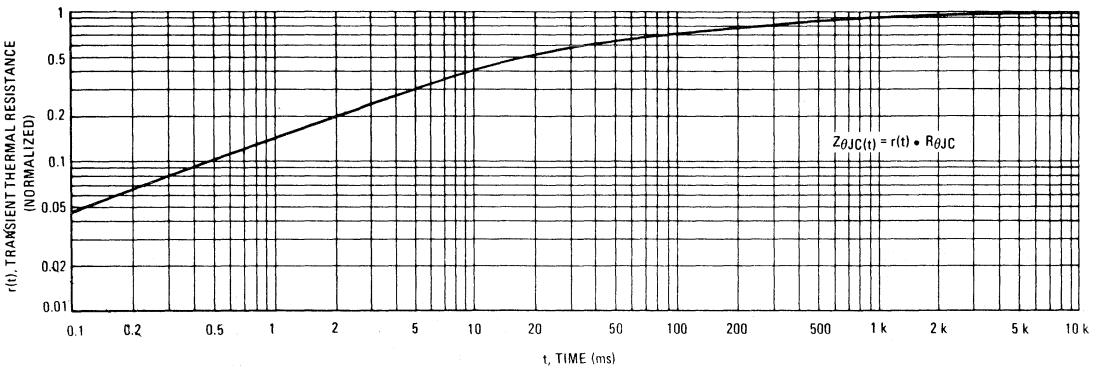
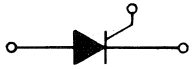


FIGURE 8 – THERMAL RESPONSE





PLASTIC SILICON CONTROLLED RECTIFIERS

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity

MAXIMUM RATINGS

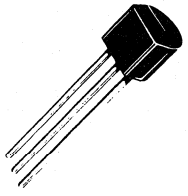
Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage MCR100-3 MCR100-4 MCR100-5 MCR100-6 MCR100-7 MCR100-8	V_{RRM}	 100 200 300 400 500 600	Volts
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power – Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current – Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)		+230	°C

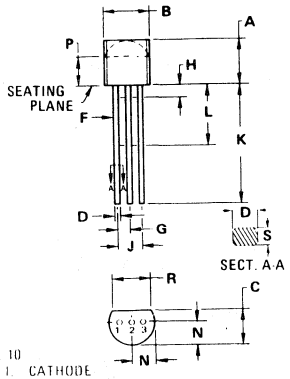
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R θJC	75	°C/W
Thermal Resistance, Junction to Ambient	R θJA	200	°C/W

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 to 600 VOLTS





STYLE 10
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)	MCR100-3	V_{DRM}	100		Volts
	MCR100-4		200		
	MCR100-5		300		
	MCR100-6		400		
	MCR100-7		500		
	MCR100-8		600		
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	--	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1	--	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C		–	10	

NOTE:
1. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
2. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

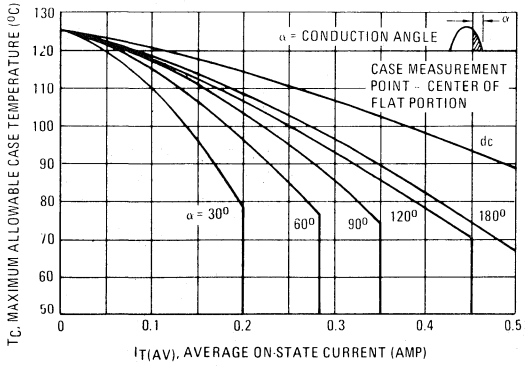
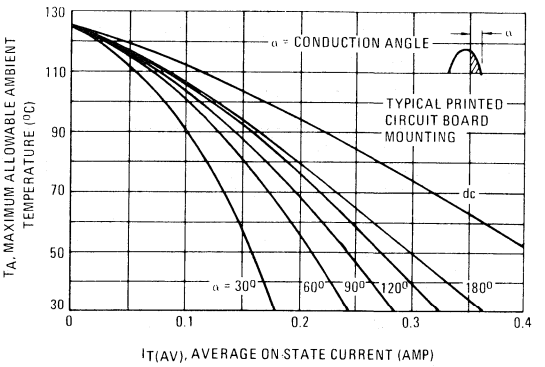


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



MCR106-1 thru MCR106-4
MCR106-6 • MCR106-8

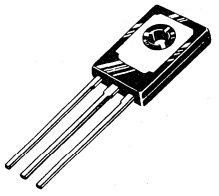
SILICON
CONTROLLED RECTIFIERS

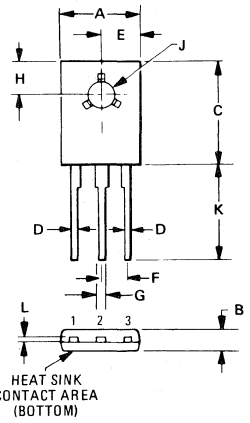
. . . Annular♦ PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Annular♦ Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability.

THYRISTORS

4.0 AMPERES RMS
30 thru 600 VOLTS





Pin 1. Cathode
2. Anode
3. Gate

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.860	8.380	0.270	0.330
B	1.770	3.300	0.070	0.130
C	9.910	11.430	0.390	0.450
D	0.508	0.660	0.020	0.026
E	3.810 NOM		0.150 NOM	
F	2.290 TP		0.090 TP	
G	0.635	0.889	0.025	0.035
H	3.300	4.450	0.130	0.175
J	2.910	3.000	0.115	0.118
K	15.110	16.650	0.595	0.655
L	0.381	0.635	0.015	0.025

CASE 77-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) MCR106-1	V_{RRM}	30	Volts
-2		60	
-3		100	
-4		200	
-6		400	
-8		600	
RMS Forward Current (All Conduction Angles)	$I_{T(RMS)}$	4.0	Amp
Average Forward Current $T_C = 93^oC$	$I_{T(AV)}$	2.55	Amp
$T_A = 30^oC$		0.68	
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, $T_J = -40$ to $+110^oC$)	I_{TSM}	25	Amp
Circuit Fusing Considerations ($T_J = -40$ to $+110^oC$, t = 1.0 to 8.3 ms)	I^2t	2.6	A^2s
Peak Gate Power	P_{GM}	0.5	Watt
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6.0	Volts
Operating Junction Temperature Range	T_J	-40 to +110	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC
Mounting Torque (Note 2)	—	6.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$

♦Annual Semiconductors Patented by Motorola Inc.

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C, Note 1)	V_{DRM}				Volts
MCR106-1		30	–	–	
-2		60	–	–	
-3		100	–	–	
-4		200	–	–	
-6		400	–	–	
-8		600	–	–	
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	–	–	200	μA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	–	–	200	μA
Forward "On" Voltage (I_{TM} = 4.0 A Peak)	V_{TM}	–	–	2.0	Volts
Gate Trigger Current (Continuous dc)	I_{GT}				μA
(V_{AK} = 7.0 Vdc, R_L = 100 ohms)		–	–	200	
(V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = -40°C)		–	–	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 7.0 Vdc, T_C = 25°C)	I_H	–	–	5.0	mA
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	–	10	–	V/μs

NOTES:

1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

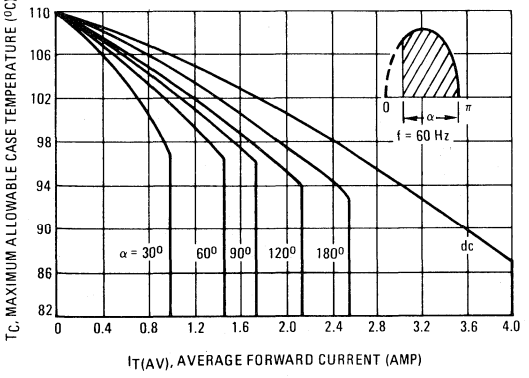
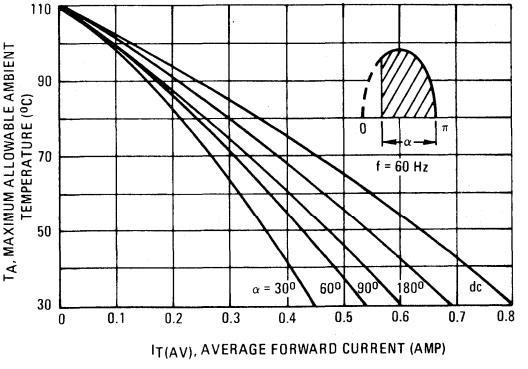


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



2N2646
2N2647

SILICON ANNULAR♦ PN UNIJUNCTION TRANSISTORS

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits. These devices feature:

- Low Peak Point Current – 2.0 μA (Max)
- Low Emitter Reverse Current – 200 nA (Max)
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTORS

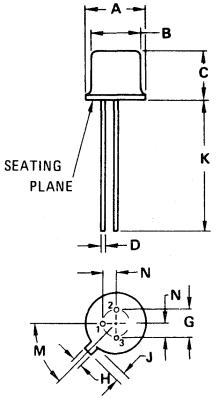
*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_E	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

(2) Capacitor discharge – 10 μF or less, 30 volts or less.



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A

♦Annular Semiconductors Patented by Motorola Inc.

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N2646	η	0.56	–	0.75	–
	2N2647		0.68	–	0.82	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		r_{BB}	4.7	7.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -55°C to +125°C)		α_{rBB}	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646	I_{EB2O}	–	0.005	12	μA
	2N2647		–	0.005	0.2	
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646	I_P	–	1.0	5.0	μA
	2N2647		–	1.0	2.0	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N2646	I_V	4.0	6.0	–	mA
	2N2647		8.0	10	18	
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646	V_{OB1}	3.0	5.0	–	Volts
	2N2647		6.0	7.0	–	

*Indicates JEDEC Registered Data.

Notes:

(1) Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_F}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ⩽ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

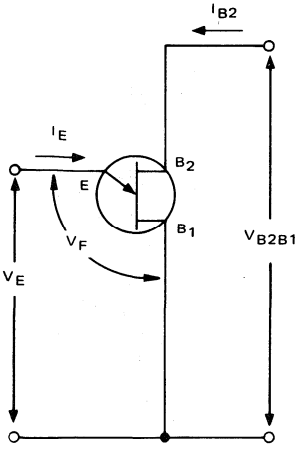


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

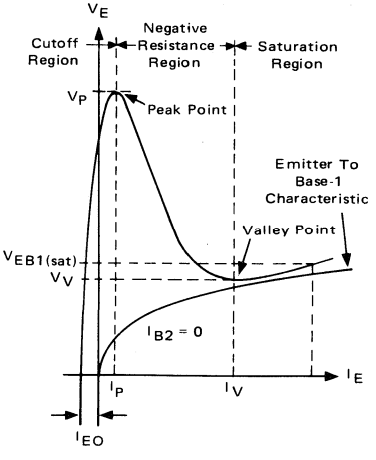
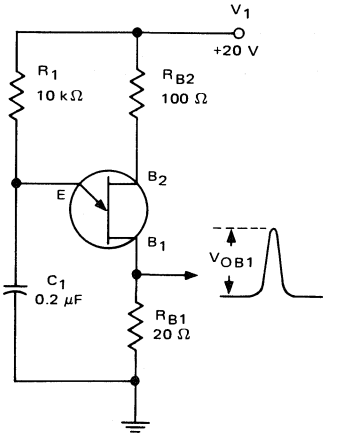
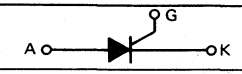


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



2N4441 thru 2N4444



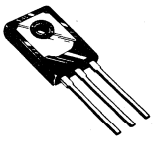
PLASTIC THYRISTORS

. . . designed for high-volume consumer phase-control applications such as motor speed, temperature, and light controls and for switching applications in ignition and starting systems, voltage regulators, vending machines, and lamp drivers requiring:

- Small, Rugged, Thermopad ▲ Construction – for Low Thermal Resistance, High Heat Dissipation, and Durability.
- Practical Level Triggering and Holding Characteristics @ 25°C
  I_{GT} = 7.0 mA (Typ)
  I_H = 6.0 mA (Typ)
- Low "On" Voltage – V_{TM} = 1.0 Volt (Typ) @ 5.0 Amp @ 25°C
- High Surge Current Rating – I_{TSM} = 80 Amp

PLASTIC SILICON CONTROLLED RECTIFIERS

8.0 AMPERES RMS
50 thru 600 VOLTS



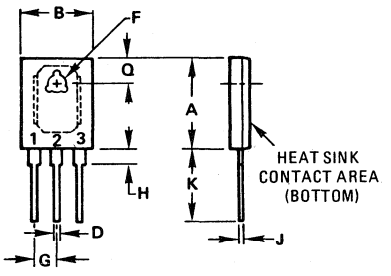
MAXIMUM RATING (T_J = 100°C unless otherwise noted.)

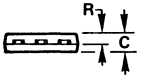
Rating	Symbol	Value	Unit
*Repetitive Peak Reverse Blocking Voltage (Note 1) 2N4441	V_{RRM}	50	Volts
2N4442		200	
2N4443		400	
2N4444		600	
*Non-Repetitive Peak Reverse Blocking Voltage (t = 5.0 ms (max) duration) 2N4441	V_{RSM}	75	Volts
2N4442		300	
2N4443		500	
2N4444		700	
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	8.0	Amp
Average On-State Current, T_C = 73°C	$I_{T(AV)}$	5.1	Amp
*Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz preceded and followed by rated current and voltage)	I_{TSM}	80	Amp
Circuit Fusing Considerations (T_J = −40 to +100°C; t = 1.0 to 8.3 ms)	I^2t	25	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 screw) (Note 2)	–	8.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	–	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	–	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.95	16.71	0.628	0.658
B	12.45	13.21	0.490	0.520
C	3.05	3.81	0.120	0.150
D	1.09	1.25	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	–	3.18	–	0.125
J	0.76	0.86	0.030	0.034
K	14.99	16.51	0.590	0.650
Q	4.50	5.00	0.177	0.197
R	1.91	2.16	0.075	0.085

CASE 90-04

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 100°C) Note 1 2N4441	V_{DRM}	50	–	–	Volts
2N4442		200	–	–	
2N4443		400	–	–	
2N4444		600	–	–	
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 100°C, gate open)	I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (Rated V_{DRM}, T_J = 100°C, gate open)	I_{RRM}	–	–	2.0	mA
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	I_{GT}				mA
T_C = 25°C		–	7.0	30	
* T_C = -40°C				60	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
T_C = 25°C		–	0.75	1.5	
* (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms) T_C = -40°C		–	–	2.5	
* (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms) T_J = 100°C		0.2	–	–	
Peak On-State Voltage (Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}				Volts
(I_{TM} = 5.0 A peak)		–	1.0	1.5	
* (I_{TM} = 15.7 A peak)		–	–	2.0	
Holding Current (Anode Voltage = 7.0 Vdc, gate open)	I_H				mA
T_C = 25°C		–	6.0	40	
* T_C = -40°C		–	–	70	
Gate Controlled Turn-On Time (I_{TM} = 5.0 A, I_{GT} = 20 mA)	t_{gt}	–	1.0	–	μs
Circuit Commutated Turn-Off Time (I_{TM} = 5.0 A, I_R = 5.0 A)	t_q	–	15	–	μs
(I_{TM} = 5.0 A, I_R = 5.0 A, T_J = 100°C)		–	20	–	
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, T_J = 100°C, Gate Open)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data

Note 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

Note 2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C.

FIGURE 1 – MAXIMUM FORWARD VOLTAGE

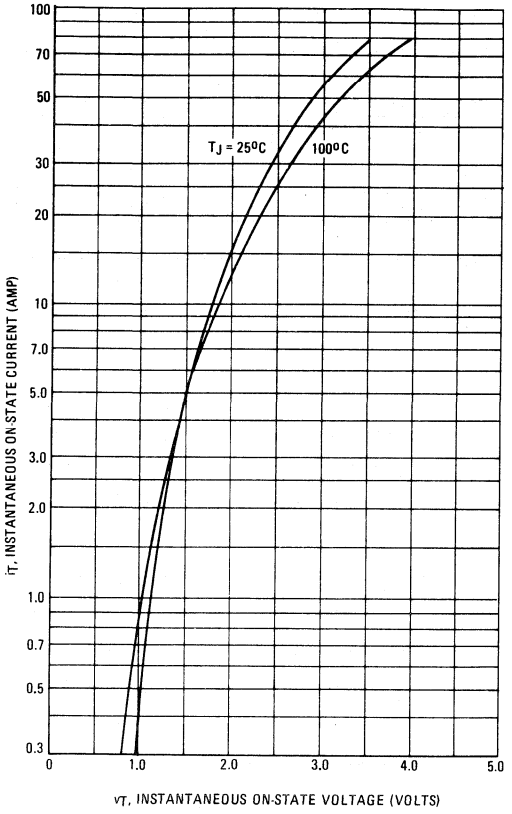


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

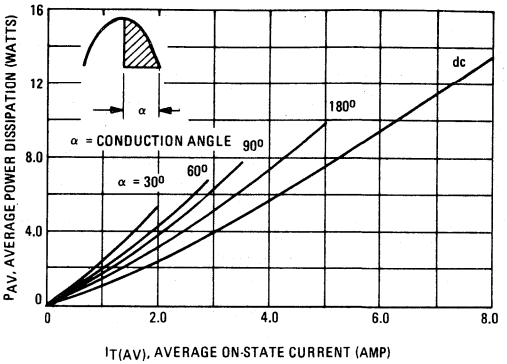


FIGURE 3 – AVERAGE CURRENT DERATING

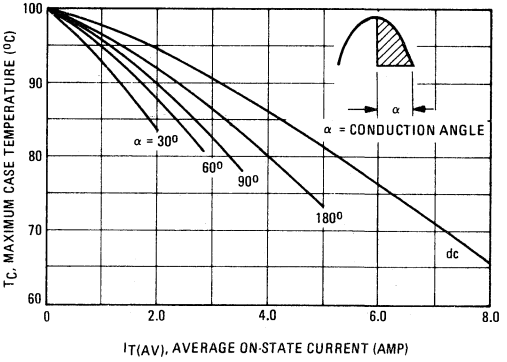


FIGURE 4 – THERMAL RESPONSE

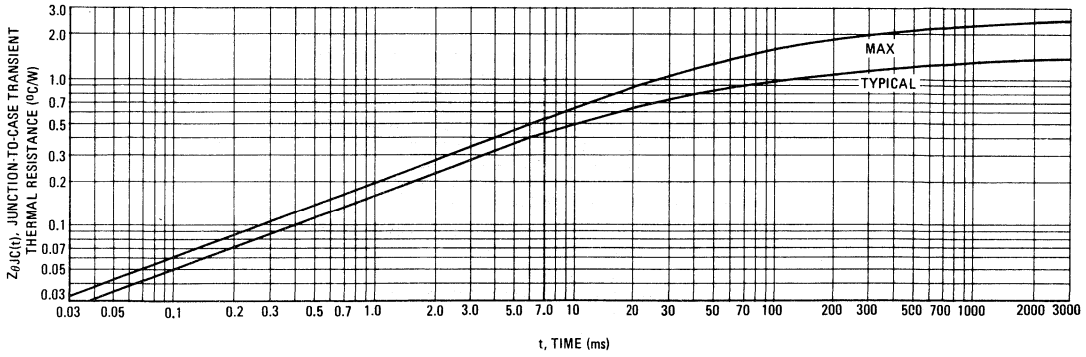


FIGURE 5 – MAXIMUM NON-REPETITIVE SURGE CURRENT

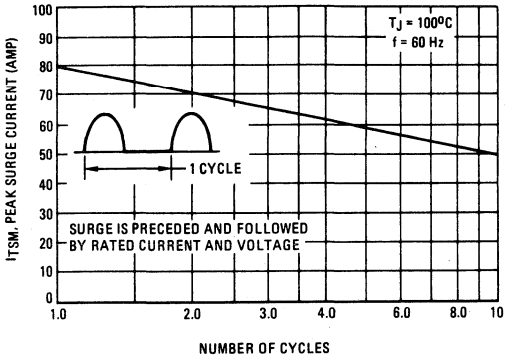


FIGURE 6 – TYPICAL HOLDING CURRENT

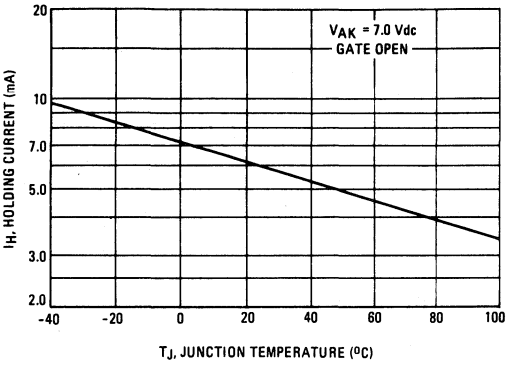


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

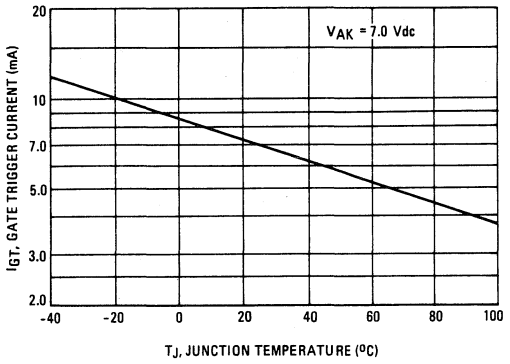
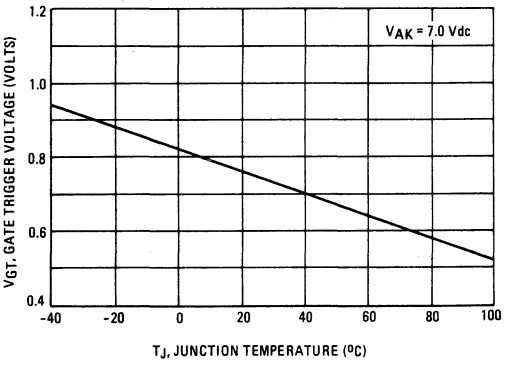


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE



SELECTED THYRISTOR-TRIGGER APPLICATION NOTES

AN-240 —SCR Power Control Fundamentals
AN-290B —Mounting Procedure for, and Thermal Aspects of, Thermopad ▲ Plastic Power Devices
AN-295 —Suppressing RFI in Thyristor Circuits
AN-422 —Testers for Thyristors and Trigger Diodes
AN-453 —Zero Point Switching Techniques

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

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2N4870
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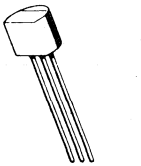


CASE 29
(TO-92)

PN unijunction transistors designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage†	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty cycle ≦ 1%, PRR = 10 PPS (see Figure 5).
†Based upon power dissipation at T_A = 25°C.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

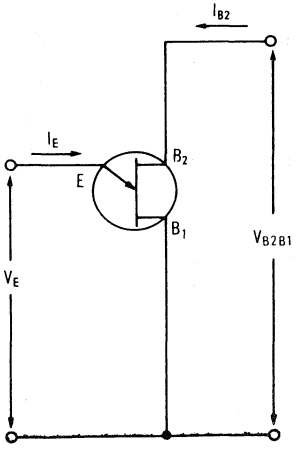
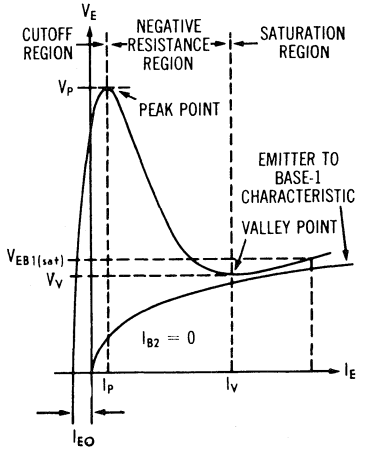


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V)	2N4870 2N4871	4, 7	η*	0.56 0.70	- -	0.75 0.85	-
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		10, 11	R_{BB}	4.0	6.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)		11	αR_{BB}	0.10	-	0.90	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$**	-	2.5	-	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	-	15	-	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		6	I_{EB2O}	-	0.005	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)		8, 9	I_P	-	1.0	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4870 2N4871	12, 13	I_V**	2.0 4.0	5.0 7.0	- -	mA
Base-One Peak Pulse Voltage	2N4870 2N4871	3, 16	V_{OB1}	3.0 5.0	6.0 8.0	- -	Volts

* η Intrinsic standoff ratio, is defined in terms of peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is approximately 0.49 volt at 25° C @ I_F = 10 μA and decreases with temperature at approximately 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator, the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 μs, duty cycle ≦ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 — V_{OB1} TEST CIRCUIT

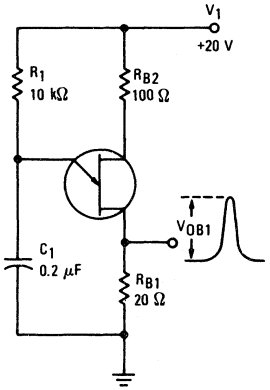
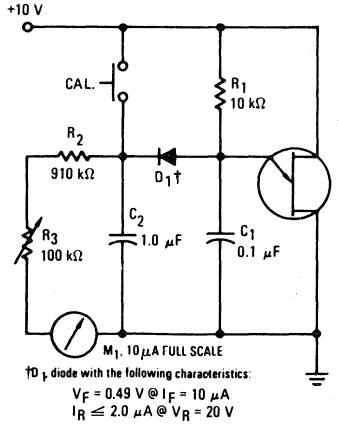
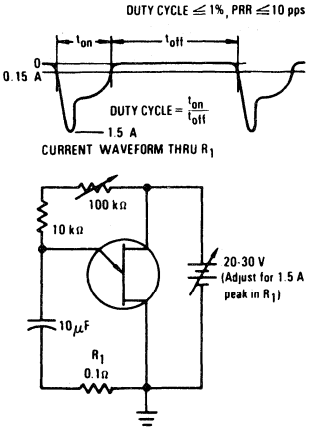


FIGURE 4 — η TEST CIRCUIT



†D_1 diode with the following characteristics:
V_F = 0.49 V @ I_F = 10 μA
I_R ≦ 2.0 μA @ V_R = 20 V

FIGURE 5 — PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 6 — EMITTER REVERSE CURRENT

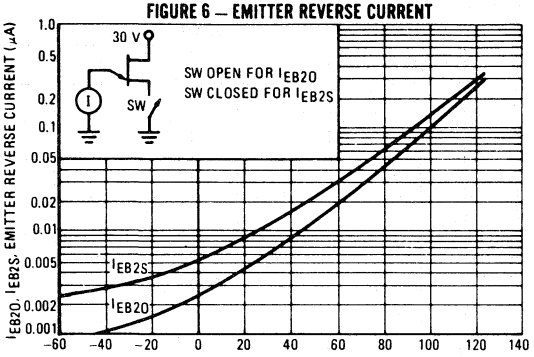
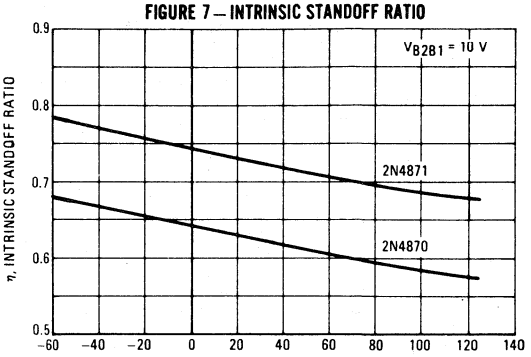


FIGURE 7 — INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 — EFFECT OF VOLTAGE

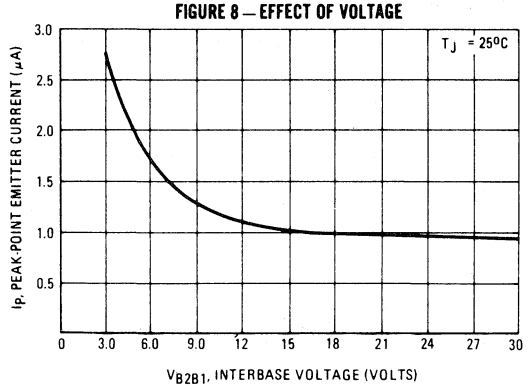
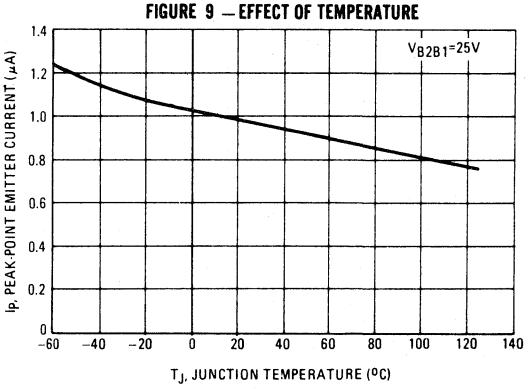


FIGURE 9 — EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 — EFFECT OF VOLTAGE

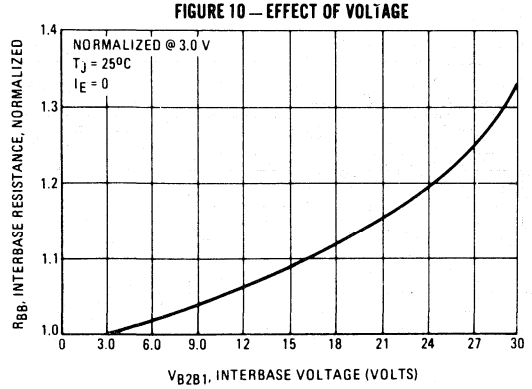
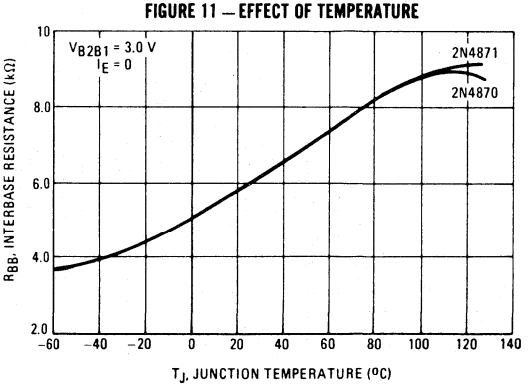


FIGURE 11 — EFFECT OF TEMPERATURE



TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 — EFFECT OF VOLTAGE

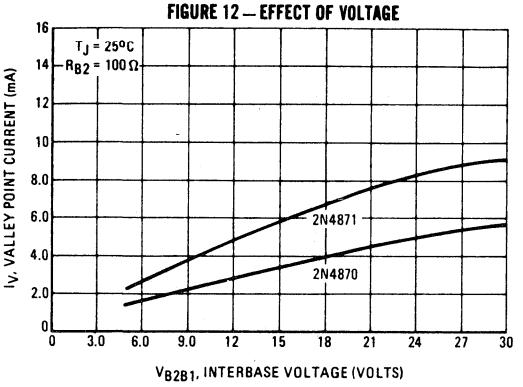
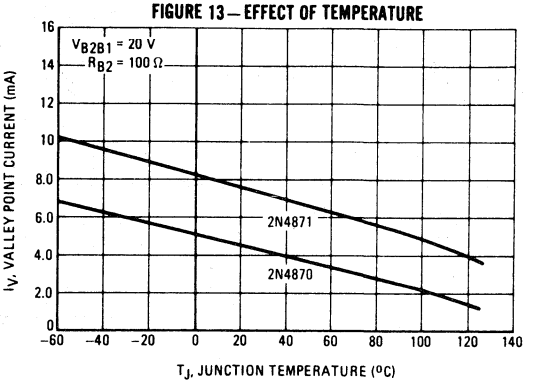


FIGURE 13 — EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 14 — EFFECT OF VOLTAGE

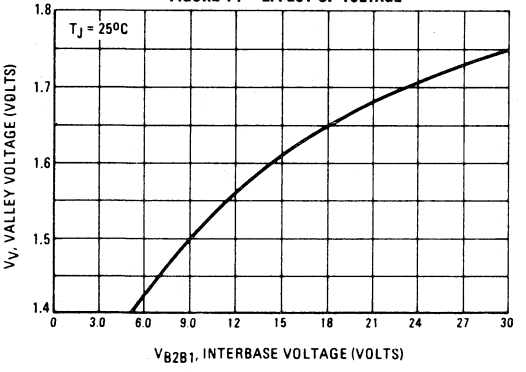


FIGURE 15 — EFFECT OF TEMPERATURE

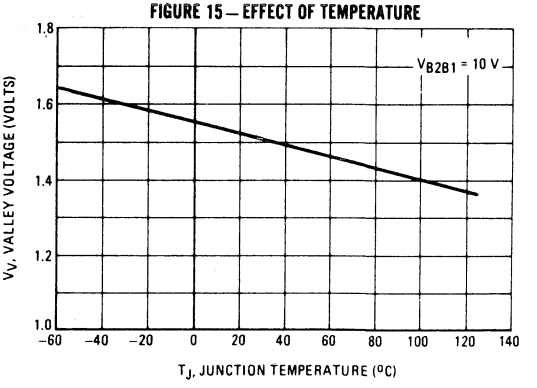
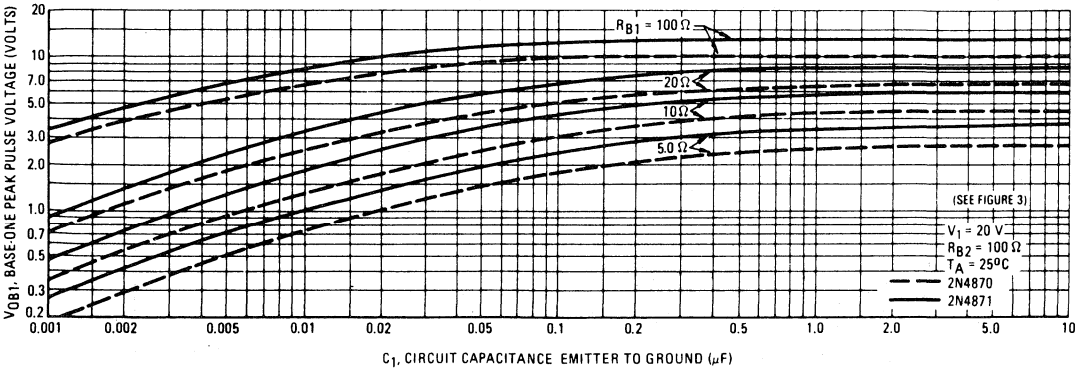
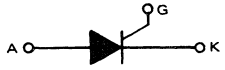


FIGURE 16 — OUTPUT VOLTAGE





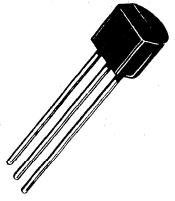
PLASTIC THYRISTORS

. . . Annular♦ PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 μA Maximum
- Low Reverse and Forward Blocking Current — 50 μA Maximum, T_C = 125°C
- Low Holding Current — 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS



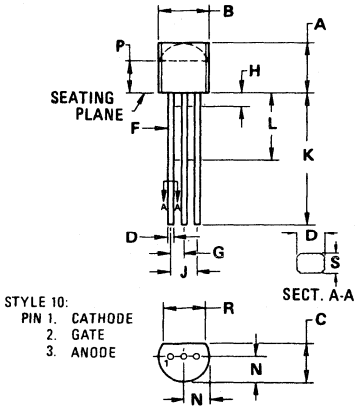
MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
*Peak Repetitive Reverse Blocking Voltage (2) 2N5060 2N5061 2N5062 2N5063 2N5064	V_{RRM}	 30 60 100 150 200	Volts
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	 0.51 0.255	Amp
*Peak Non-Repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
*Peak Gate Power, T_A = 25°C	P_{GM}	0.1	Watt
*Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.01	Watt
*Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	1.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	5.0	Volts
*Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s Max)	—	+230*	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
(2) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.92	0.080	0.115
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

♦Annular Semiconductor Patented by Motorola Inc.
*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (Note 1) (T_C = 125°C, R_{GK} = 1000 Ohms)	2N5060	V_{DRM}	30	–	–	Volts
	2N5061		60	–	–	
	2N5062		100	–	–	
	2N5063		150	–	–	
	2N5064		200	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{DRM}	–	–	50	μA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{RRM}	–	–	50	μA
*Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	–	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3)	T_C = 25°C	I_{GT}	–	–	200	μA
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_C = -65°C		–	–	350	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–		0.8	Volts
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–		1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1		–	
Holding Current	T_C = 25°C	I_H	–	–	5.0	mA
*(Anode Voltage = 7.0 Vdc, initiating current = 20 mA	T_C = -65°C		–	–	10	
Turn-On Time						μs
Delay Time		t_d	–	3.0	–	
Rise Time		t_r	–	0.2	–	
(I_{GT} = 1.0 mA, R_{GK} = 1.0 Ohm, V_{RRM} = 30 V, Forward Current = 1.0 A, di/dt = 6.0 A/μs)						
Turn-Off Time	2N5060,2N5061	tq	–	10	–	μs
(Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1.0 mA, R_{GK} = 1.0 k Ohm)	2N5062,5063,5064		–	30	–	
Forward Voltage Application Rate (Rated V_{DRM}, R_{GK} = 1.0 k, Exponential)		dv/dt	–	300	–	V/μs

*Indicates JEDEC Registered Data.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

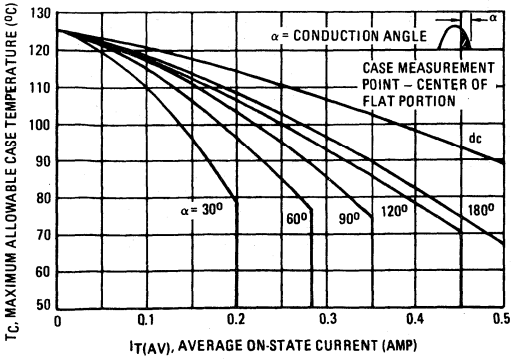


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE

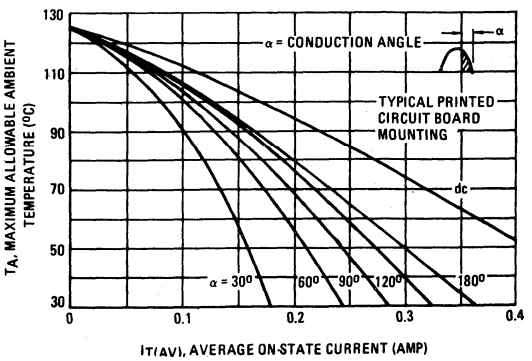


FIGURE 3 – TYPICAL FORWARD VOLTAGE

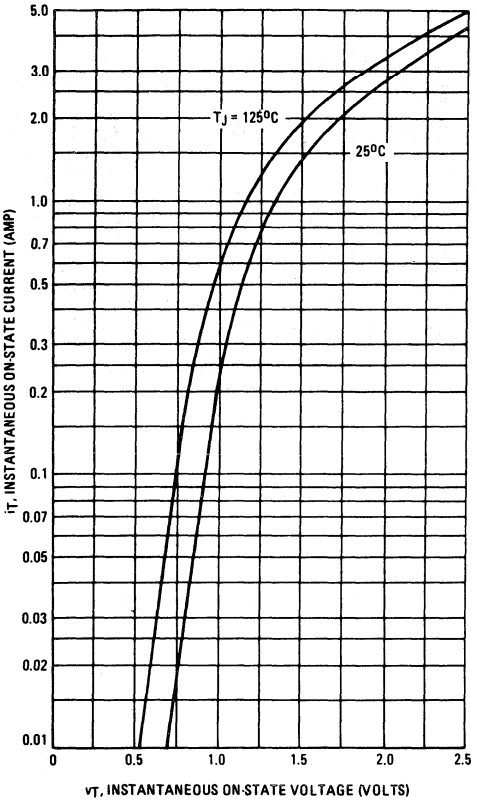


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

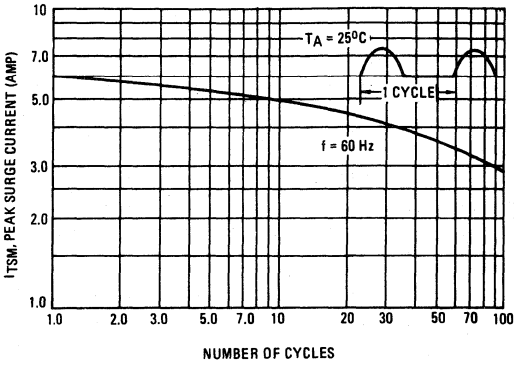


FIGURE 5 – POWER DISSIPATION

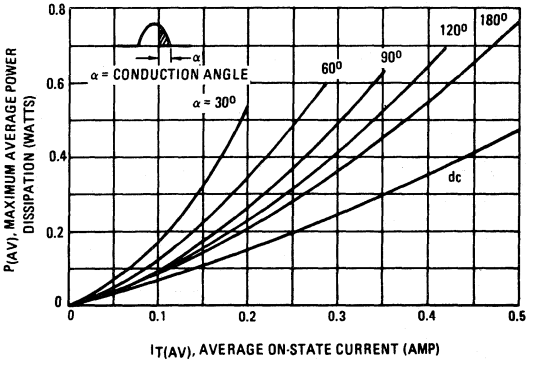
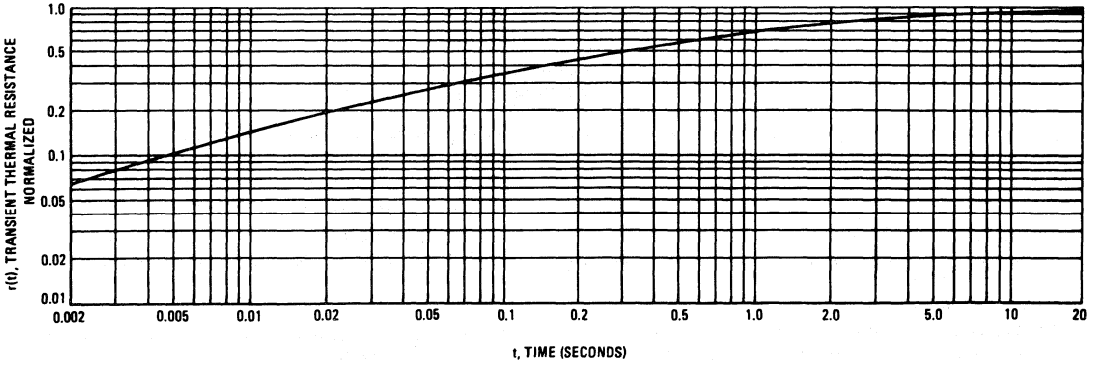


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

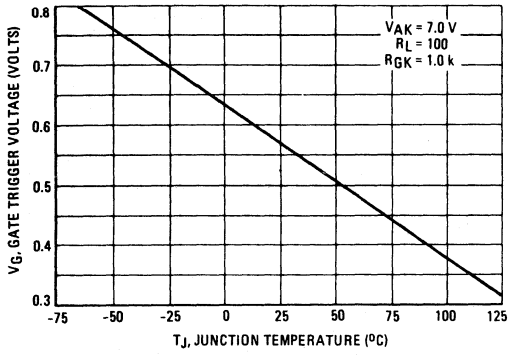


FIGURE 8 – GATE TRIGGER CURRENT

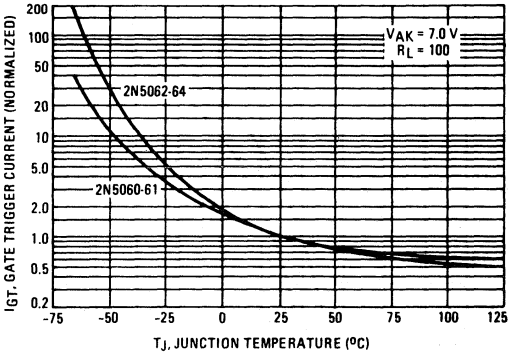


FIGURE 9 – HOLDING CURRENT

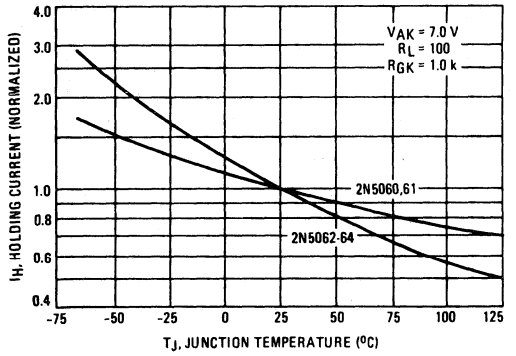
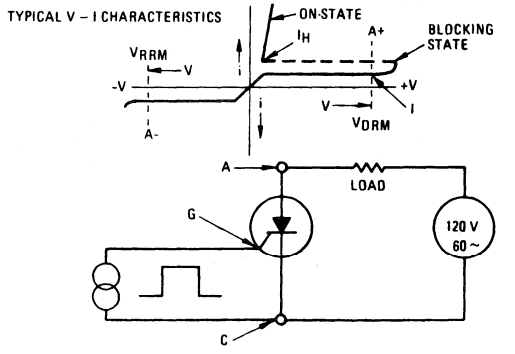


FIGURE 10 – CHARACTERISTICS AND SYMBOLS



THYRISTOR APPLICATION NOTES

AN-189 Solid-State Pulse Width Modulation DC Motor Control

AN-240 SCR Power Control Fundamentals

AN-295 Suppressing RFI in Thyristor Circuits

AN-413 Unijunction Trigger Circuits for Gated Thyristors

AN-441 SCR Slaving Circuits

AN-443 Directional and Speed Control for Series, Universal and Shunt Motors

AN-450 Induction Motor Speed Control

AN-453 Zero Point Switching Techniques

AN-482 Electronic Speed Control of Appliance Motors

AN-526 Theory, Characteristics and Applications of Silicon Unilateral and Bilateral Switches

AN-527 Theory, Characteristics and Applications of the Programmable Unijunction Transistor

AN-568 A Fuse-Thyristor Coordinator Primer

AN-580 Thermal Runaway in High Power Thyristors

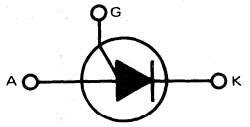
AN-597 Power Control Uisng the Zero Voltage Switch

AN-599 Mounting Techniques for Metal Packaged Power Semiconductors

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to:

Technical Information Center
Motorola Semiconductor Products, Inc.
P.O Box 20924
Phoenix, Arizona 85036

2N6027
2N6028



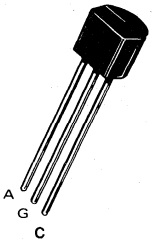
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

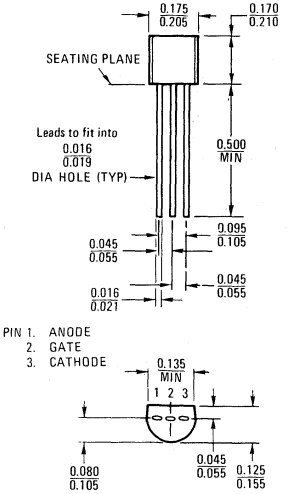
40 VOLTS
375 mW



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation (1) Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current (2) Derate Above 25°C	I_T	200 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle *20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
* Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
* Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
* Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
* Anode to Cathode Voltage	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
* Storage Temperature Range	T_{stg}	-55 to +150	°C

*Indicates JEDEC Registered Data
(1) JEDEC Registered Data is 300 mW, derating at 4.0 mW/°C.
(2) JEDEC Registered Data is 150 mA.



All JEDEC dimensions and notes apply

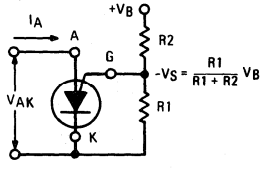
CASE 29-03
TO-92
PLASTIC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

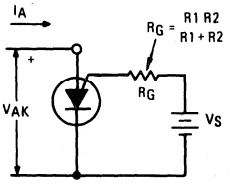
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
*Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	1.25	2.0	
	2N6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			–	4.0	5.0	
	2N6028			–	0.70	1.0	
*Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	18	50	
	2N6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	270	–	
	2N6028			25	270	–	
(V_S = 10 Vdc, R_G = 200 Ohms)	2N6027			1.5	–	–	mA
	2N6028			1.0	–	–	
* Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
*Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

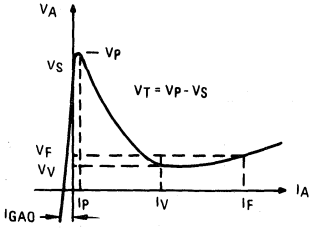
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2



1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)



1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

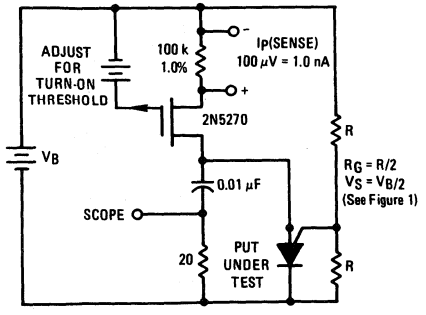
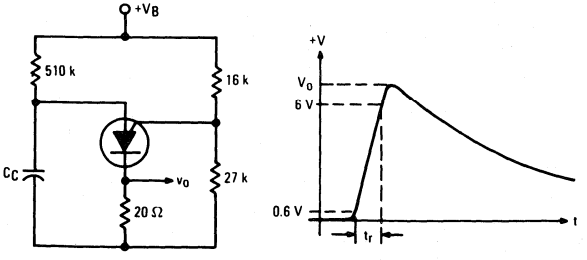


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

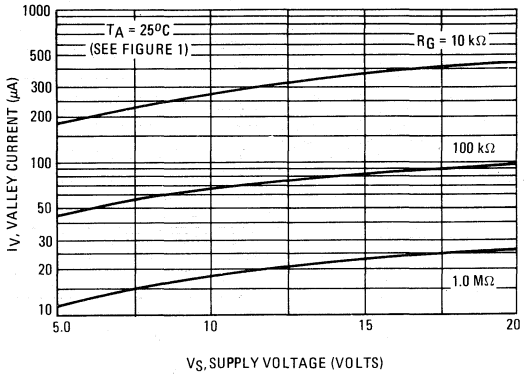


FIGURE 5 – EFFECT OF TEMPERATURE

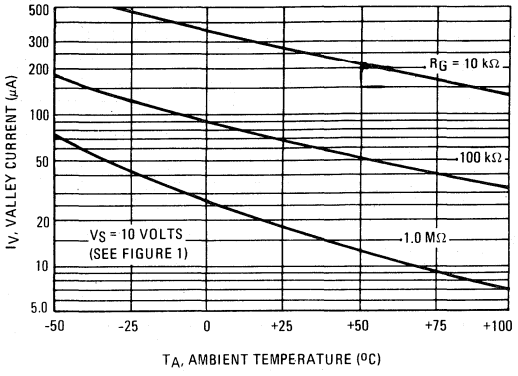


FIGURE 6 – FORWARD VOLTAGE

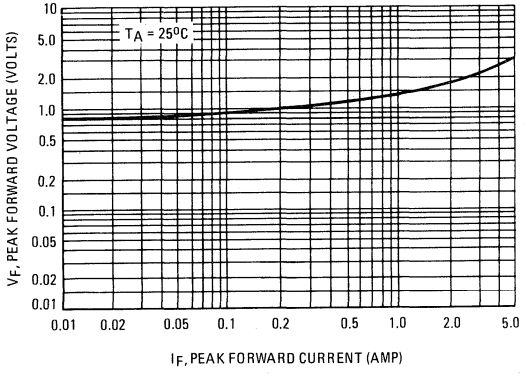


FIGURE 7 – PEAK OUTPUT VOLTAGE

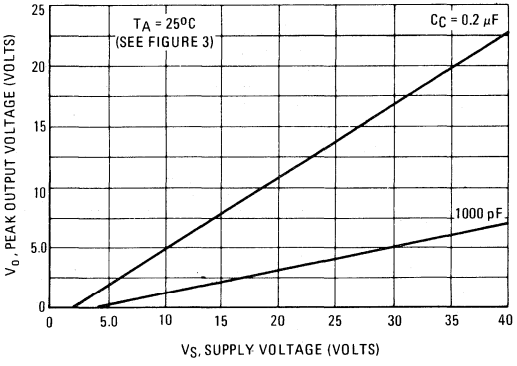
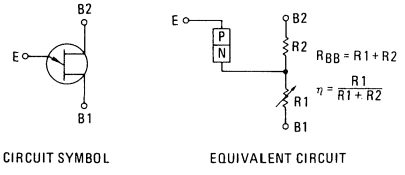


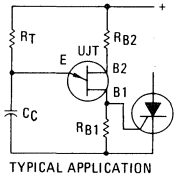
FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

STANDARD UNIJUNCTION



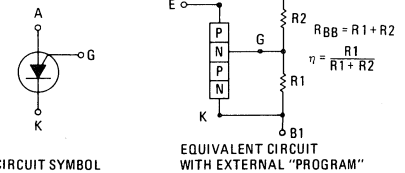
CIRCUIT SYMBOL

EQUIVALENT CIRCUIT



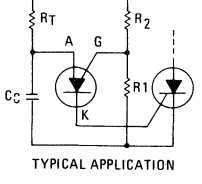
TYPICAL APPLICATION

PROGRAMMABLE UNIJUNCTION



CIRCUIT SYMBOL

EQUIVALENT CIRCUIT WITH EXTERNAL "PROGRAM" RESISTORS R1 and R2



TYPICAL APPLICATION

TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

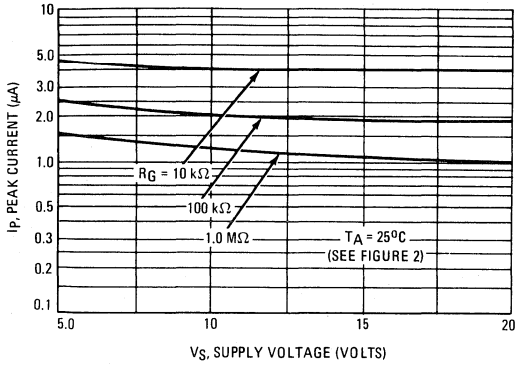
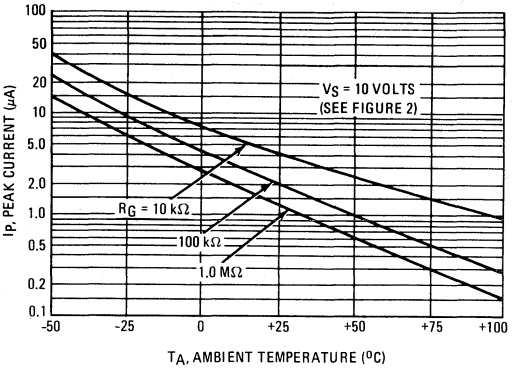


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

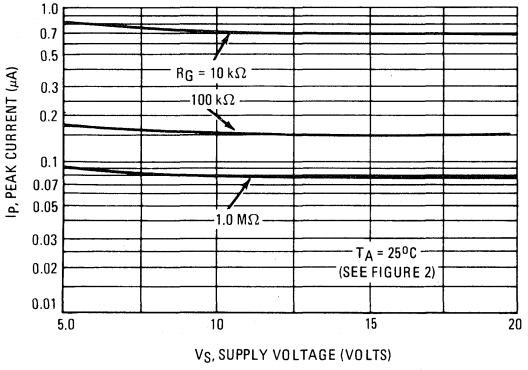
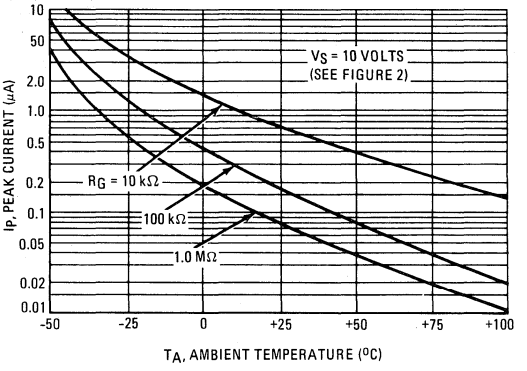
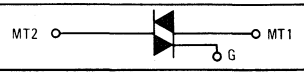


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G





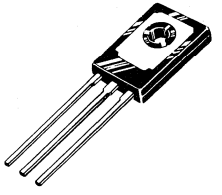
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions.
- Gate Triggering 2 Mode – 2N6068 thru 2N6075
  4 Mode – 2N6068A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SENSITIVE GATE

TRIACS
(THYRISTORS)
4 AMPERES RMS
25 THRU 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C) 2N6068,A,B	V_{DRM}	25	Volts
2N6069,A,B		50	
2N6070,A,B		100	
2N6071,A,B		200	
2N6072,A,B		300	
2N6073,A,B		400	
2N6074,A,B		500	
2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4.0	Amp
*Peak Surge Current (One Full cycle, 60 Hz, T_J = -40 to +110°C)	I_{TSM}	30	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	3.6	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5.0	Volts
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb.

THERMAL CHARACTERISTICS

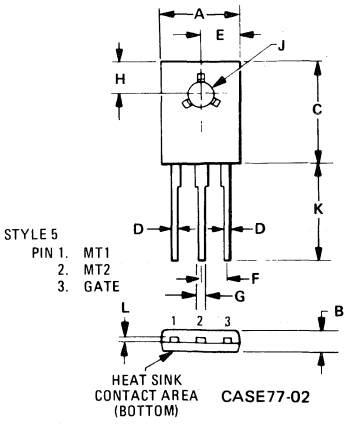
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R\theta_{CA}$	60	°C/W

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

▲Trademark of Motorola Inc.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.270	0.330	6.860	8.380
B	0.070	0.130	1.770	3.300
C	0.390	0.450	9.910	11.430
D	0.020	0.026	0.508	0.660
E	0.150 NOM		3.810 NOM	
F	0.090 TP		2.290 TP	
G	0.025	0.035	0.635	0.889
H	0.130	0.175	3.300	4.450
J	0.115	0.118	2.910	3.000
K	0.595	0.655	15.110	16.650
L	0.015	0.025	0.381	0.635

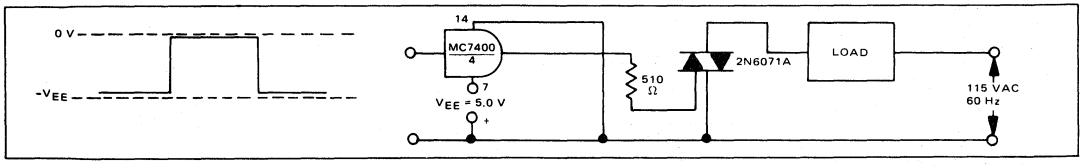
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

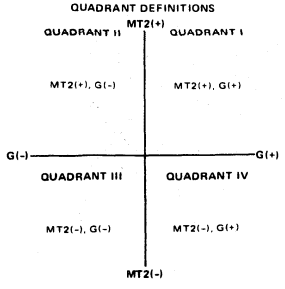
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 6.0 A Peak	V_{TM}	–	–	2.0	Volts
*Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = -40°C	V_{GTM}				Volts
MT2 (+), G(+); MT2 (–), G(–) All Types		–	1.4	2.5	
MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B		–	1.4	2.5	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B		0.2	–	–	
*Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, T_J = -40°C Initiating Current = 1.0 Adc	I_H				mA
2N6068 thru 2N6075		–	–	70	
2N6068A,B thru 2N6075A,B		–	–	30	
T_J = 25°C 2N6068 thru 2N6075		–	–	30	
2N6068A,B thru 2N6075A,B		–	–	15	
Turn-On Time (Either Direction) I_{TM} = 14 Adc, I_{GT} = 100 mAdc	t_{on}	–	1.5	–	μs
Blocking Voltage Application Rate at Commutation @ V_{DRM}, T_J = 85°C, Gate Open	dv/dt	–	5.0	–	V/μs

	Type	I_{GTM} @ T_J	QUADRANT (See Definition Below) I mA	II mA	III mA	IV mA
*Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 ohms Maximum Value	2N6068 thru 2N6075	+25°C	30	–	30	–
		-40°C	60	–	60	–
	2N6068A thru 2N6075A	+25°C	5.0	5.0	5.0	10
		-40°C	20	20	20	30
	2N6068B thru 2N6075B	+25°C	3.0	3.0	3.0	5.0
		-40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III





Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

For 2N6068 Thru 2N6075

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

SENSITIVE GATE LOGIC REFERENCE

IC LOGIC FUNCTIONS	FIRING QUADRANT I	II	III	IV
TTL		2N6068A Series	2N6068A Series	
HTL		2N6068A Series	2N6068A Series	
McMOS (NAND)	2N6068B Series			2N6068B Series
McMOS (Buffer)		2N6068B Series	2N6068B Series	
Operational Amplifier	2N6068A Series			2N6068A Series
Zero Voltage Switch		2N6068A Series	2N6068A Series	

FIGURE 1 – AVERAGE CURRENT DERATING

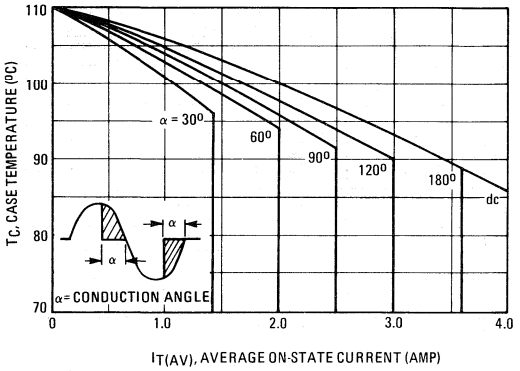


FIGURE 2 – RMS CURRENT DERATING

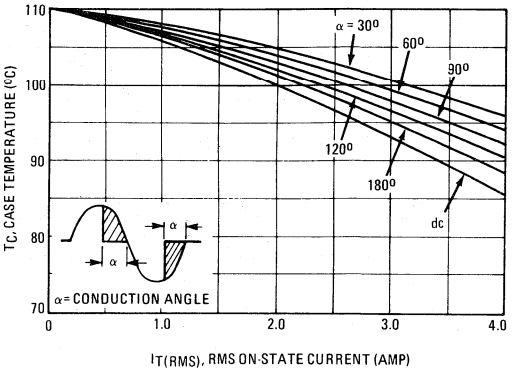


FIGURE 3 – POWER DISSIPATION

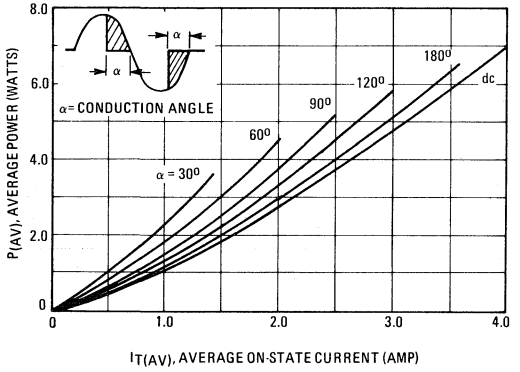


FIGURE 4 – POWER DISSIPATION

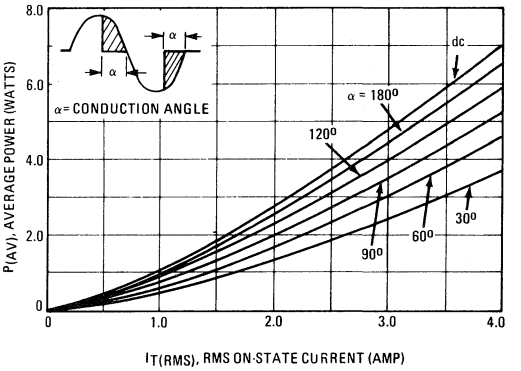


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

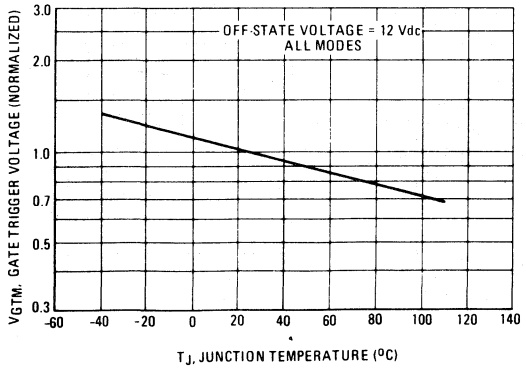


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT

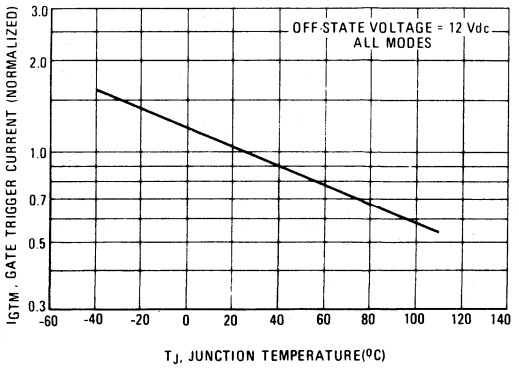


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

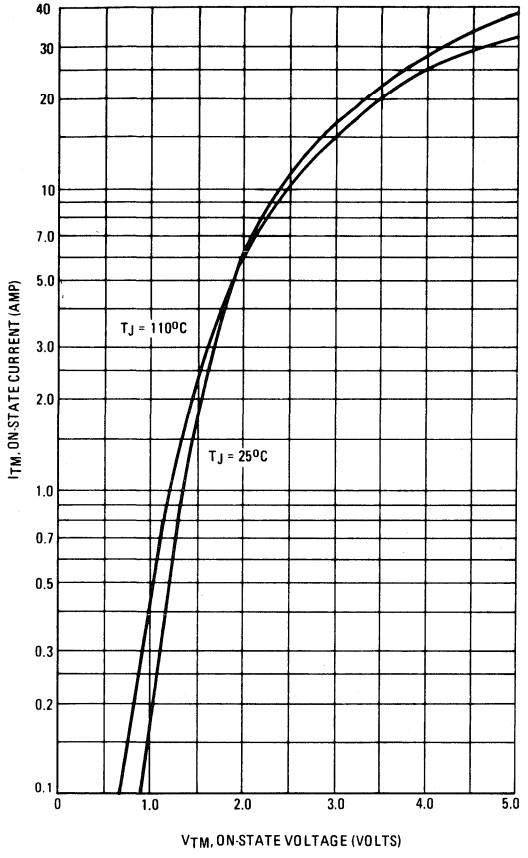


FIGURE 8 – TYPICAL HOLDING CURRENT

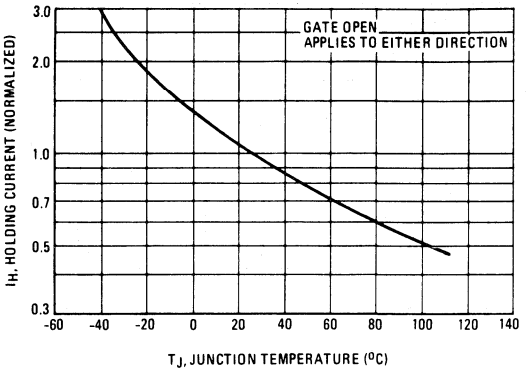


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

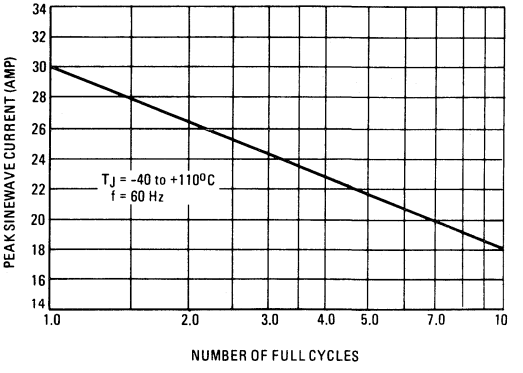
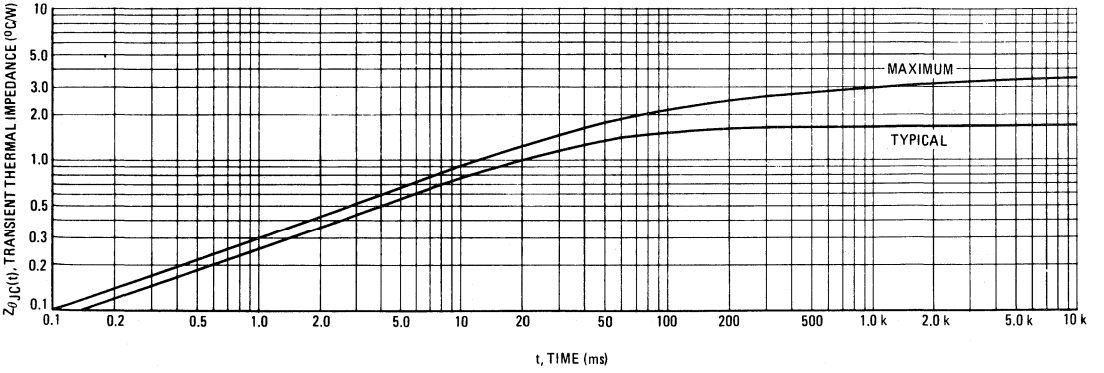
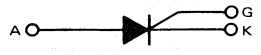


FIGURE 10 – THERMAL RESPONSE





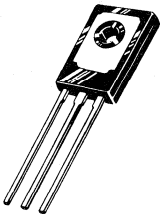
SILICON CONTROLLED RECTIFIERS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106

THYRISTORS

4.0 AMPERES RMS
30 thru 600 VOLTS



MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

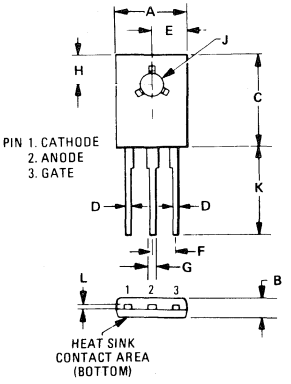
Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage (Note 1) (1/2 Sine Wave) (Gate Open, T_J = -40 to +110°C)	2N6236	V_{DRM}, V_{RRM}	30	Volts
	2N6237		50	
	2N6238		100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage (1/2 Sine Wave, Gate Open, T_J = -40 to +110°C)	2N6236	V_{RSM}	50	Volts
	2N6237		100	
	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current (T_C = -40 to +90°C) (T_C = +100°C)		$I_{T(AV)}$	2.6 1.6	Amp
*Surge On-State Current (1/2 Sine Wave, 60 Hz, T_C = +90°C) (1/2 Sine Wave, 1.5 ms, T_C = +90°C)		I_{TSM}	25 35	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)		I^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs)		P_{GM}	0.5	Watts
*Average Gate Power (t = 8.3 ms)		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6.0	Volts
*Operating Junction Temperature Range		T_J	-40 to +110	°C
*Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (Note 2)		—	6.0	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.

▲Trademark of Motorola Inc.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.270	0.330	6.860	8.380
B	0.070	0.130	1.770	3.300
C	0.390	0.450	9.910	11.430
D	0.020	0.026	0.508	0.660
E	0.150 NOM		3.810 NOM	
F	0.090 TP		2.290 TP	
G	0.025	0.035	0.635	0.889
H	0.130	0.175	3.300	4.450
J	0.115	0.118	2.910	3.000
K	0.595	0.655	15.110	16.650
L	0.015	0.025	0.381	0.635

CASE 77-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms.)

Characteristics	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (Note 1) (Rated V_{DRM}, T_J = 110°C)	I_{DRM}	–	–	200	μA
*Peak Reverse Blocking Current (Note 1) (Rated V_{RRM}, T_J = 110°C)	I_{RRM}	–	–	200	μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (V_{AK} = 12 Vdc, R_L = 24 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	I_{GT}	– –	– –	200 500	μA
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_J = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, I_{GT} = 2.0 mA) T_J = 25°C *(Initiating On-State Current = 200 mA) T_J = -40°C	I_H	– –	– –	5.0 10	mA
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6.0 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2.0 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	–	–	2.0	μs
Forward Voltage Application Rate (T_J = 110°C)	dv/dt	–	10	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

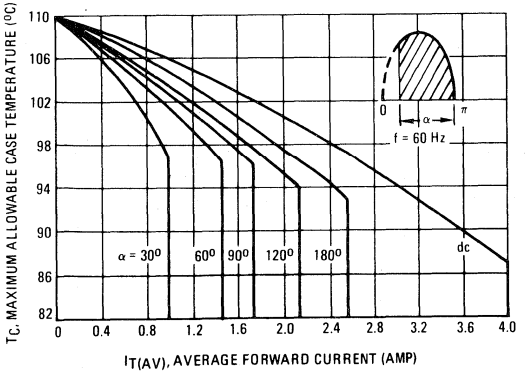
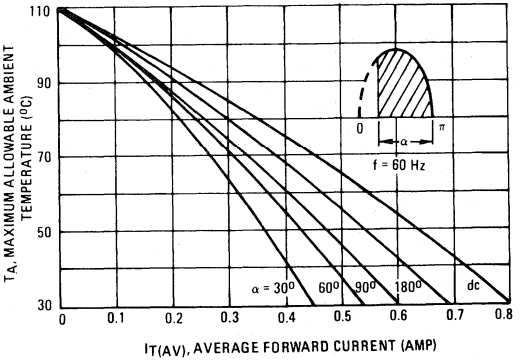
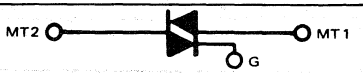


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



2N6342 thru 2N6349
MAC220 Series • MAC221 Series

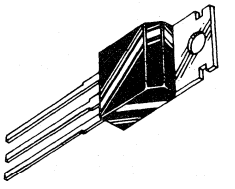


SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345, MAC220 Series) or Four Modes (2N6346, 2N6347, 2N6348,2N6349,MAC221 Series)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

TRIACS
(THYRISTORS)
8 AMPERES RMS
200-800 VOLTS



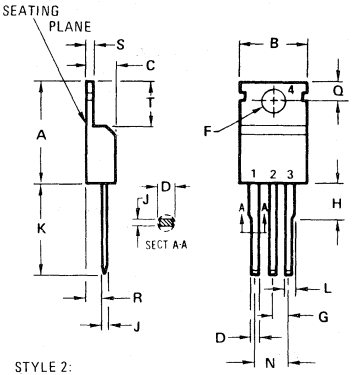
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC220-2,MAC221-2		50	
MAC220-3,MAC221-3		100	
2N6342,2N6346		200	
MAC220-5,MAC221-5		300	
2N6343,2N6347		400	
MAC220-7,MAC221-7		500	
2N6344,2N6348		600	
MAC220-9,MAC221-9		700	
2N6345,2N6349		800	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	8.0 4.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) preceded and followed by 10 Rated Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.2	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

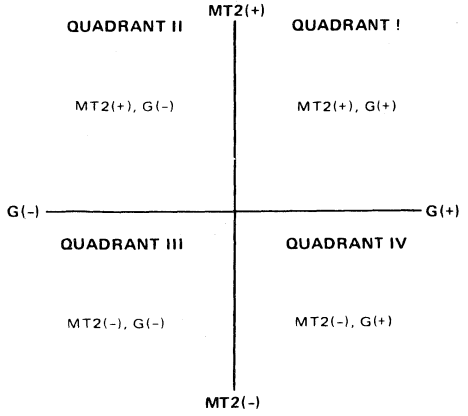
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 11 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.55	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	12	50	
MT2 (+), G(–) 2N6346 thru 49,MAC221		–	12	75	
MT2 (–), G(–) All Types		–	20	50	
MT2 (–), G(+) 2N6346 thru 49,MAC221		–	35	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346 thru 49,MAC221		–	–	125	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346 thru 49, MAC221		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346 thru 49, MAC221		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346 thru 49, MAC221		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(–) 2N6346 thru 49, MAC221		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General	
PART NUMBER	MBS4991	MBS4992
V_S	6.0 – 10 V	7.5 – 9.0 V
I_S	350 μA Max	120 μA Max
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max
Temperature Coefficient	0.02%/°C Typ	

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

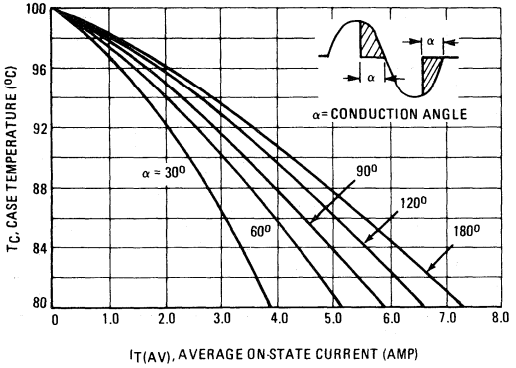


FIGURE 2 – RMS CURRENT DERATING

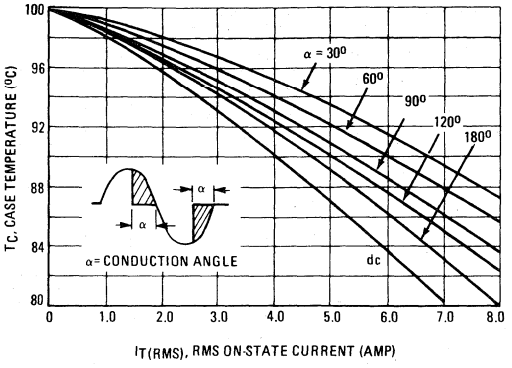


FIGURE 3 – ON-STATE POWER DISSIPATION

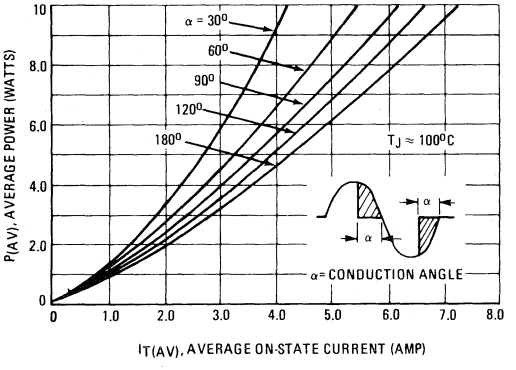


FIGURE 4 – ON-STATE POWER DISSIPATION

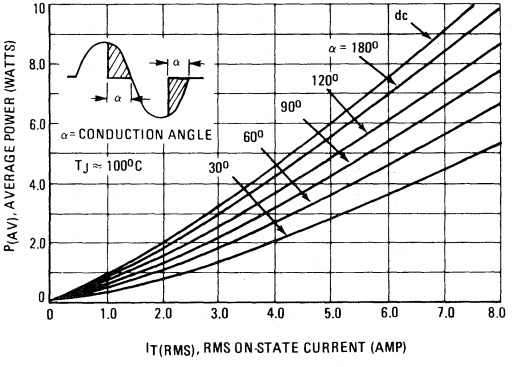


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

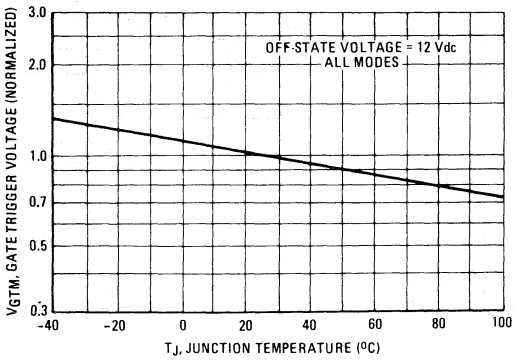


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

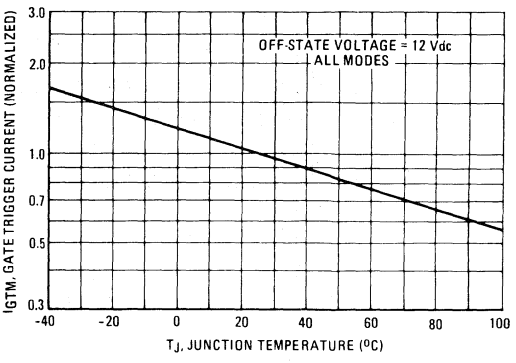


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

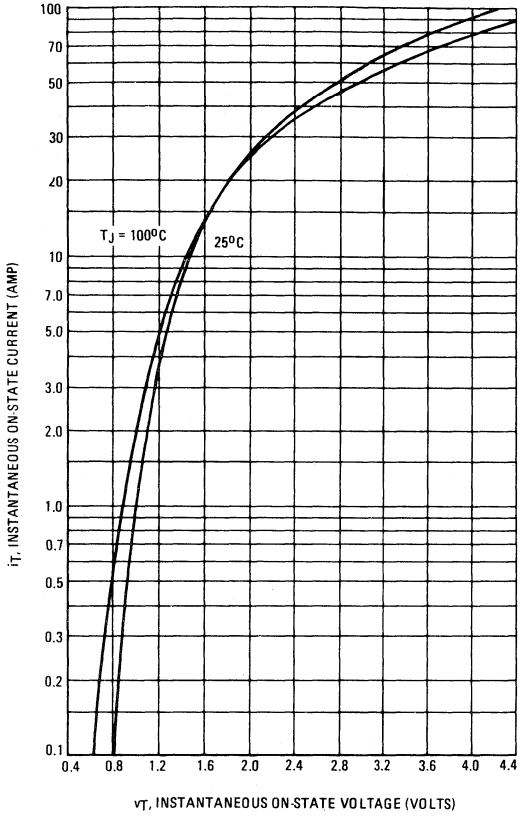


FIGURE 8 – TYPICAL HOLDING CURRENT

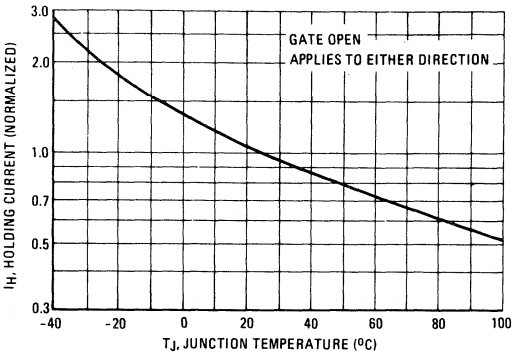


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

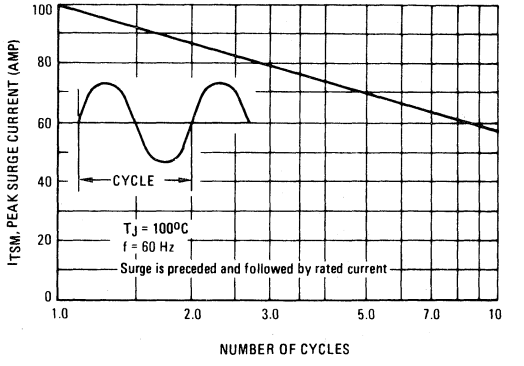
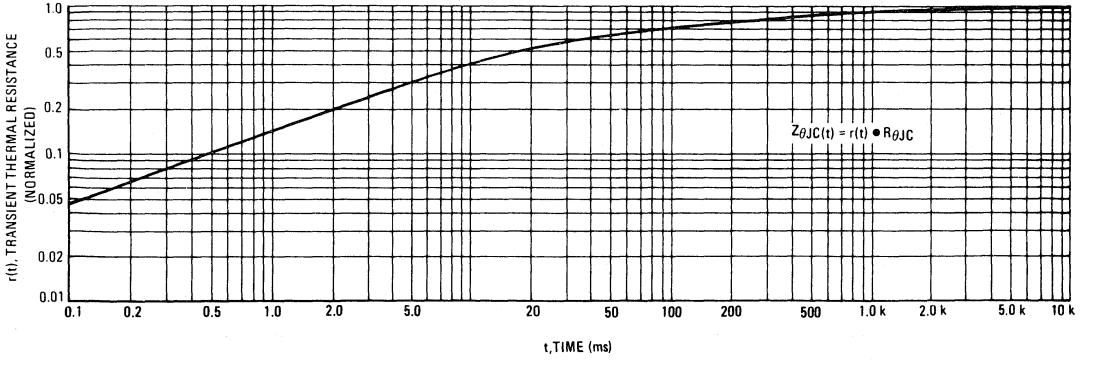
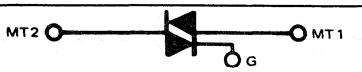


FIGURE 10 – THERMAL RESPONSE



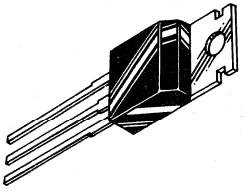


SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349

TRIACS (THYRISTORS) 12 AMPERES RMS 200 – 800 VOLTS



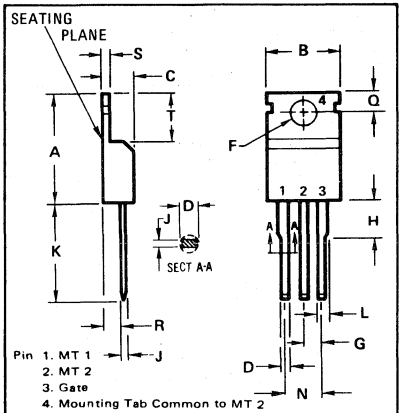
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N6342A, 2N6346A		200	
2N6343A, 2N6347A		400	
2N6344A, 2N6348A		600	
2N6345A, 2N6349A		800	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +95°C)	$I_{T(RMS)}$	12 6.0	Amp
*Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	120	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB
All JEDEC dimensions and notes apply

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

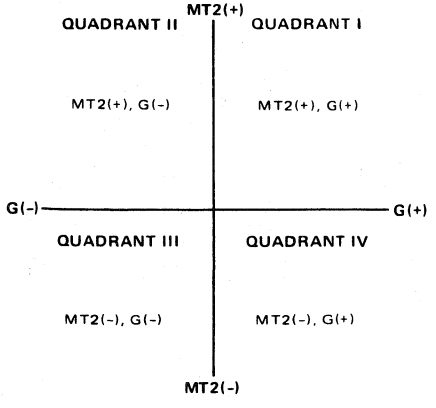
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.75	Volts
Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GTM}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	125	
Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GTM}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6346A thru 2N6349A		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6346A thru 2N6349A		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA; T_C = 25°C	I_H	–	6.0	40	mA
T_C = -40°C		–	–	75*	
*Turn-On Time Rated V_{DRM}, I_{TM} = 17A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 17A, Commutating di/dt = 6.5 A/ms, Gate Unenergized T_C = 80°C	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 – 10 V	7.5 – 9.0 V	3.0 – 5.0 V
I_S	350 μA Max	120 μA Max	100 – 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

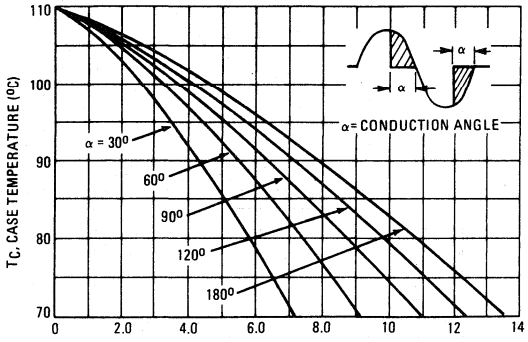


FIGURE 2 – RMS CURRENT DERATING

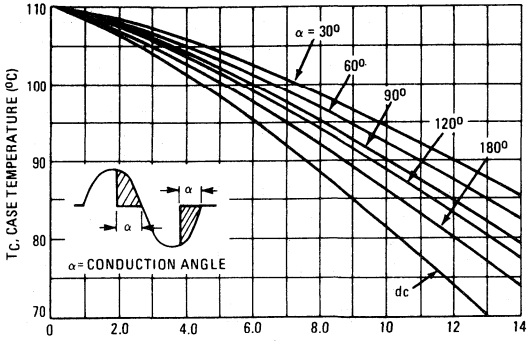


FIGURE 3 – ON-STATE POWER DISSIPATION

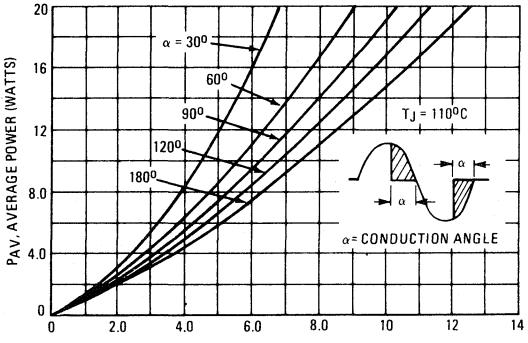


FIGURE 4 – ON-STATE POWER DISSIPATION

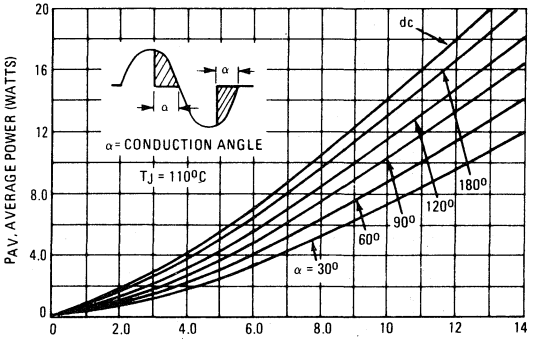


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

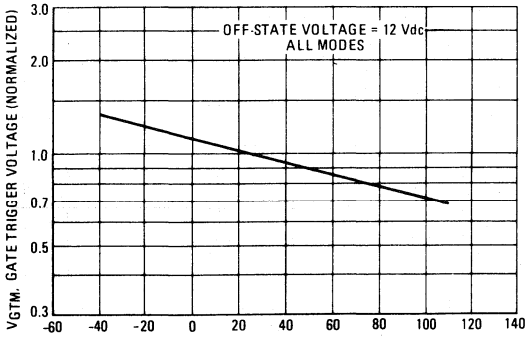


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

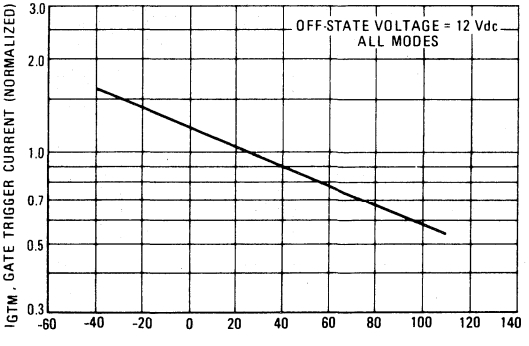


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

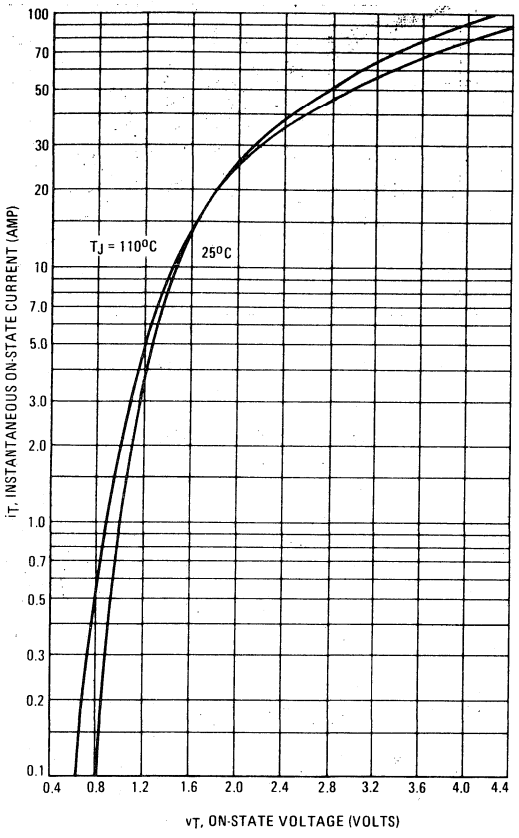


FIGURE 8 – TYPICAL HOLDING CURRENT

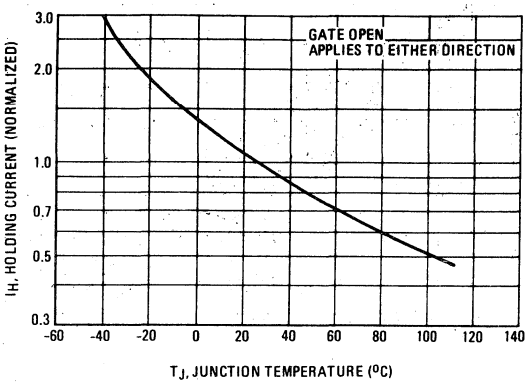


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

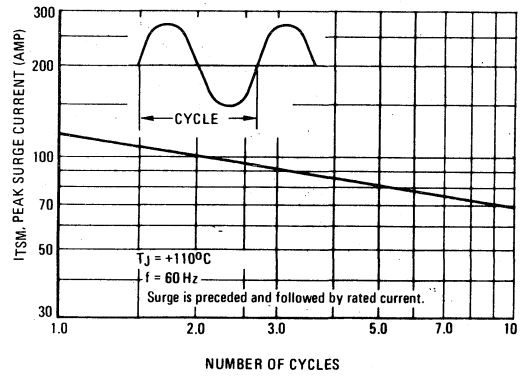
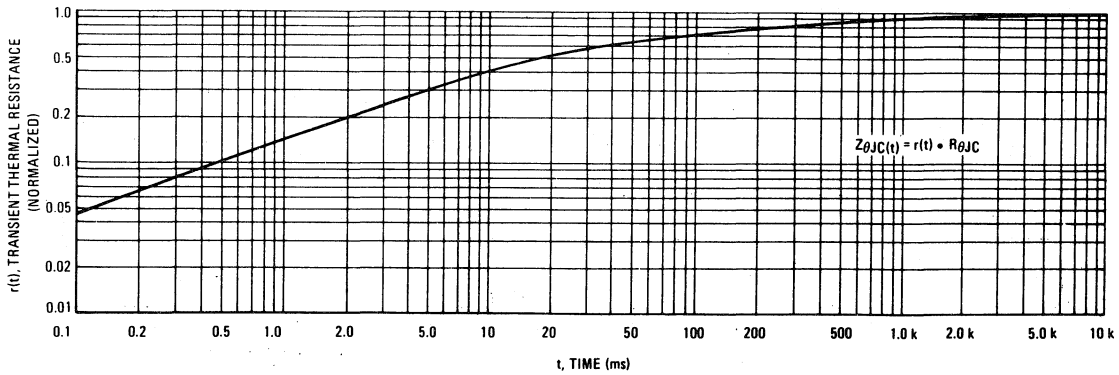
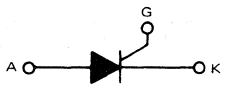


FIGURE 10 – THERMAL RESPONSE



2N6394 thru 2N6399
MCR220-5 • MCR220-7 • MCR220-9



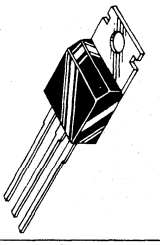
THYRISTORS

12 AMPERES RMS
50-800 VOLTS

SILICON CONTROLLED RECTIFIERS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Voltage (1)	V_{RRM}		Volts
2N6394		50	
2N6395		100	
2N6396		200	
MCR220-5		300	
2N6397		400	
MCR220-7		500	
2N6398		600	
MCR220-9		700	
2N6399		800	
Forward Current RMS T_J = 125°C (All Conduction Angles)	$I_{T(RMS)}$	12	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	100	Amps
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.

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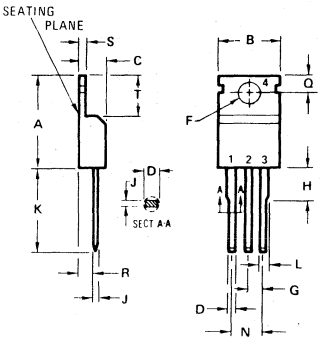


PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H		6.35		0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)		V_{DRM}				Volts
	2N6394		50	–	–	
	2N6395		100	–	–	
	2N6396		200	–	–	
	MCR220-5		300	–	–	
	2N6397		400	–	–	
	MCR220-7		500	–	–	
	2N6398		600	–	–	
	MCR220-9		700	–	–	
	2N6399		800	–	–	
* Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
* Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
* Forward "On" Voltage (I_{TM} = 24 A Peak)		V_{TM}	–	1.7	2.2	Volts
* Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
* Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
* Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
* Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	2.0	μs
Turn-Off Time (V_{DRM} = rated voltage)		tq				μs
(I_{TM} = 12 A, I_R = 12 A)			–	15	–	
(I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)			–	35	–	
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

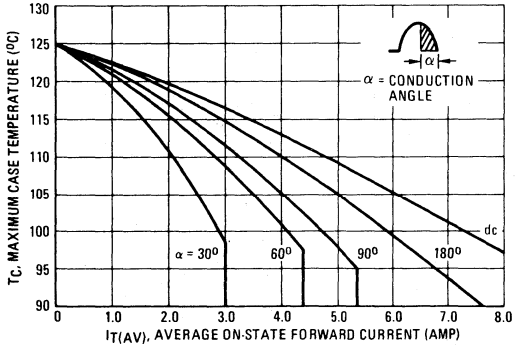


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

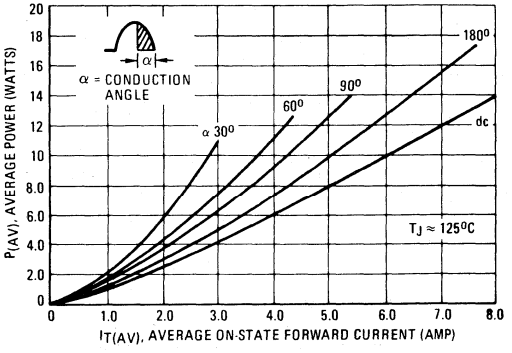


FIGURE 3 – ON-STATE CHARACTERISTICS

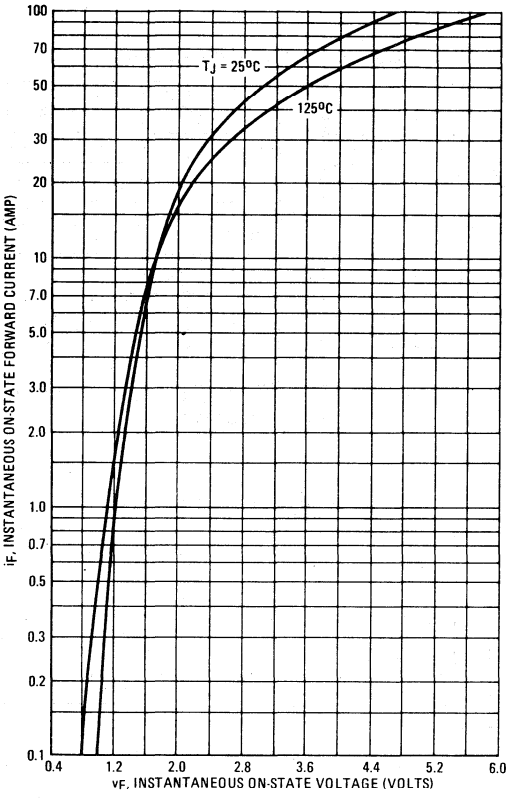


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

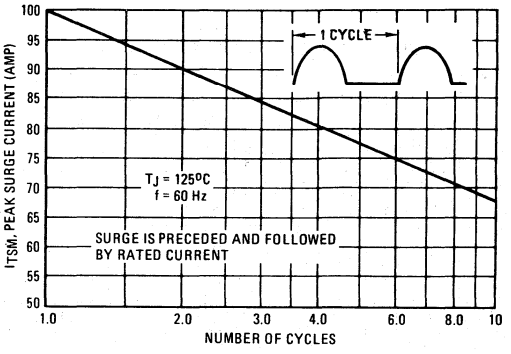


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

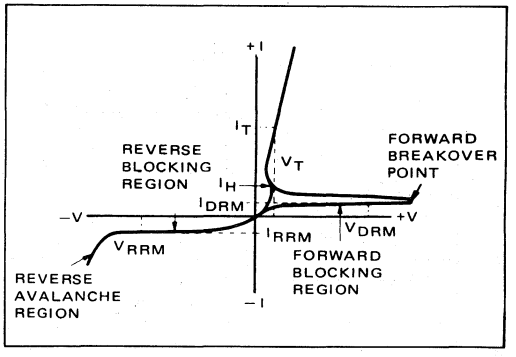
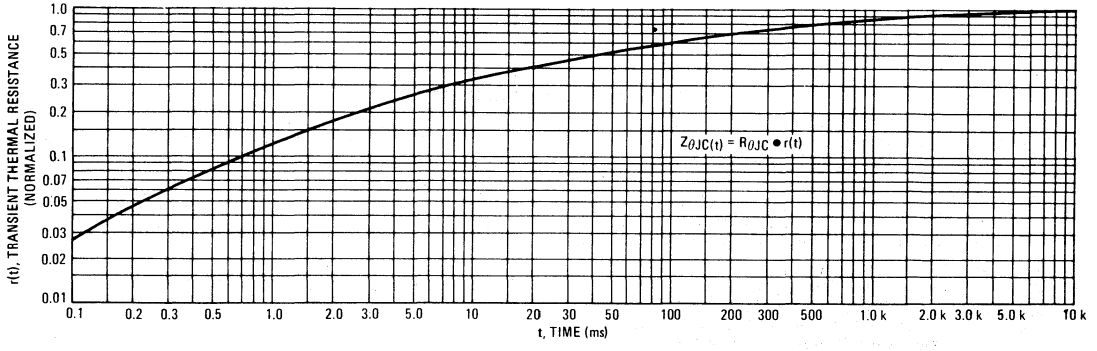


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – PULSE TRIGGER CURRENT

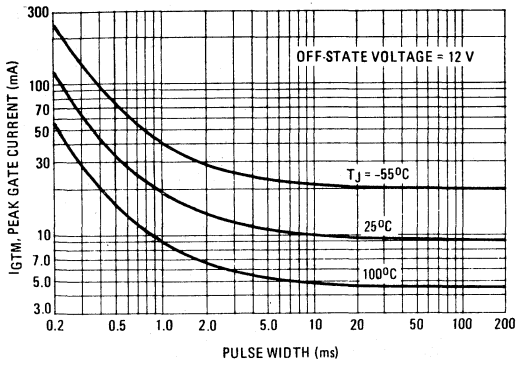


FIGURE 8 – GATE TRIGGER CURRENT

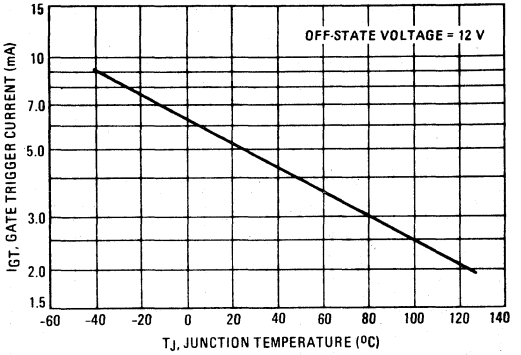


FIGURE 9 – GATE TRIGGER VOLTAGE

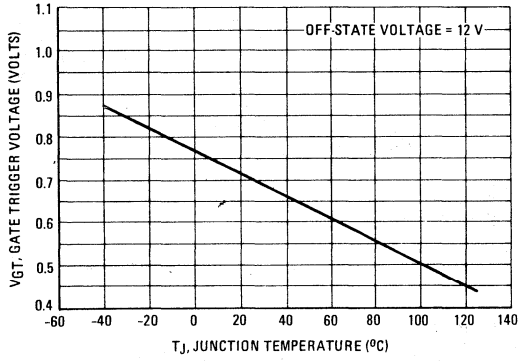
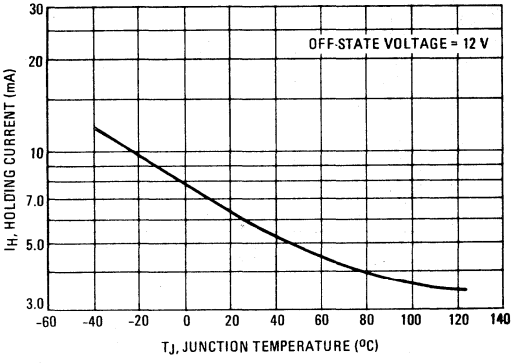


FIGURE 10 – HOLDING CURRENT



THYRISTOR APPLICATION NOTES

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AN-734 SCR Controller for a Series Field dc Motor

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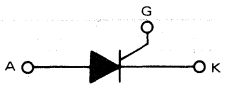


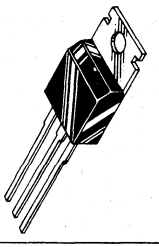
SILICON CONTROLLED RECTIFIERS

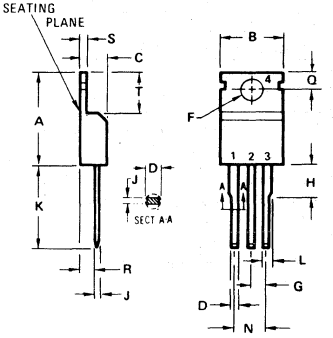
. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts

THYRISTORS

16 AMPERES RMS
50-800 VOLTS





PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1) 2N6400 2N6401 2N6402 MCR221-5 2N6403 MCR221-7 2N6404 MCR221-9 2N6405	V_{RRM}	 50 100 200 300 400 500 600 700 800	Volts
Forward Current RMS (T_C = 90°C) (All Conduction Angles)	$I_{T(RMS)}$	16	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	160	Amps
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

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*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (T_J = 125°C)	2N6400	V_{DRM}	50	–	–	Volts
	2N6401		100	–	–	
	2N6402		200	–	–	
	MCR221-5		300	–	–	
	2N6403		400	–	–	
	MCR221-7		500	–	–	
	2N6404		600	–	–	
	MCR221-9		700	–	–	
	2N6405		800	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
*Forward "On" Voltage (I_{TM} = 32 A peak)		V_{TM}	–	–	1.7	Volts
*Gate Trigger Current (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		I_{GT}	–	5.0	30	mA
*Gate Trigger Voltage (Continuous dc) (Anode Voltage = 12 Vdc, R_L = 100 Ohms)		V_{GT}	–	0.7	1.5	Volts
*Gate Non-Trigger Voltage (Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)		V_{GD}	0.2	–	–	Volts
*Holding Current (Anode Voltage = 12 Vdc)		I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc)		t_{gt}	–	1.0	–	μs
Turn-Off Time (V_{DRM} = rated voltage)		t_q				μs
(I_{TM} = 16 A, I_R = 16 A)			–	15	–	
(I_{TM} = 16 A, I_R = 16 A, T_J = 125°C)			–	35	–	
Forward Voltage Application Rate (T_J = 125°C)		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

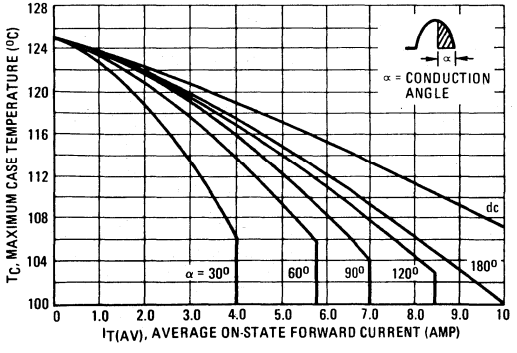


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

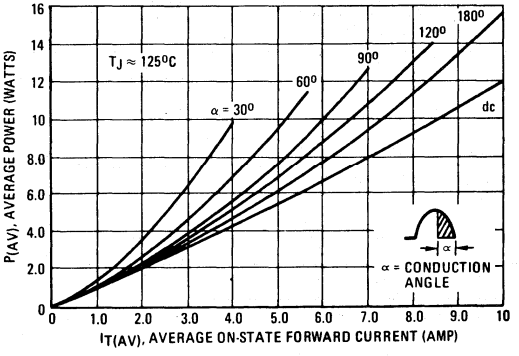


FIGURE 3 – ON-STATE CHARACTERISTICS

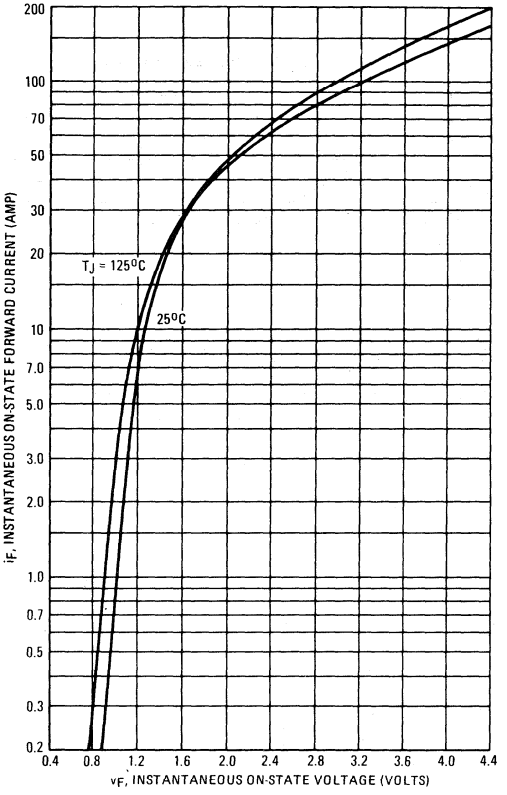


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

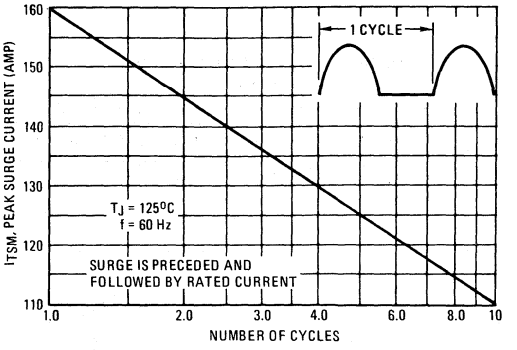


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

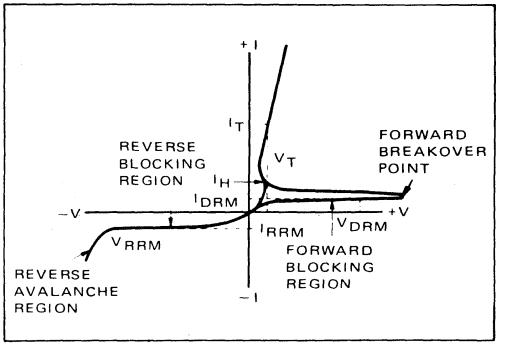
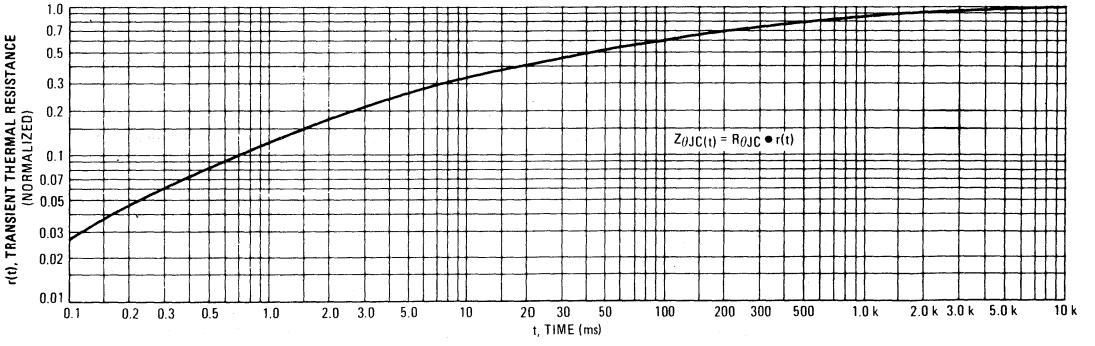


FIGURE 6 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 7 – GATE TRIGGER CURRENT

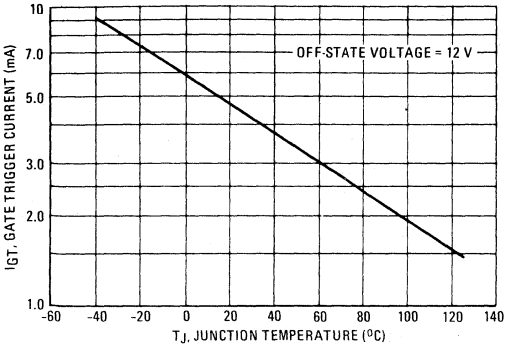


FIGURE 8 – GATE TRIGGER VOLTAGE

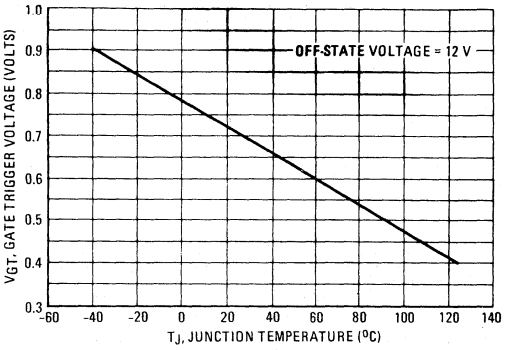
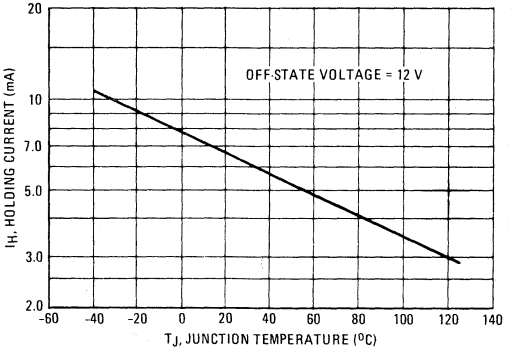


FIGURE 9 – HOLDING CURRENT



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DIODES and BRIDGES

	Rectifier Diodes	V_{RRM} Max. V	I_{FAV} Max. A	I_{FSM} Max. A	V_F Max. V	I_R Max. μA	t_{rr} Max. μS	Package	Page
Fast, Soft and Standard Recovery	BA157-159	400-1000	0.5	25	1.3	5	0.3	59-04	7-1
	BY126-127	650-1250	1	40	–	–	–	59-04	7-7
	BY196-199	100-800	1.2	70	1.2	10	0.5	59-04	7-9
	BY206-207	350-600	0.6	25	1.4	2	0.3	59-04	7-11
	BY210	400-800	1	30	1.4	10	0.3	59-04	7-13
	BY251-255	200-1300	3	100	1.1	10	–	267	7-15
	BY296-299, 400	100-1300	2	100	1.3	10	0.5	267-01	7-21
	BY330-334	50-400	1	40	1.25	10	0.75	59-04	7-23
	BY336-339	500-1500	1	40	1.25	10	0.75	59-04	7-23
	BY601-608	50-1250	1.5	50	1.15	10	–	59-04	7-29
	BYX10	1600	0.6	25	1.4	4	–	59-04	7-36
	MR501, 502, 504	100-400	3	100	1.1	5	–	267	7-57
	MR506, 508, 510	600-1000	3	100	1.1	5	–	267	7-57
	MR751, 752, 754, 756	100-600	6	400	1.25	250	–	194-02	7-63
	MR810-814	50-400	1	30	1.1	10	0.75	59-04	7-67
	MR816-818	500-1000	1	30	1.1	10	0.75	59-04	7-67
	MR850-852, 854-856	50-600	3	100	1.25	10	0.2	267	7-73
	MR910-914	50-400	3	100	1.25	10	0.75	267-01	7-81
	MR916-918	500-1000	3	100	1.25	10	0.75	267-01	7-81
	1N4001-4007	50-100	1	30	1.1	10	–	59-04	7-98
	1N4933-4937, MR2271	50-600	1	30	1.1	5	0.2	59-04	7-102
Hot Carrier	1N5817-5818	20-30	1	100	0.55	1000	–	59	7-112
	1N5820-5821	20-30	3	250	0.5	2000	–	267	7-116
Single Phase Full Wave Bridge	BYW20-29	50-1000	15	400	–	100	–	309-01	7-33
	MDA920A1-920A9	25-1000	1.5	45	–	20	–	109-03	7-49
	3N246-252 (MDA100A-110A)	50-1000	1	30	–	10	–	312-02	7-120
	3N253-259 (MDA200-210)	50-1000	2	60	–	10	–	312-02	7-122

	Reference Diodes	$V_{Z\ (nom)}$ V	I_{Zr} mA	P_D Max. mW	Package	Page
Zener Diodes	BZX79 C2V4-C200	2.4-200	5	500	DO-35	7-38
	BZX83 C2V7-C33 (MZPD2.7-3.3)	2.7-33	5	500	DO-35	7-41
	MZD3.9-200	3.9-200	–	1300	DO-41	7-94
	1N5333-5388	3.3-200	–	5000	17	7-108
Tuning Diode Volt. Reference Diodes	MVS240	24	26	625	182-03	7-90
	MVS460	33	18	625	182-01	7-92

Variable Capacitance Tuning Diodes	V_R Max. V	I_F Max. mA	C_T P_F Min.	C_T P_F Max.	@ f MHz	@ V_R V	C_R Min.	@ f MHz	Q Min.	@ f MHz	@ V_R V	Package	Page
BB105A-105G, 205B-205G	30	20	2.3-1.8	2.8-2.6	–	25	4-4.3	–	225-150	100	–	226	7-3
BB109	30	200	26	32	1	3	5	1	280	50	3	226	7-5
MV104	32	200	37	42	1	3	2.5	1	100	100	3	TO-92	7-82
MV209	30	200	26	32	1	3	5	1	200	50	3	182-02	7-84
MV1401	12	250	468	633	1	1	14	1	200	1	2	DO-14	7-86
MV1403-1405	12	250	140	300	1	2	10	1	200	1	2	DO-14	7-86
MVAM115	18	50	440	560	1	1	15	1	150	1	1	182-03	7-88
MVAM125	28	50	440	560	1	1	15	1	150	1	1	182-03	7-88

Hot Carrier Diodes	V_R Max. V	V_F @ I_F = 10 mA Max. V	C_T Max. pF	@ f MHz	@ V_R V	I_R Max. nA	@ V_R V	Package	Page
MBD101	4	0.6	1	1	0	250	3	182-01	7-43
MBD102	4	0.6	1	1	0	250	3	226	7-45
MBI-101	4	0.6	1	1	0	250	3	166-02	7-47

Pin Switching Diodes	V_R Max. V	R_S @ I_F = 10 mA Max. Ω	C_T Max. pF	@ f MHz	@ V_R V	L_S Typ nH	@ f MHz	Package	Page
MPN3401	30	0.7	1	1	20	3	250	226	7-53
MPN3402	30	0.6	2	1	20	3	250	226	7-53
MPN3404	20	0.85	2	1	15	6	250	182-03	7-55

BA157 Series

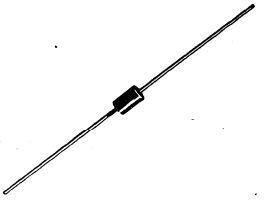
AXIAL LEAD MOUNTED RECTIFIERS

Featuring non snap off characteristics

. . . intended switchmode power supplies, TV scan rectifiers and HF power supplies.

SILICON RECTIFIER DIODES

400, 600, 1,000 VOLTS
400 mA



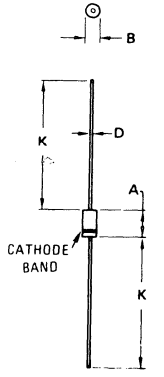
MAXIMUM RATINGS

Rating	Symbol	BA157	BA158	BA159	Unit
Peak repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	400	600	1000	Volts
Non-Repetitive Reverse Voltage	V_{RSM}	500	800	200	Volts
Average Rectified Forward Current (Average over any 20 mS period)	I_{FAV}	0.4			Amp
Repetitive Peak Forward Current	I_{FRM}	2			Amp
Non-Repetitive Peak Surge Current, (t = 10 ms, half sine wave, T_J = 125°C prior to surge)	I_{FSM}	15			Amp
Storage Junction Temp. range	T_{stg}	— 65 to + 150			°C
Junction Temperature	T_J	+ 150			°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Forward Voltage I_F = 5 A, T_J = 25°C (see Note 1)	V_F		1.3	Volts
Reverse Current $V_R = V_{RRM}$, T_J = 25°C $V_R = V_{RRM}$, T_J = 125°C	I_R		5 100	μA
Capacitance at F = 1 MHz $V_R = V_{RRM}$	C_d	2		pF
Reverse Recovery Charge I_F = 1 A to V_R 50 with $\frac{-dI}{dt}$ = 1.0 A/μs $\frac{-dI}{dt}$ = 20 A/μs	Q_S			 nC nC
Reverse Recovery Time I_F = 10 mA through I_R = 10 mA to I_R = 1 mA	t_{rr}		300	nS

Note 1: Measured under pulse conditions to avoid excessive dissipation.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

Does Not Conform to DO-41 Outline

7

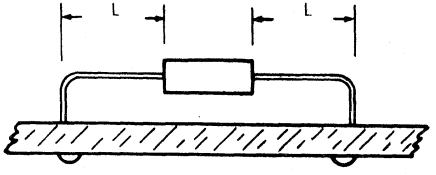
THERMAL RESISTANCE

Data shown for thermal resistance junction to ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

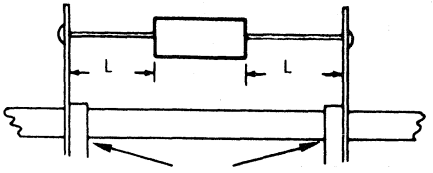
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

Mounting Method	Lead length, L (mm) 3.18	6.35	12.7	19.1	$R\theta_{JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3		40			°C/W

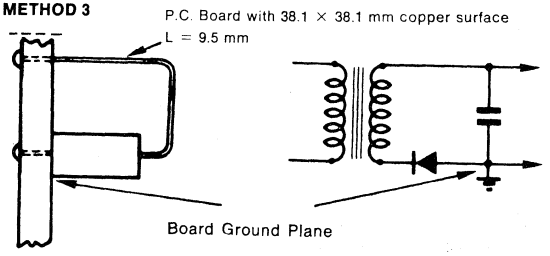
MOUNTING METHOD 1



MOUNTING METHOD 2
Vector Pin mounting



MOUNTING METHOD 3



BB105A, B, G
BB205B, G

VVC

SILICON EPICAP▲ DIODES

. . . designed in the low-inductance mini-L package for high volume requirements of UHF and VHF TV tuning and AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

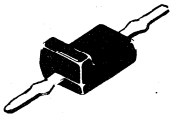
- Guaranteed Minimum Q Values at VHF and UHF Frequencies
- Controlled and Uniform Tuning Ratio
- Guaranteed Matching* Tolerance From Diode to Diode

* Upon request, diodes are available in matched sets or matched groups. All diodes in a set or group are matched for a given capacitance tolerance at all points along the specified tuning range.
BB105A, BB105B, BB205B and BB205G can be ordered matched to ±1.5% by adding "M" to the device title (i.e., BB205BM).
BB105G will be supplied matched to ±3.0% if "M" is added to the device title. All matched groups will be shipped in multiples of 12 pcs. Minimum quantity per group is 48 pcs.

Matched sets of for example 3 or 4 diodes can also be ordered by adding "M3" (multiples of 3) or "M4" (multiples of 4) to the device title respectively. By ordering this option any quantity per bag in multiples of 3 or 4 will be shipped.

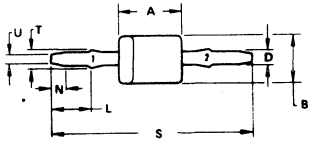
VOLTAGE VARIABLE CAPACITANCE DIODES

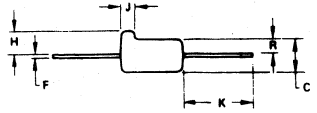
30 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	20	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



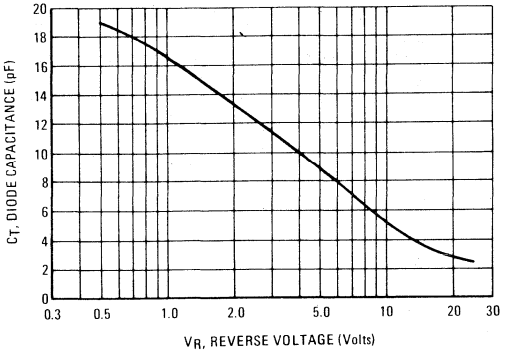


PIN 1 CATHODE
2 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.86	4.11	0.152	0.162
B	2.92	3.18	0.115	0.125
C	1.91	2.16	0.075	0.085
D	0.64	0.89	0.025	0.035
F	0.08	0.18	0.003	0.007
H	1.30	1.55	0.051	0.061
J	0.64	0.89	0.025	0.035
K	4.06	4.32	0.160	0.170
L	2.36	2.62	0.093	0.103
N	1.12	1.37	0.044	0.054
R	0.79	1.04	0.031	0.041
S	11.99	12.75	0.472	0.502
T	1.14	1.40	0.045	0.055
U	0.43	0.69	0.017	0.027

CASE 226

FIGURE 1 – DIODE CAPACITANCE (TYPICAL)



▲Trademark of Motorola Inc.

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic-All Types	Symbol	Min	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	–	Vdc
Reverse Voltage Leakage Current (VR = 28 V) (VR = 28 V) T_A = 60°C	I_R	–	50.0 0.5	nAdc μAdc
Series Inductance (f = 250 MHz)	L_S	–	3.0	nH
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	400	ppm/°C

Device Type	C_T V_R = 25 Vdc pF		Q f = 100 MHz C_T = 9 pF	R_S Ohms	C_3/C_{25}	
	Min	Max	Min	Max	Min	Max
BB105A	2.3	2.8	225	0.8	4.0	5
BB105B	2.0	2.3	225	0.8	4.5	6
BB105G	1.8	2.8	150	1.2	4.0	6
BB205B	1.9	2.2	225	0.8	5.0	6
BB205G	1.8	2.6	150	1.2	4.3	6

FIGURE 2 – FIGURE OF MERIT

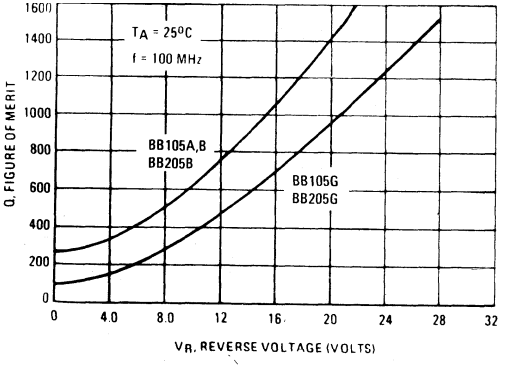
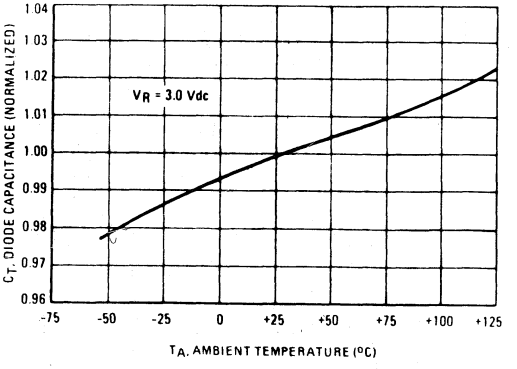


FIGURE 3 – DIODE CAPACITANCE



VVC

SILICON EPICAP▲ DIODE

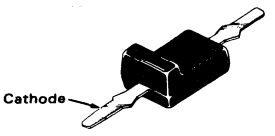
. . . designed in the new low-inductance Mini-L package for high volume requirements in VHF TV tuning, AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q With Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Low Inductance Mini-L Package
- Guaranteed Matching* Tolerance From Diode to Diode and Group to Group

*Upon request, diodes are available in matched sets of any number or in matched groups.

VOLTAGE VARIABLE CAPACITANCE DIODE

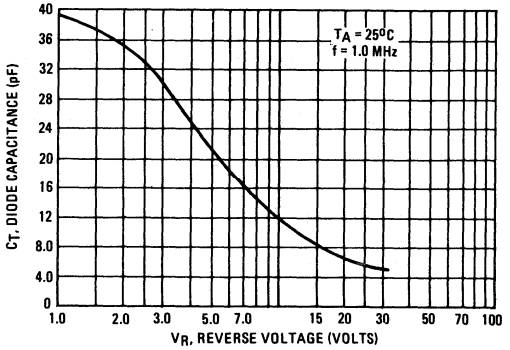
26–32 pF

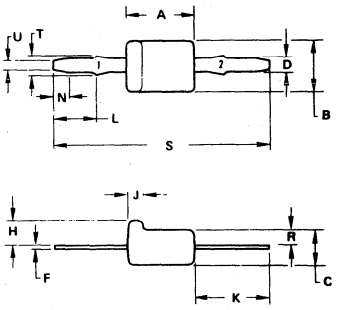


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE





PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.86	4.11	0.152	0.162
B	2.92	3.18	0.115	0.125
C	1.91	2.16	0.075	0.085
D	0.64	0.89	0.025	0.035
F	0.08	0.18	0.003	0.007
H	1.30	1.55	0.051	0.061
J	0.64	0.89	0.025	0.035
K	4.06	4.32	0.160	0.170
L	2.36	2.62	0.093	0.103
N	1.12	1.37	0.044	0.054
R	0.79	1.04	0.031	0.041
S	11.99	12.75	0.472	0.502
T	1.14	1.40	0.045	0.055
U	0.43	0.69	0.017	0.027

CASE 226

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 28 Vdc, T_A = 25°C)	I_R	–	–	50	nA
Series Inductance (f = 250 MHz, Measured at Lead Stop≈1/8")	L_S	–	3.0	–	nH
Case Capacitance (f = 1.0 MHz)	C_C	–	0.1	–	pF
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	400	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz		Package Stripe
Device	Min	Nom	Max	Min	Min	Max	Color
BB109	26	29	32	280	5.0	6.5	RED

FIGURE 2 – FIGURE OF MERIT

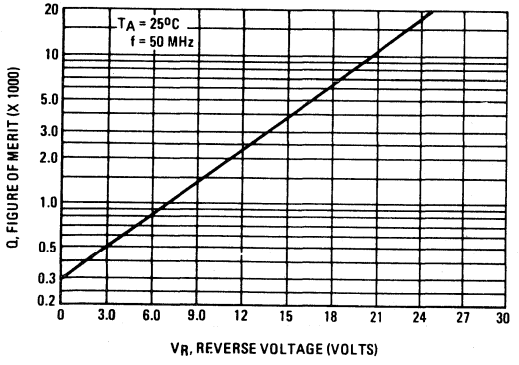


FIGURE 3 – LEAKAGE CURRENT

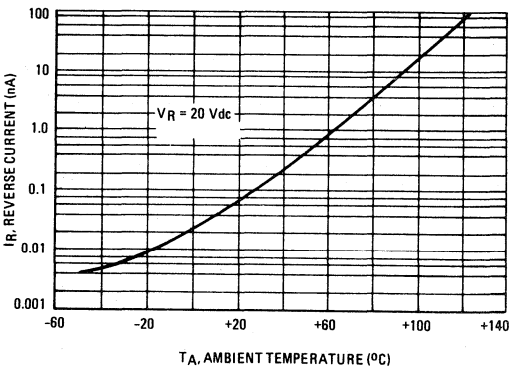
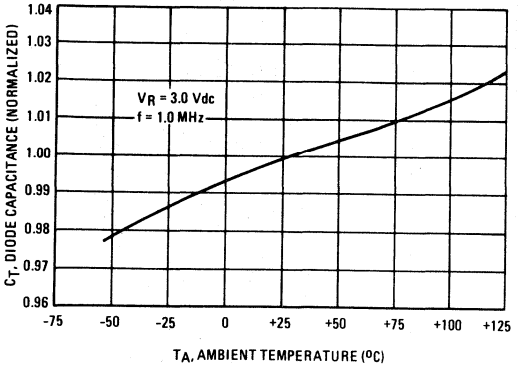


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_T measured at 3.0 Vdc divided by C_T measured at 25 Vdc.

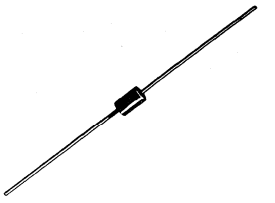
BY126
BY127

AXIAL LEAD MOUNTED RECTIFIERS

. . . intended for use in main rectifier applications, in television receivers.

SILICON RECTIFIER DIODES

650 & 1,250 VOLTS
1.0 AMP



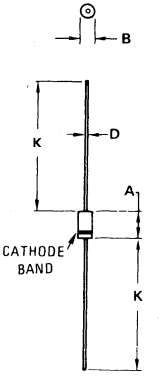
MAXIMUM RATINGS

Rating	Symbol	BY126	BY127	Unit
Peak Working Reverse Voltage	V_{RWM}	450	800	Volts
Peak Repetitive Reverse Voltage	V_{RRM}	650	1250	Volts
Non Repetitive Peak Reverse Voltage (t = 10 mS)	V_{RSM}	650	1250	Volts
Average Rectified Forward Current-Resistive Load (average over any 20 mS period) V_{RWM} = V_{RWM} Max V_{RWM} = 60 V	I_O	1.0 1.2		Amp Amp
Repetitive Peak Forward Current	I_{FRM}	10		Amp
Non Repetitive Peak Surge Current t = 10 mS-Half sine wave T_J = 150°C prior to surge	I_{FSM}	40		Amp
Storage Junction Temperature Range	T_{stg}	— 65 to + 150		°C
Junction Temperature Range	T_J	+ 150		°C

ELECTRICAL AND THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Forward Voltage I_F = 5 A, T_J = 25°C (see Note 1)	V_F	1.5			Volts
Reverse Current V_{RM} = V_{RRM} Max	I_R	10			μA

Note 1: Measured under pulsed conditions to avoid excessive dissipation.



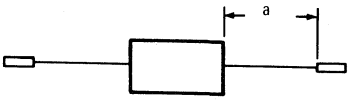
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

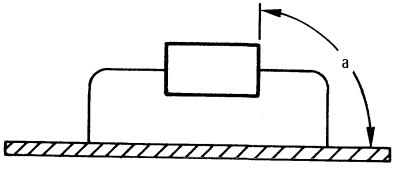
Does Not Confirm to DO-41 Outline

THERMAL RESISTANCE (Influence of mounting method)

The quoted values apply when no other leads run to the tie-points. If leads of other dissipating components share the same tie-points, the thermal resistance will be higher than that quoted.



1. Mounted to solder tags at a lead-length a = 10 mm. $R_{th\ j\text{-}a}$ = 60°C/W
2. Mounted to solder tags at a = maximum lead-length $R_{th\ j\text{-}a}$ = 70°C/W
3. Mounted on printed-wiring board at a = maximum lead-length $R_{th\ j\text{-}a}$ = 85°C/W
4. Mounted on printed-wiring board at a lead-length a = 10 mm. $R_{th\ j\text{-}a}$ = 95°C/W



SOLDERING AND MOUNTING NOTES

1. Soldered joints must be at least 5 mm from the seal.
2. The maximum permissible temperature of the soldering iron or bath is 300°C, it must be in contact with the joint for no more than 3 seconds.
3. Avoid hot spots due to handling or mounting; the body of the device must not come into contact with or be exposed to a temperature higher than 150°C.

Curves and characteristics of MOTOROLA series 1N4001... 1N4007 shall apply to BY126/BY127.

BY196 Series

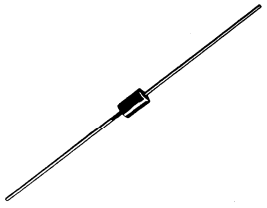
AXIAL LEAD MOUNTED RECTIFIERS

Featuring non snap off characteristics

. . . intended for use in amplifiers, switchmode power supplies, TV scan rectifiers and HF power supplies.

SILICON RECTIFIER DIODES

100, 200, 400, 800 VOLTS
1.2 AMP



MAXIMUM RATINGS

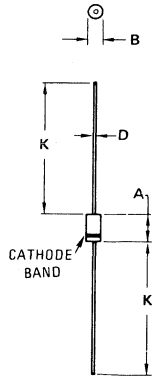
Rating	Symbol	BY196	BY197	BY198	BY199	Unit
Peak repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	800	Volts
Non-Repetitive Reverse Voltage	V_{RSM}	200	300	500	1000	Volts
Average Rectified Forward Current (Average over any 20 mS period)	I_{FAV}	1.2[1]				Amp
Repetitive Peak Forward Current	I_{FRM}	12				Amp
Non-Repetitive Peak Surge Current (t = 10 ms, half time wave, T_J = 75°C prior to surge)	I_{FSM}	70				Amp
Storage Junction Temperature	T_{stg}	— 40 to + 150				°C
Junction Temperature	T_J	+ 150				°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 10 mm from case.

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Max	Unit
Forward Voltage, I_F = 3 A; T_J = 25°C (see Note 2)	V_F		1.3	Volts
Reverse Current $V_R = V_{RRM}$, T_J = 25°C	I_R		10	μA
Capacitance at F = 1 MHz V_R = 150 V T_J = 25 to 125°C	C_d		4.0	pF
Reverse Recovery Time from I_F = 10 mA through I_R = 10 mA to I_R = 1 mA	t_{rr}		500	nS

Note 2: Measured under pulse conditions to avoid excessive dissipations.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

Does Not Conform to D0-41 Outline

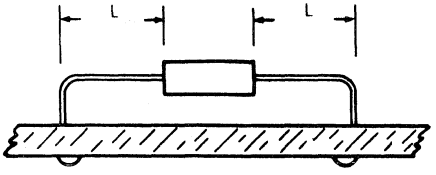
THERMAL RESISTANCE

Data shown for thermal resistance junction to ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

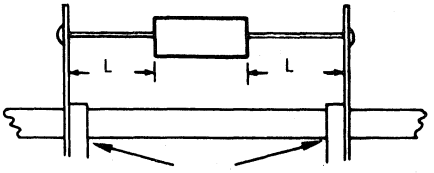
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

Mounting Method	Lead length, L (mm) 3.18	6.35	12.7	19.1	$R\theta_{JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3		40			°C/W

MOUNTING METHOD 1

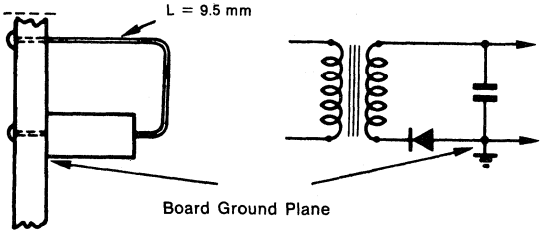


MOUNTING METHOD 2
Vector Pin mounting



MOUNTING METHOD 3

P.C. Board with 3.81 × 3.81 mm copper surface
L = 9.5 mm



Curves and characteristics of Motorola series MR810... MR818 shall apply to BY196... BY198

BY206
BY207

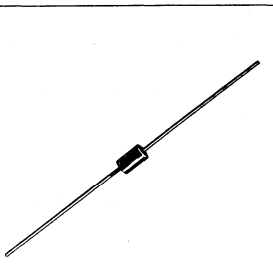
AXIAL LEAD MOUNTED RECTIFIERS

Featuring non snap off characteristics

. . . intended for use in amplifiers, switchmode power supplies, TV scan rectifiers and HF power supplies.

SILICON RECTIFIER DIODES

300-500 VOLTS
0.5 AMP



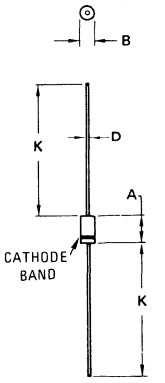
MAXIMUM RATING

Rating	Symbol	BY206	BY207	Unit
Peak repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	350	600	Volts
Non-Repetitive Reverse Voltage	V_{RSM}	450	800	Volts
Average Rectified Forward Current (Average over any 20 mS period)	I_{FAV}	0.5		Amp
Repetitive Peak Forward Current	I_{FRM}	5		Amp
Non-Repetitive Peak Surge Current (t = 10 ms - half sine wave - T_J = 125°C prior to surge)	I_{FSM}	15		Amp
Storage Junction Temperature	T_{stg}	— 65 to + 150		°C
Junction Temperature	T_J	+ 150		°C

ELECTRICAL AND THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Forward Voltage I_F = 2A T_J = 25°C (see Note 1)	V_F		1.3	Volts
Reverse Current $V_R = V_{RRM}$, T_J = 25°C $V_R = V_{RRM}$, T_J = 75°C	I_R		2 100	μA μA
Capacitance at F = 1 MHz V_R = 150V, T_J = 25°C to 125°C	C_d		4.0	pF
Reverse Recovery Time I_F = 400 mA to $V_R \geqslant$ 50 V with: $\frac{-dI}{dt}$ = 400 mA/μs, T_J = 25°C I_F = 10 mA to $V_R \geqslant$ 50 V with: $\frac{-dI}{dt}$ = 500 mA/μs, T_J = 25°C	t_{rr}		 1000 300	 nS nS
Reverse Recovery charge I_F = 400 mA to $V_R \geqslant$ 50 V with: $\frac{dt}{-dI}$ = 400 mA/μs	Q_S		60	nC

Note 1: Measured under pulse conditions to avoid excessive dissipation.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

Does Not Conform to DO-41 Outline

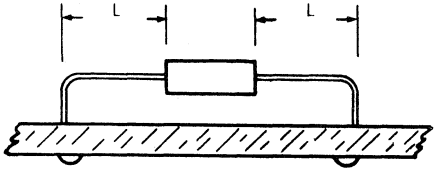
THERMAL RESISTANCE

Data shown for thermal resistance junction to ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

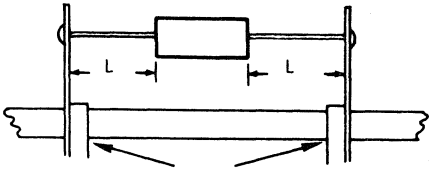
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

Mounting Method	Lead length, L (mm) 3.18	6.35	12.7	19.1	$R\theta_{JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3		40			°C/W

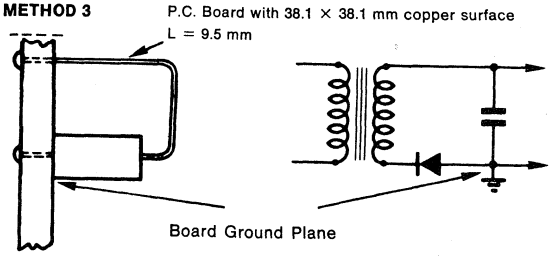
MOUNTING METHOD 1



MOUNTING METHOD 2
Vector Pin mounting



MOUNTING METHOD 3



BY210-400 Series

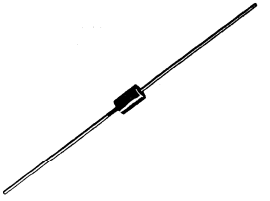
AXIAL LEAD MOUNTED RECTIFIERS

Featuring non snap-off characteristics

. . . intended for use in amplifiers, switchmode power supplies, TV scan rectifiers and HF Power supplies

SILICON RECTIFIER DIODES

400, 600, 800 VOLTS



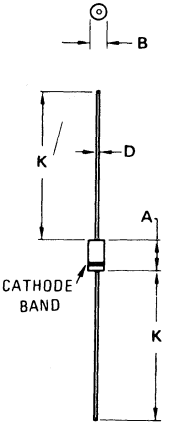
MAXIMUM RATINGS

Rating	Symbol	BY210 400	BY210 600	BY210 800	Unit
Peak repetitive reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	400	600	800	VOLTS
Non-Repetitive Reverse Voltage	V_{RSM}	500	800	1000	VOLTS
Average Rectified Forward	I_{FAV}	1			AMP
Repetitive Peak Forward Current	I_{FRM}	5			AMP
Non-Repetitive Peak Surge Current	I_{FSM}	30			AMP
Storage Junction Temp. range	T_{stg}	-40 to −150			°C
Junction Temperature	T_J	−150			°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Typ	Max	Unit
Forward Voltage – I_F = 5A T_J = 25°C (see note 1)	V_F		1.4	VOLTS
Reverse Current $V_R = V_{RRM} - T_J$ = 25°C $V_R = V_{RRM} - T_J$ = 125°C	I_R		10 100	μA μA
Capacitance at F = 1 MHz V_R = 100 V	C_d	4.5		
Reverse Recovery Time (when switched from I_F = 50 mA to V_R = 50 V measured at I_R = 5.0 mA RL = 100 Ω)	t_{rr}		300	nS

Note 1 – Measured under pulse conditions to avoid excessive dissipation.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
Does Not Conform to DO-41 Outline.

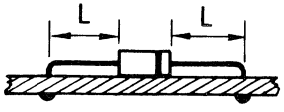
THERMAL RESISTANCE

Data shown for thermal resistance junction to ambien (θ_{JA}) for the mounting shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR θ_{JA} IN STILL AIR

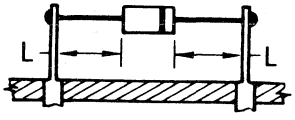
Mounting Method	Lead length, L (mm)				$R\theta_{JA}$
	0.318	0.635	1.270	1.91	
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1



MOUNTING METHOD 2

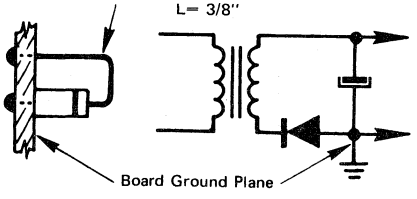
Vector Pin mounting



MOUNTING METHOD 3

P.C. Board with 3.81 x 3.81 mm copper surface

L= 3/8"



Curves and characteristics of Motorola series MR810 ... MR818 shall apply to BY210 ... 400 Series.

Designers Data Sheet

MINIATURE SIZE, AXIAL LEAD MOUNTED STANDARD RECOVERY POWER RECTIFIERS

. . . designed for use in T.V. line deflection, power supplies and other applications having need of a device woth the following features:

- High Current to Small Size
- High Surge Current Capability
- Low Forward Voltage Drop
- Void-Free Economical Plastic Package
- Available in Volume Quantities

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol		BY 251	BY 252	BY 253	BY 254	BY 255	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R		200	400	600	800	1300	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}		250	450	650	850	1350	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 95°C, PC Board Mounting) (1) (EIA Standard Conditions L – 1/32", T_L = 85°C)	I_O	← 3.0 → ← 8.0 →						Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	← 100 → (one cycle)						Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	← -65 to +175 →						°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mounting, See Note 2 on Page 4).	$R_{\theta JA}$	28	°C/W

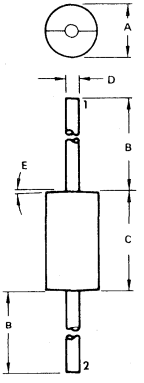
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (3) (i_F = 9.4 Amp, T_J = 175°C) (i_F = 3.0 Amp, Tj = 25°C)	v_F	– –	0.9 1.04	1.0 1.1	Volts
Reverse Current (rated dc voltage) (3) Tj = 25°C Tj = 100°C	I_R	– –	0.1 2.8	10 500	μA

(1) Derate for reverse power dissipation. See Note on Page 2.
(2) Derate as shown in Figure 1.
(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
▲Trademark of Motorola Inc.

STANDARD RECOVERY POWER RECTIFIERS

200 - 1300 VOLTS
3 AMPERE



	INCHES		MILLIMETERS	
A	0.190	0.210	4.83	5.33
B	1.062	1.072	26.97	27.23
C	0.370	0.380	9.40	9.65
D	0.048	0.052	1.22	1.32
E	20°		20°	

CASE 267

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 200 volts. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (175°C or the temperature at which thermal runaway occurs, whichever is lowest.)

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figure solves for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where $T_J = 175°C$, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figure 1 as a difference in the rate of change of the slope in the vicinity of 165°C. The data of Figure 1 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the rectifiers reverse characteristics.

Example: Find $T_{A(max)}$ for BY 255 operated in a 400 Volt dc supply using a full wave center-tapped circuit with capacitive filter such that $I_{DC} = 6.0$ A, ($I_{F(AV)} = 3.0$ A), $I_{(PK)}/I_{(AV)} = 10$, Input Voltage = 283 V(rms) (line to center tap), $R_{\theta JA} = 28°C/W$.

Step 1: Find $V_{R(equiv)}$. Read F = 1.11 from Table 1 ∴
$V_{R(equiv)} = 1.41)(283)(1.11) = 444$ V

Step 2: Find T_R from Figure 1. Read $T_R = 167°C$ @ $V_R = 444$ V & $R_{\theta JA} = 28°C/W$.

Step 3: Find $P_{F(AV)}$ from Figure 8. Read $P_{F(AV)} = 4$ W
@ $\frac{I_{PK}}{I_{AV}} = 10$ & $I_{F(AV)} = 3.0$ A

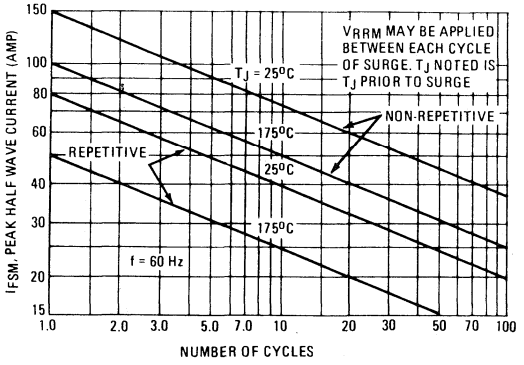
Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)} = 167-(28)(4) = 55°C$.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave Center-Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.45	1.11	0.45	0.55	0.90	1.11
Square Wave	0.61	1.22	0.61	0.61	1.22	1.22

*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}.

FIGURE 2 – MAXIMUM SURGE CAPABILITY



CURRENT DERATING

(Reverse Power Loss Neglected)

FIGURE 3 – PC BOARD MOUNTING

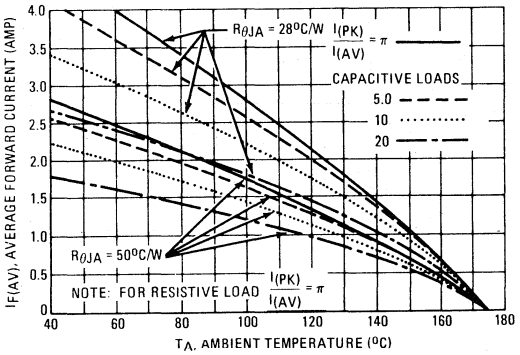


FIGURE 4 – SEVERAL LEAD LENGTHS

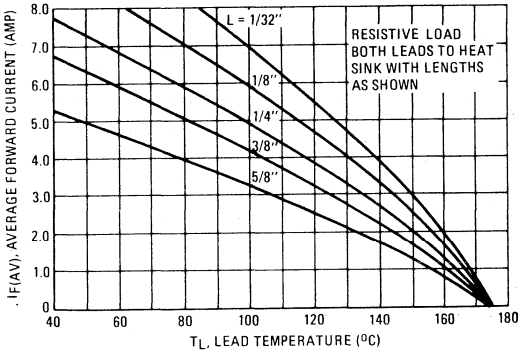


FIGURE 5 – 1/8" LEAD LENGTH

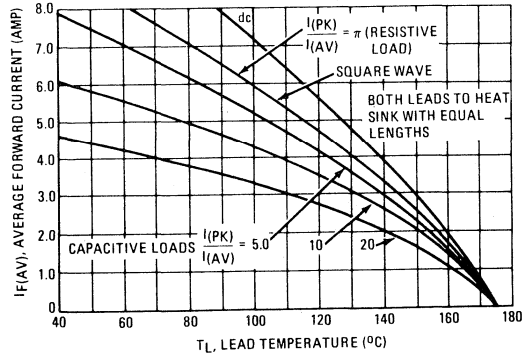


FIGURE 6 – MAXIMUM FORWARD VOLTAGE

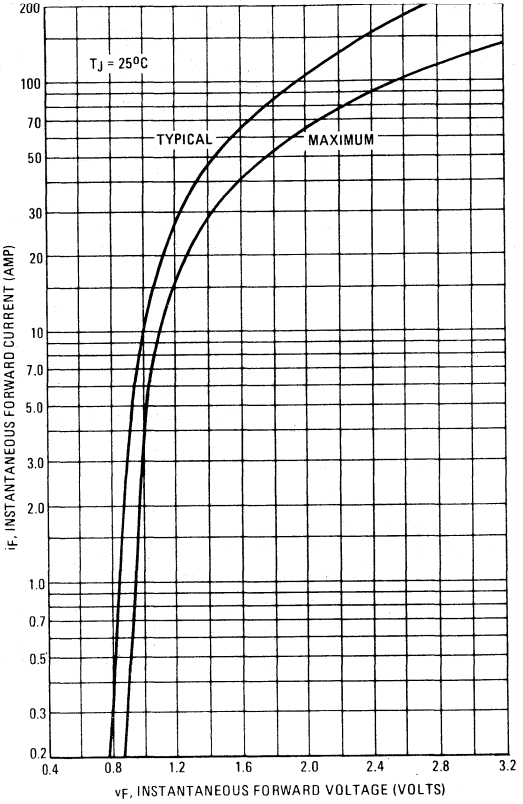


FIGURE 7 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

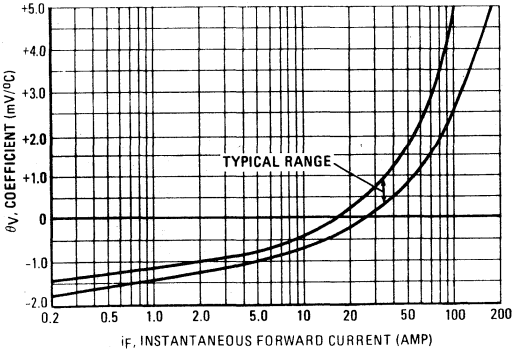


FIGURE 8 – FORWARD POWER DISSIPATION

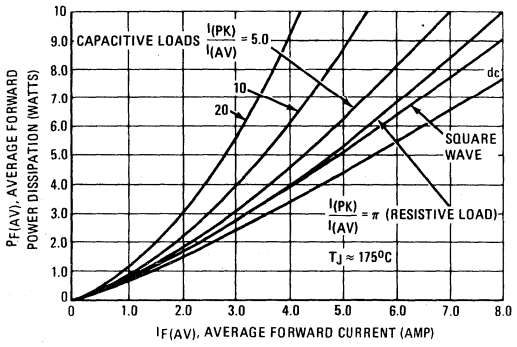
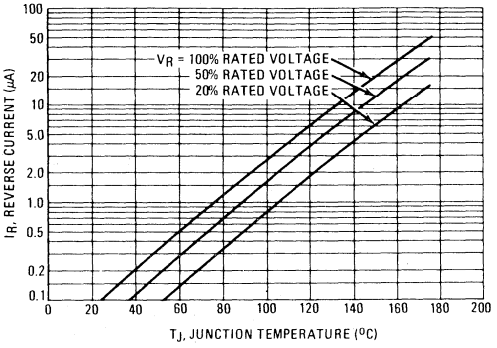


FIGURE 9 – TYPICAL REVERSE CURRENT



THERMAL CHARACTERISTICS

FIGURE 10 – THERMAL RESPONSE

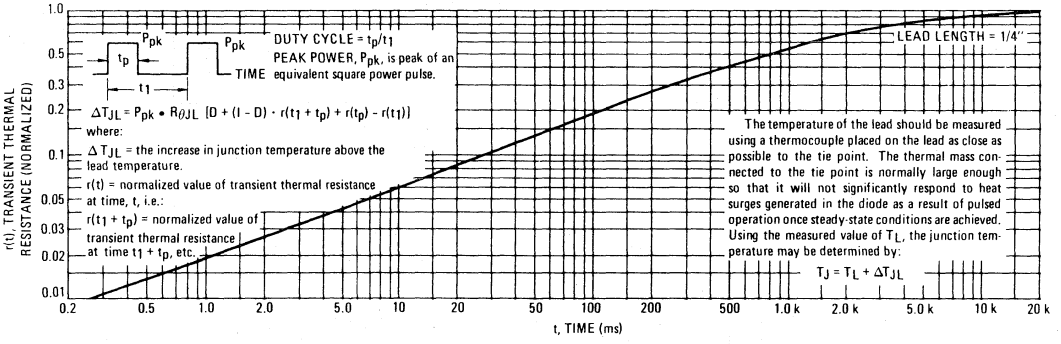
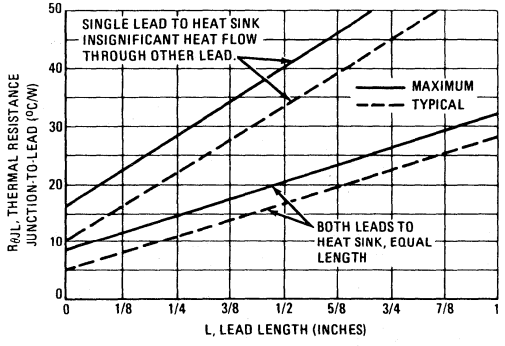


FIGURE 11 – STEADY-STATE THERMAL RESISTANCE



NOTE 2 – AMBIENT MOUNTING DATA

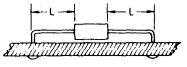
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

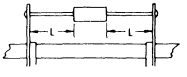
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface

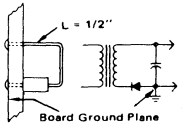
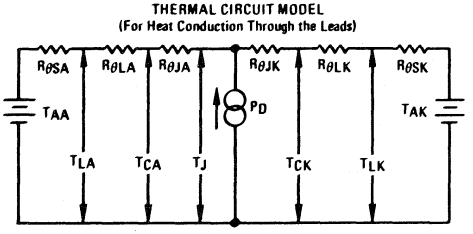


FIGURE 12 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)
Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} \approx R_{\theta JL}$

TYPICAL DYNAMIC CHARACTERISTICS
(T_J = 25°C)

FIGURE 13 – FORWARD RECOVERY TIME

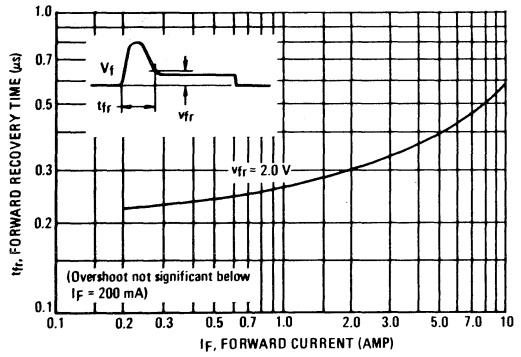


FIGURE 14 – REVERSE RECOVERY TIME

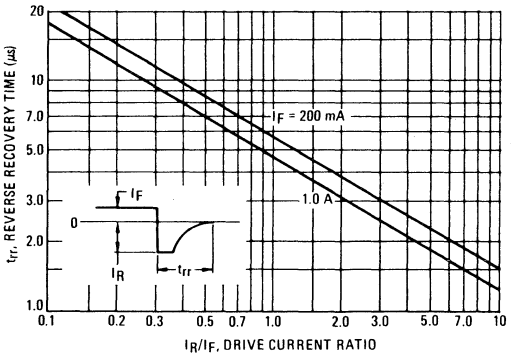


FIGURE 15 – RECTIFICATION WAVEFORM EFFICIENCY

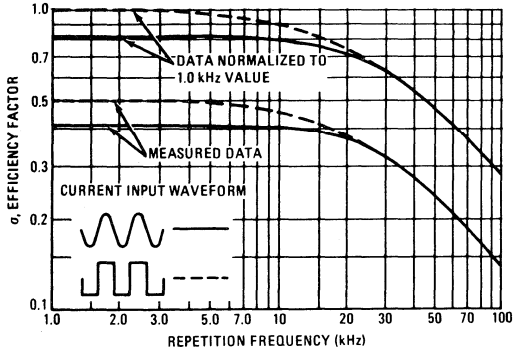
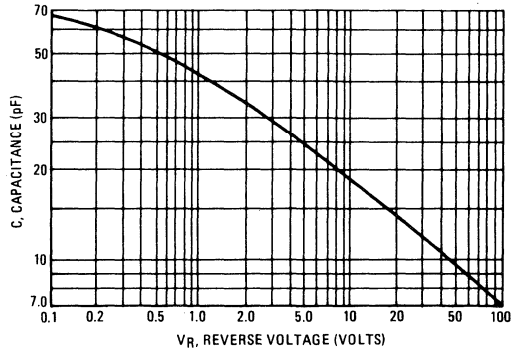
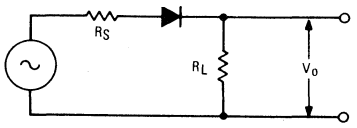


FIGURE 16 – JUNCTION CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 17 – SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 15 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_{o(dc)}}{R_L}}{\frac{V^2_{o(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{o(dc)}}{V^2_{o(ac)} + V^2_{o(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 14) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 15.

It should be emphasized that Figure 15 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the figure.

AXIAL LEAD MOUNTED RECTIFIERS

Featuring non snap off characteristics

. . . intended for use in amplifiers, switchmode power supplies, TV scan rectifiers and HF power supplies.

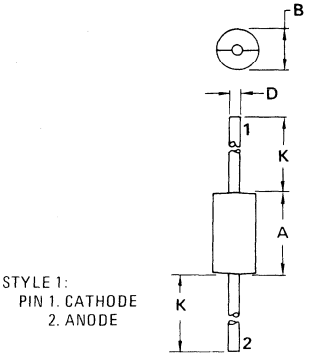
SOFT/FAST RECOVERY SILICON RECTIFIER DIODES

100-1300 VOLTS
2 AMPERES

MAXIMUM RATING

Rating	Symbol	BY296	BY297	BY298	BY299	BY400	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	800	1300	V
Non Repetitive Reverse Voltage	V_{RSM}	200	300	500	1000	1400	V
Average Rectified Forward Current (Average over any 20 mS period)	I_{FAV}	2.0[1]					A
Repetitive Peak Forward Current	I_{FRM}	15					A
Non Repetitive Peak Surge Current (t = 10 ms, half sine wave, (T_j = 25 °C prior to surge)	I_{FSM}	100					A
Storage Junction Temperature	T_{stg}	−40 to +150					°C
Junction Temperature	T_j	+150					°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 10 mm from case.



STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Max.	Unit
Forward Voltage (I_F = 3 A, T_j = 25 °C)[2]	V_F		1.3	Volts
Reverse Current (V_R = V_{RRM}, T_J = 25 °C) (V_R = V_{RRM}, T_J = 125 °C)	I_R		10 300	μA μA
Reverse Recovery Time from I_F = 10 mA through I_R = 10 mA to I_R = 1 mA	t_{rr}		500	nS

[2] Measured under pulse conditions to avoid excessive dissipations.

THERMAL RESISTANCE

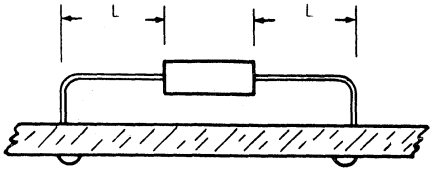
Data shown for thermal resistance junction to ambient ($R\theta_{JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R\theta_{JA}$ IN STILL AIR

Mounting Method	Lead length, L (mm) 3.18	6.35	12.7	19.1	$R\theta_{JA}$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3		28			°C/W

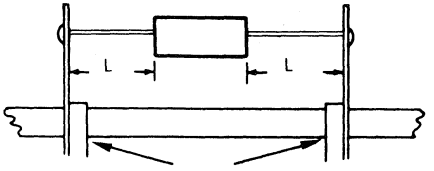
MOUNTING METHOD 1

P.C. Board where available copper surface area is small



MOUNTING METHOD 2

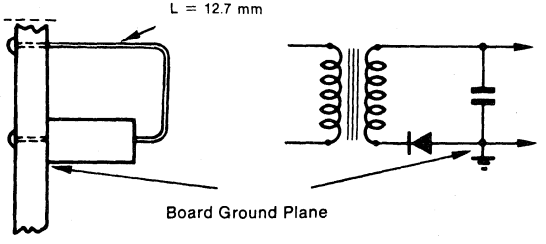
Vector Pin mounting



Vector Push In Terminals T-28

MOUNTING METHOD 3

P.C. Board with 38.1 × 38.1 mm copper surface
L = 12.7 mm



Board Ground Plane

BY330 thru BY334
BY336 thru BY339

Designers▲ Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED SOFT RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 500 nanoseconds providing high efficiency at frequencies to 250 kHz.

SOFT RECOVERY POWER RECTIFIERS

50-1500 Volts
1 AMPERE

DESIGNER'S DATA FOR "WORST CASE" CONDITIONS

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing device characteristic boundaries – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Ratings	Symbol	BY 330	BY 331	BY 332	BY 333	BY 334	BY 336	BY 337	BY 338	BY 339	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	300	400	500	800	1000	1500	Volts
Non Repetitive Peak Reverse Voltage	V_{RSM}	100	200	300	400	500	800	1000	1200	1600	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	210	280	420	560	700	1200	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75 °C)	I_O	◄ 1.0 ►									Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75 °C)	I_{FSM}	◄ 40 ►									Amps
Operating Junction Temperature Range	T_J	◄ –65 to +150 ►									°C
Storage Temperature Range	T_{stg}	◄ –65 to +175 ►									°C

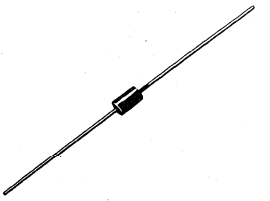
THERMAL CHARACTERISTICS

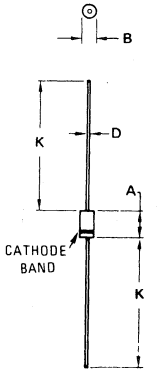
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

Characteristic	Symbol	Min	Typ	Max	Unit
Forward Voltage (I_F = 1.0 Amp, T_A = 25°C)	V_F	–	1.0	1.25	Volts
Reverse Current (rated dc voltage) T_A = 25°C T_A = 100°C	I_R	– –	1.0 50	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	t_{rr}	–	500	750	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc)(Figure 21)	$I_{RM(REC)}$	–	–	3.0	Amp





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are tin plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

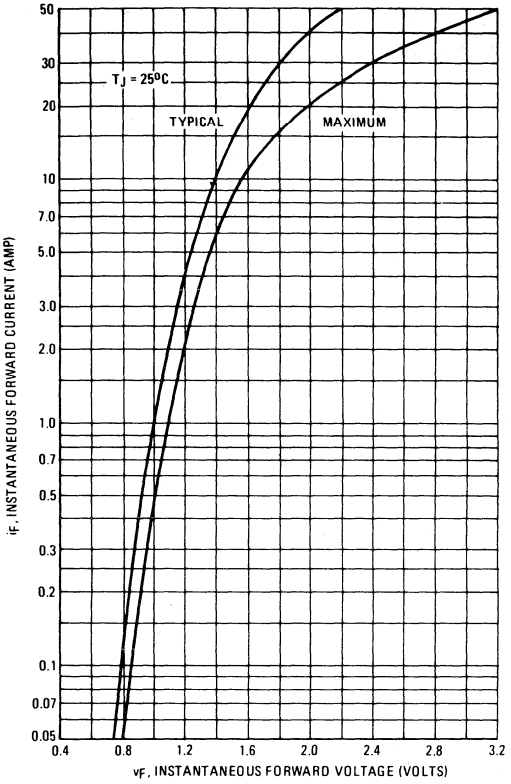


FIGURE 1 – FORWARD VOLTAGE

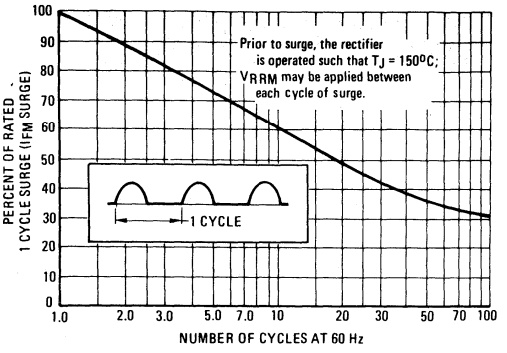


FIGURE 2 – MAXIMUM SURGE CAPABILITY

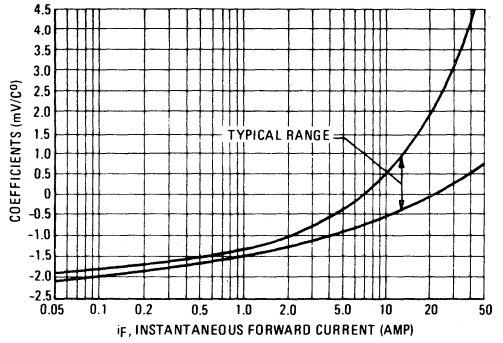


FIGURE 3 – TEMPERATURE COEFFICIENT

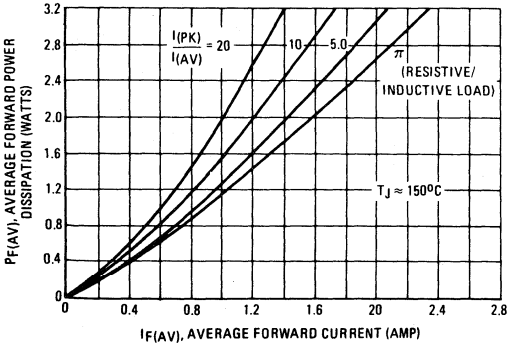


FIGURE 4 – FORWARD POWER DISSIPATION

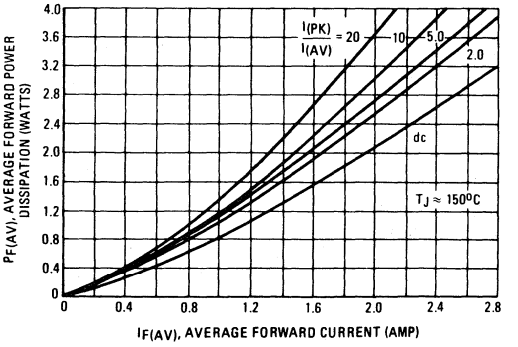


FIGURE 5 – FORWARD POWER DISSIPATION

MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

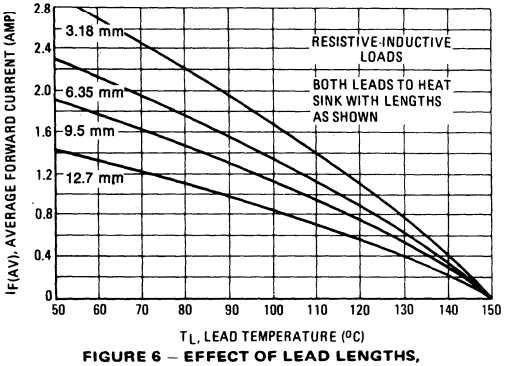


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

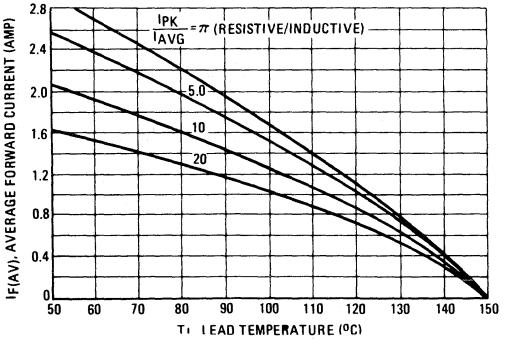


FIGURE 8 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

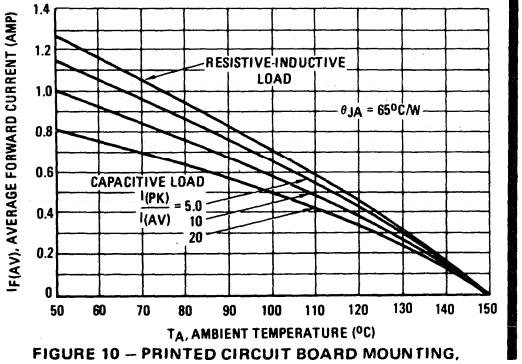


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

SQUARE WAVE INPUT

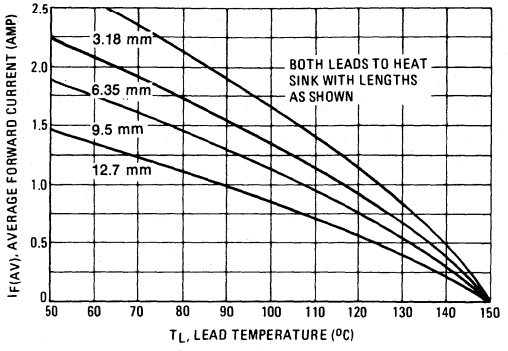


FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

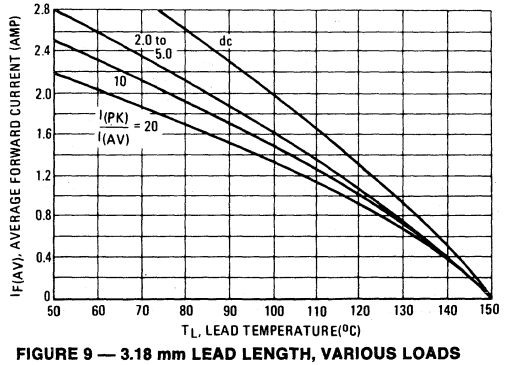


FIGURE 9 — 3.18 mm LEAD LENGTH, VARIOUS LOADS

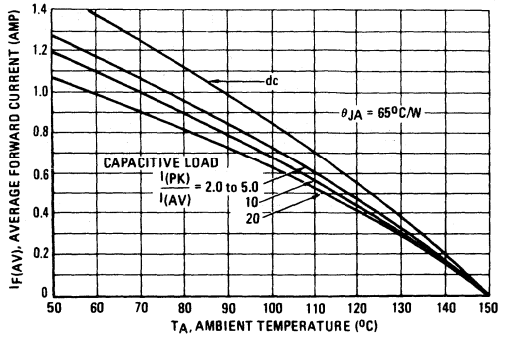


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

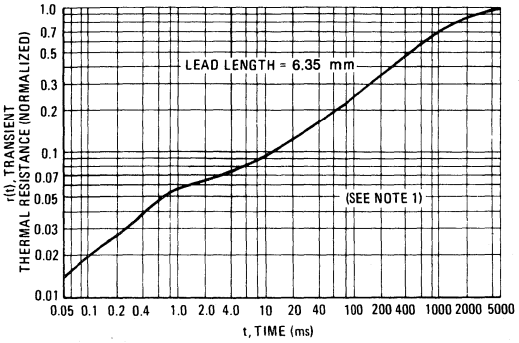


FIGURE 12 – THERMAL RESPONSE

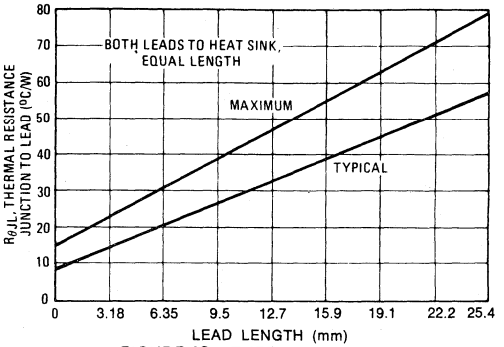
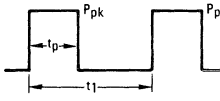


FIGURE 13 – THERMAL RESISTANCE

NOTE 1



DUTY CYCLE, D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

r ($t_1 + t_p$) = normalized value of transient thermal resistance at time $t_1 + t_p$.

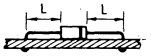
NOTE 2

Data shown for thermal resistance junction to ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

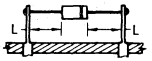
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L(mm) 3.81	6.35	12.7	19.1	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

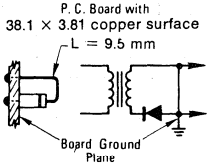


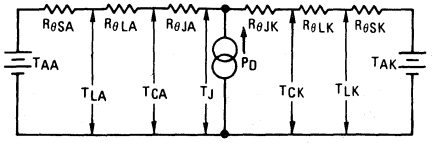
MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3





Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$T_L = 150^{\circ} - \Delta T_{JL}$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \bullet P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

FIGURE 14 – THERMAL CIRCUIT MODEL

TYPICAL DYNAMIC CHARACTERISTICS

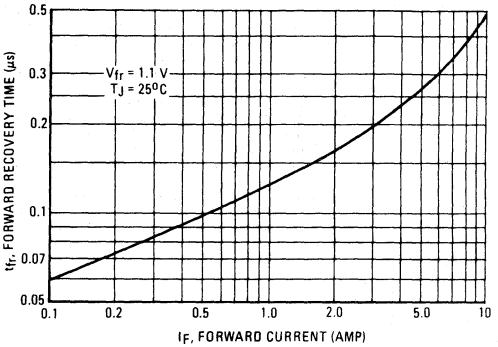


FIGURE 15 – FORWARD RECOVERY TIME

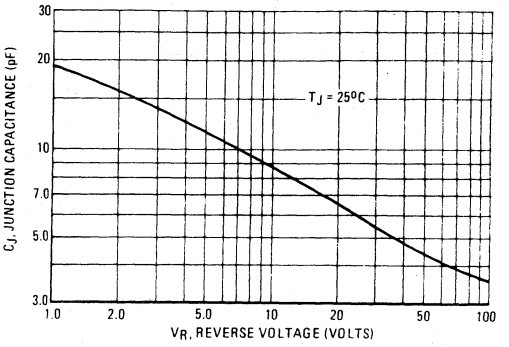


FIGURE 16 – JUNCTION CAPACITANCE

TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

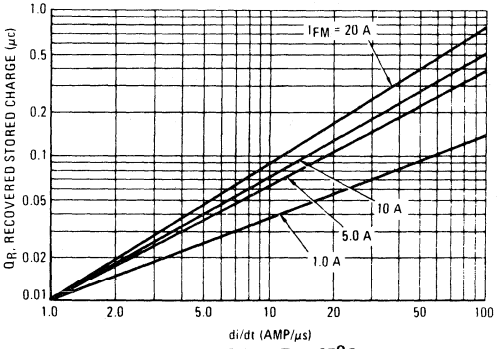


FIGURE 17 – T_J = 25°C

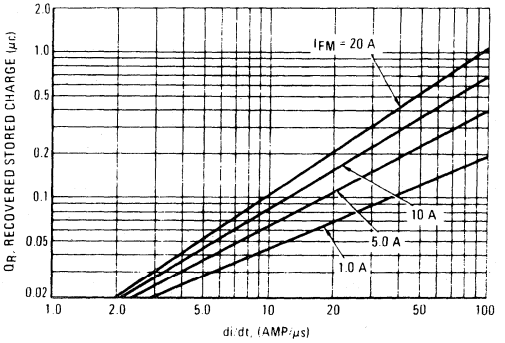


FIGURE 18 – T_J = 75°C

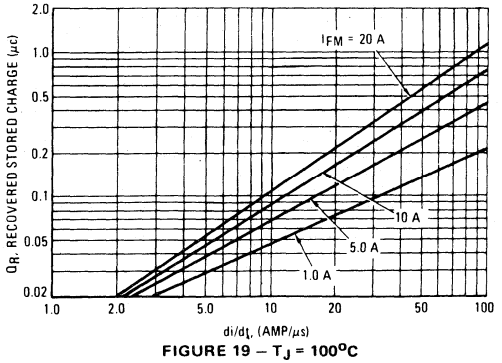


FIGURE 19 – T_J = 100°C

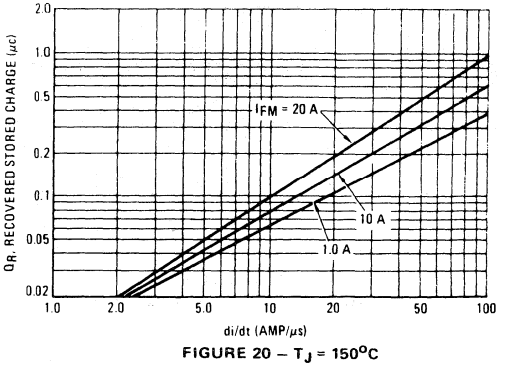


FIGURE 20 – T_J = 150°C

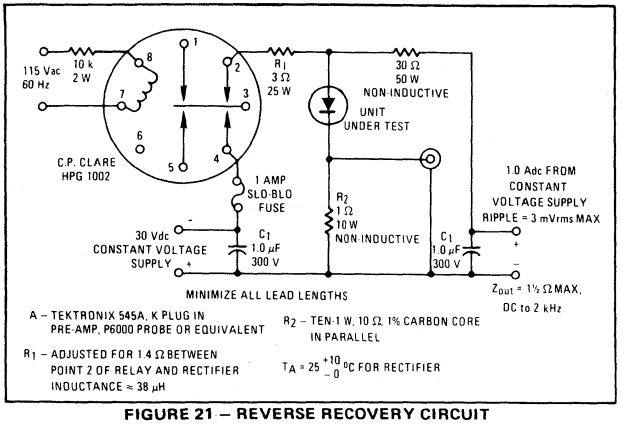


FIGURE 21 – REVERSE RECOVERY CIRCUIT

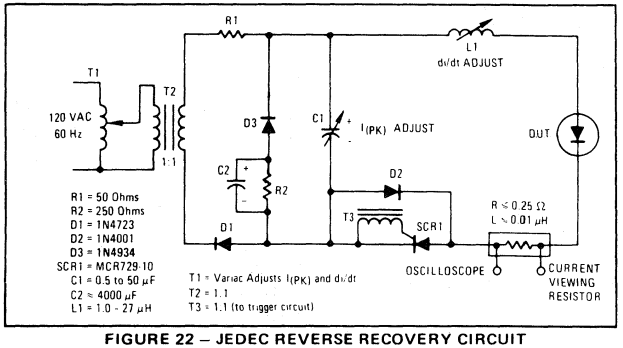


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT

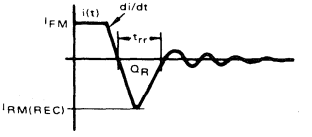
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

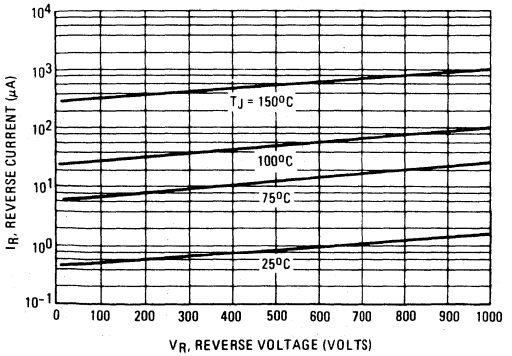


FIGURE 23 – TYPICAL REVERSE LEAKAGE

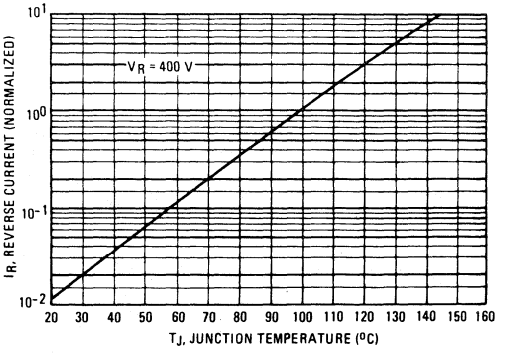


FIGURE 24 – TYPICAL REVERSE LEAKAGE

BY601 thru BY608

"SURMETIC"▲ RECTIFIERS

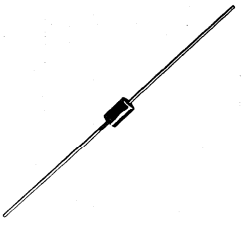
. . . subminiature size, axial lead mounted rectifiers for general-purpose main rectifier applications in TV/HiFi sets and domestic appliances.

Designers Data for "Worst Case" Conditions

The Designers▲ Data Sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

LEAD MOUNTED SILICON RECTIFIERS

50 - 1250 VOLTS
DIFFUSED JUNCTION



MAXIMUM RATINGS

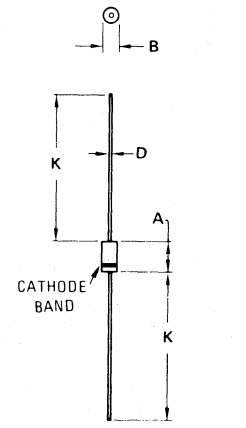
Rating	Symbol	BY601	BY602	BY603	BY604	BY605	BY606	BY607	BY608	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	1250	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 50 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	1500	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	850	Volts
Average Rectified Forward Current (single phase, resistive load, 50 Hz, see Figure 8, T_A = 75 °C)	I_O	1.5								Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	I_{FSM}	50 (for 1 cycle)								Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175								°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (I_F = 1.5 Amp, T_J = 25 °C) Figure 1	V_F	1.0	1.15	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25 °C T_J = 100 °C	I_R	 0.05 1.0	 10 50	μA

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded.
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350 °C, 1.27 cm from case for 10 seconds at 2.27 kg tension.
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable.
POLARITY: Cathode indicated by color band.
WEIGHT: 0.40 Grams (approximately).



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
Does Not Conform to DO-41 Outline.

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE

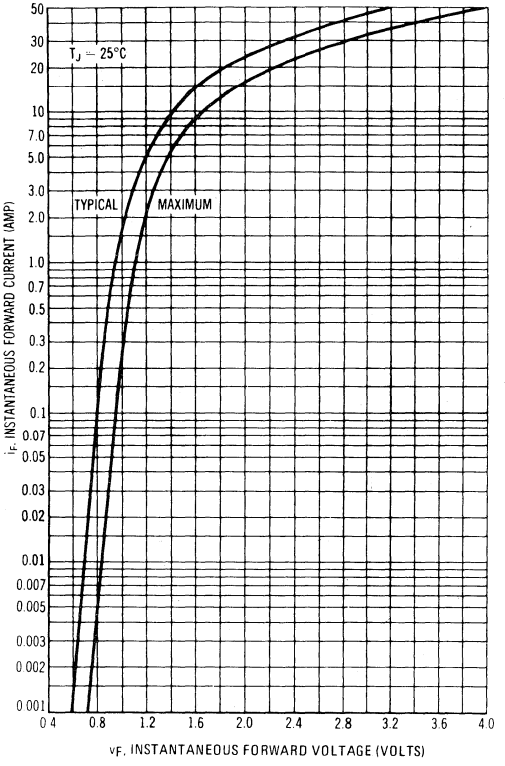


FIGURE 2 – NON REPETITIVE SURGE CAPABILITY

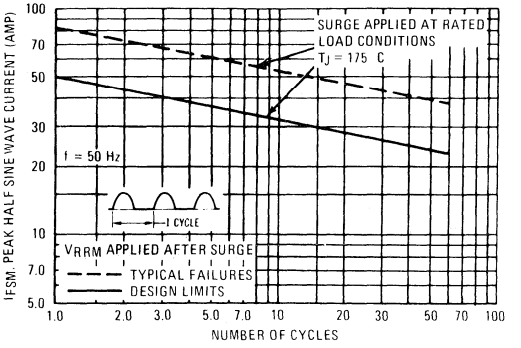


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

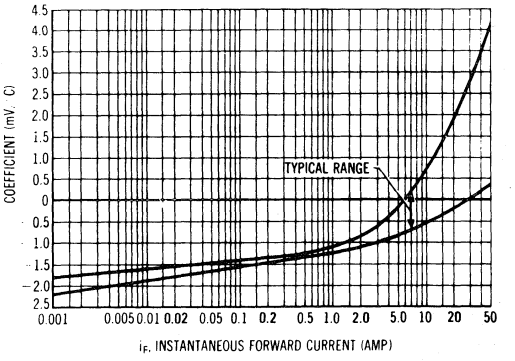
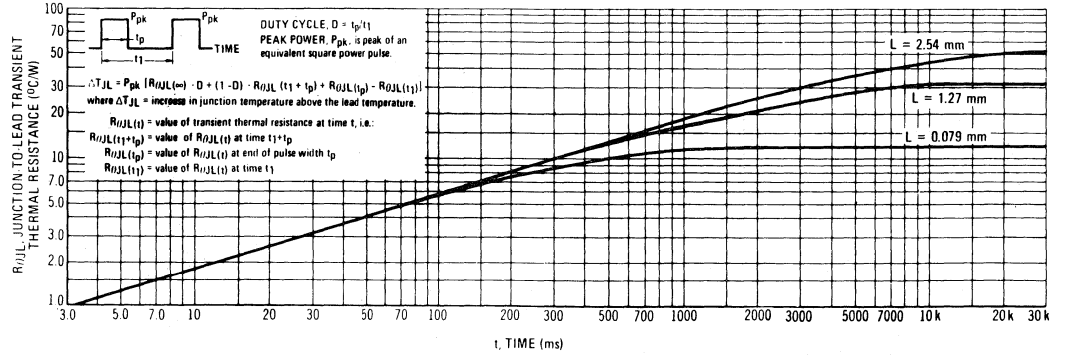


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE



The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

CURRENT DERATING DATA

FIGURE 5 – FORWARD POWER DISSIPATION

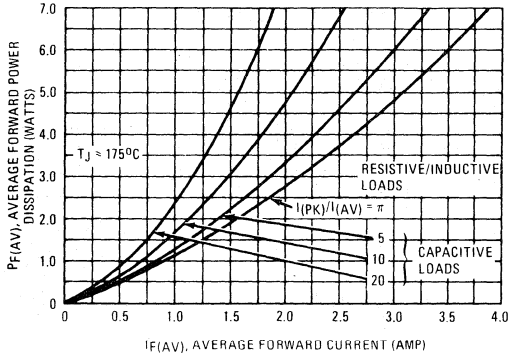


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

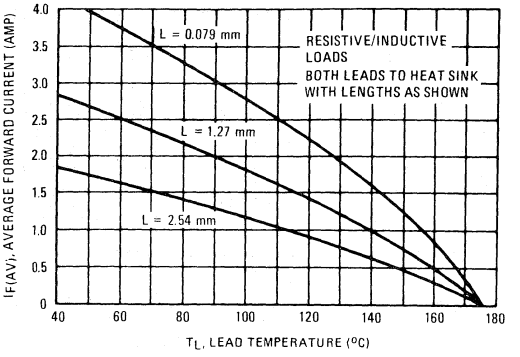


FIGURE 7 – 1.27 mm LEAD LENGTH, VARIOUS LOADS

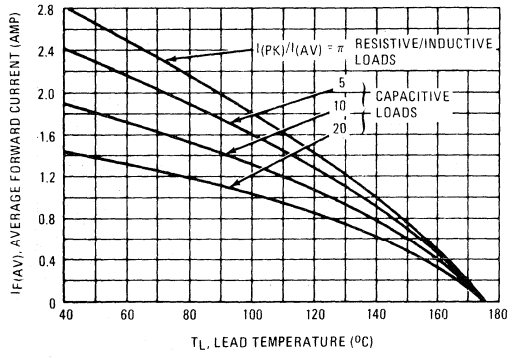


FIGURE 8 – PRINTED CIRCUIT BOARD MOUNTING VARIOUS LOADS

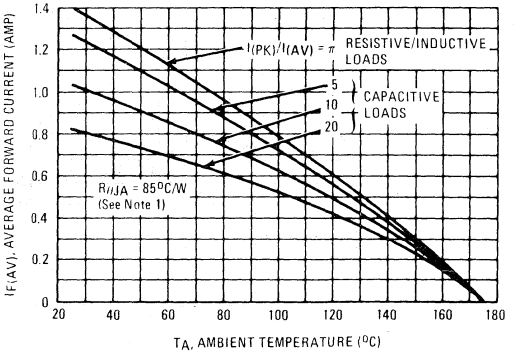
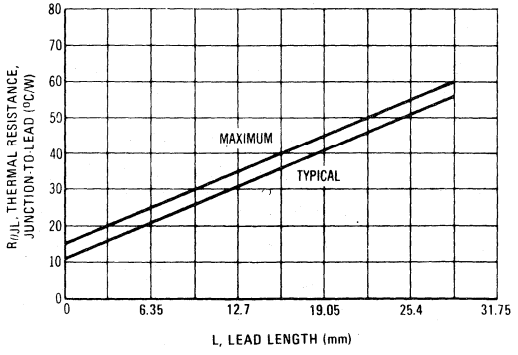


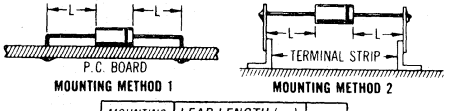
FIGURE 9 – STEADY-STATE THERMAL RESISTANCE



NOTE 1

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR



MOUNTING METHOD 1 **MOUNTING METHOD 2**

MOUNTING METHOD	LEAD LENGTH (cm)			$R_{\theta JA}$
	0.079	1.27	2.54	
1	—	75	85	C/W
2	55	72	85	C/W

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 10 – FORWARD RECOVERY TIME

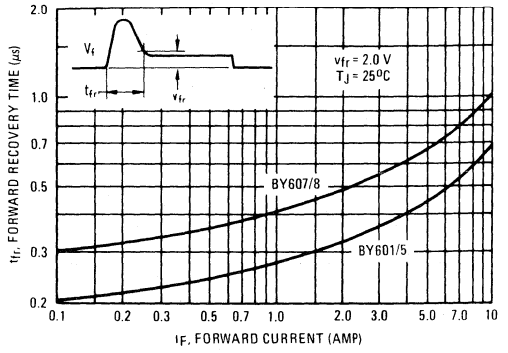


FIGURE 11 – REVERSE RECOVERY TIME

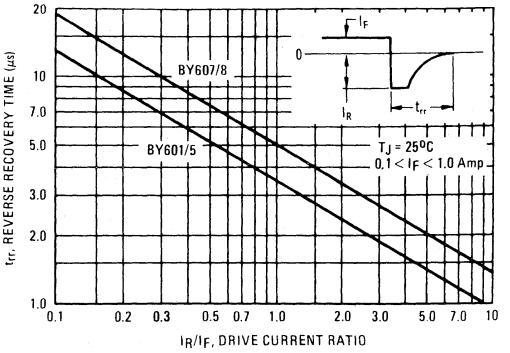


FIGURE 12 – JUNCTION CAPACITANCE

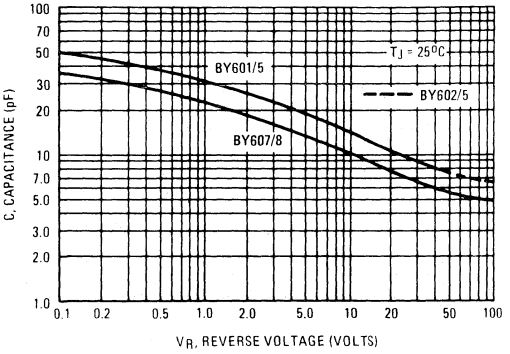


FIGURE 13 – RECTIFICATION WAVEFORM EFFICIENT FOR SINE WAVE

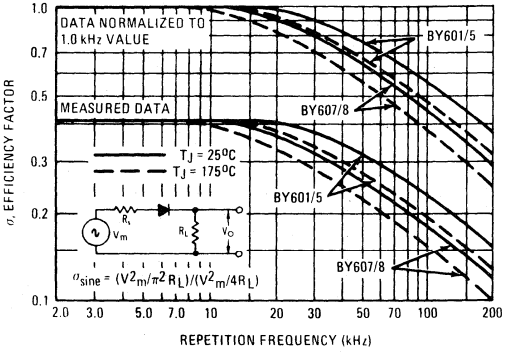
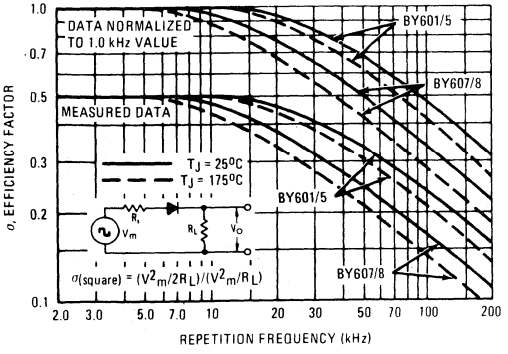


FIGURE 14 – RECTIFICATION WAVEFORM EFFICIENCY FOR SQUARE WAVE



RECTIFIER EFFICIENCY NOTE

The rectification efficiency factor σ shown in Figures 13 and 14 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \bullet 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \bullet 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes 40%; for a square wave input of amplitude V_m, the efficiency factor becomes 50%. (A full wave circuit has twice these efficiencies).

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 11) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current thereby reducing the value of the efficiency factor σ, as shown in Figures 13 and 14.

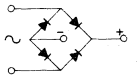
It should be emphasized that Figures 13 and 14 show waveform efficiency only; they do not account for diode losses. Data was obtained by measuring the ac component of V_O with a true rms voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the Figures.

BYW20 Series

RECTIFIER ASSEMBLY

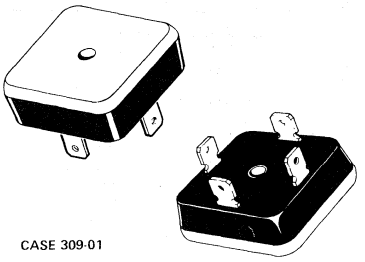
. . . utilizing individual void-free molded MR2500 Sries rectifiers, interconnected and mounted on an electrically isolated aluminum heat sink by a high thermal-conductive epoxy resin.

- 400 Ampere Surge Capability
- Electrically Isolated Base (Isolation Breakdown Voltage 2.5 KV).
- Fast Recovery Available on Request
- Cost Effective in Lower Current Applications
- Maximum Power Dissipation 25 Watts



SINGLE-PHASE FULL-WAVE BRIDGE

15 AMPERES
50-1000 VOLTS



CASE 309-01

MAXIMUM RATINGS

Rating (Per Diode)	Symbol	BYW 20	BYW 21	BYW 22	BYW 24	BYW 26	BYW 28	BYW 79	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	Vdc	 30 50	 62 100	 124 200	 250 400	 380 600	 500 800	 630 1000	Volts
Sine Wave RMS Input Voltage	V_R(RMS)	35	70	140	280	420	560	700	Volts
Average Rectifier Forward Current (Single phase bridge, resistive load, 50 Hz, T_C = 55 °C	I_O	15							Amp
Non-Repetitive Peak Surge Current applied (Surge at rated load conditions)	I_{FSM}	400							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175							°C

THERMAL CHARACTERISTICS (Total Bridge)

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.1	2.75	° C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (I_F = 24 A)	V_F	–	0.9	1.0	Volts
Reverse Current (Per Diode) (Rated V_R)	I_R	–	–	0.10	mA

MECHANICAL CHARACTERISTICS

CASE: Plastic case with electrically isolated aluminum base.

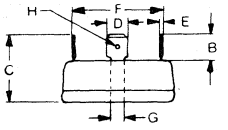
POLARITY: Terminal designation embossed on case:
+ DC output,
– DC output,
AC not marked.

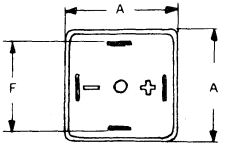
MOUNTING POSITION: Bolt down. Highest heat transfer efficiency accomplished through the surface opposite the terminals. Use silicon grease on mounting surface for maximum heat transfer.

WEIGHT: 40 grams (approx.)

TERMINALS: Suitable for fast-on connections. Readily solderable, corrosion resistant. Soldering recommended for applications greater than 15 Amperes.

MOUNTING TORQUE: 0,23 Kg-m. Max.





Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.368	1.387	34.75	35.25
B	.344	.364	8.75	9.25
C	.836	.875	21.25	22.25
D	.244	.251	6.20	6.40
E	.030	.032	0.77	0.83
F	1.102	1.125	28.00	28.60
G	.165	.177	4.20	4.50
H	.064	.068	1.65	1.75

NOTES
1. Hole is counter sunk for # 6 socket head screw.
2. Dim. "B", "C", "D", "E" and "H" are typical.

FIGURE 1 – FORWARD VOLTAGE

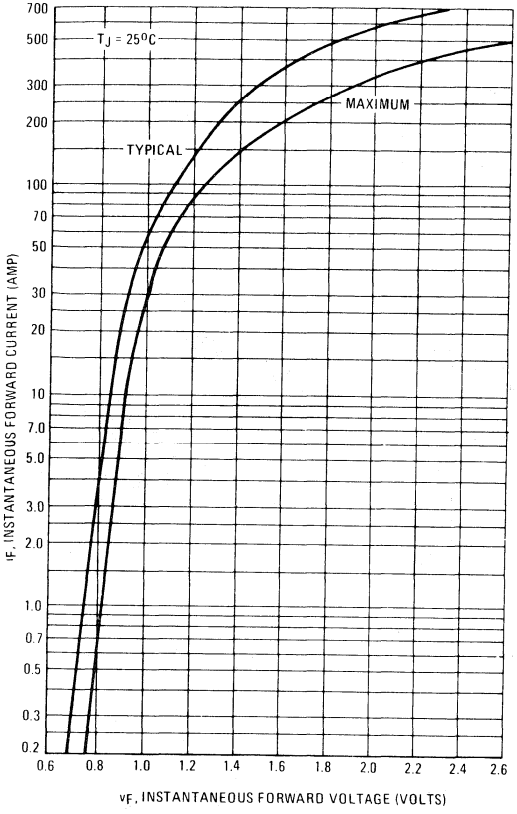


FIGURE 2 – NON REPETITIVE SURGE CURRENT

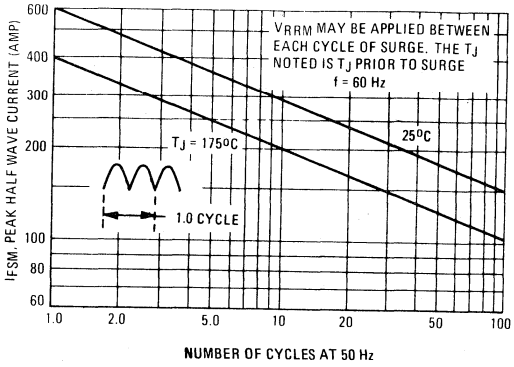


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

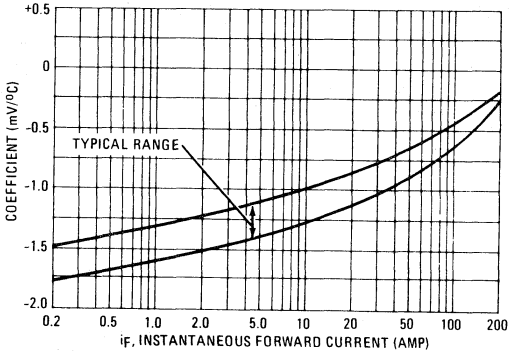


FIGURE 4 – CURRENT DERATING

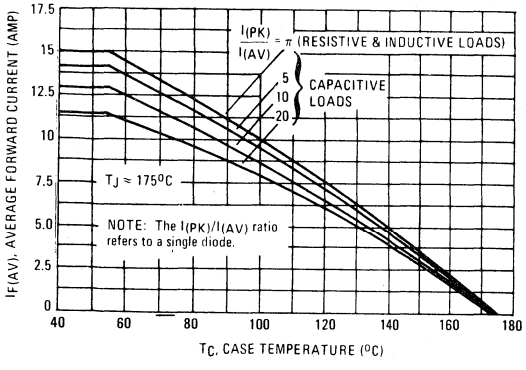


FIGURE 5 – FORWARD POWER DISSIPATION

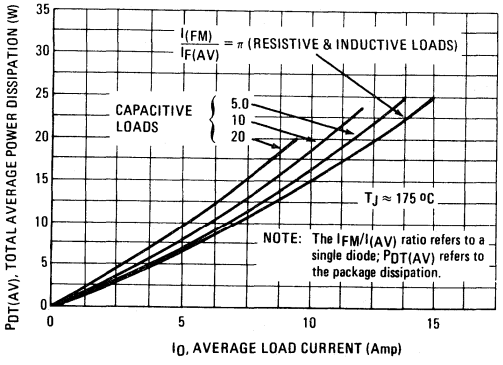
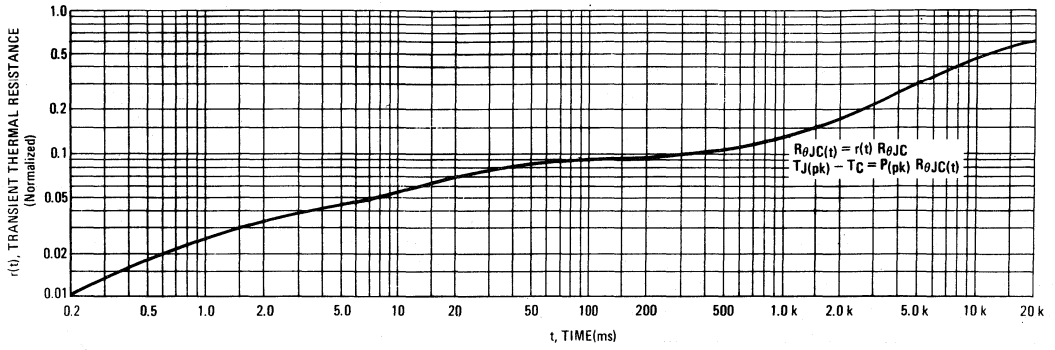
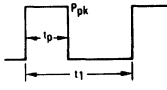


FIGURE 6 – TYPICAL THERMAL RESPONSE



NOTE 1



DUTY CYCLE, D = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended.

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see the outline drawing on page 1). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \bullet R_{\theta JC} [D + (1 - D) \bullet r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 8, i.e.,
$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

FIGURE 7 – CAPACITANCE

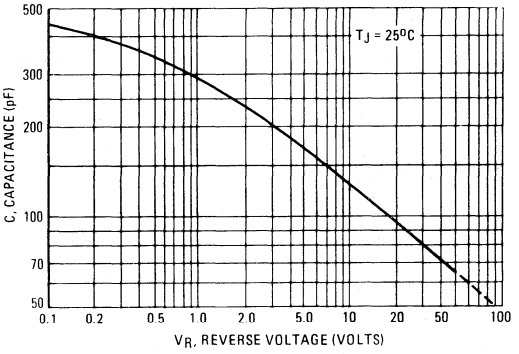


FIGURE 8 – FORWARD RECOVERY TIME

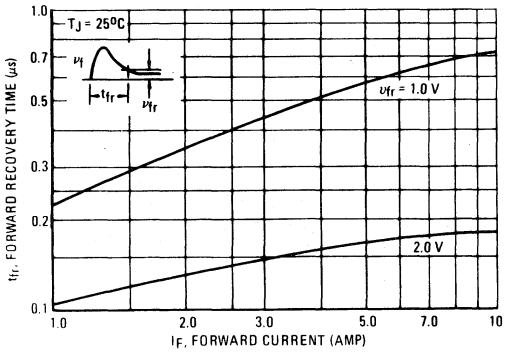
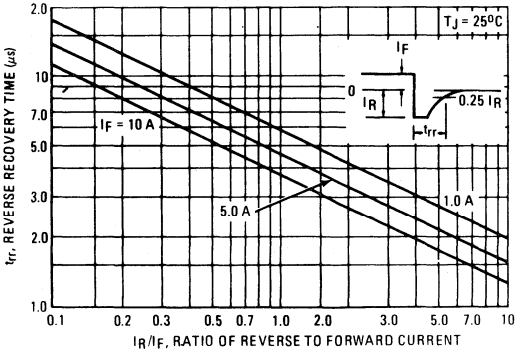


FIGURE 9 – REVERSE RECOVERY TIME



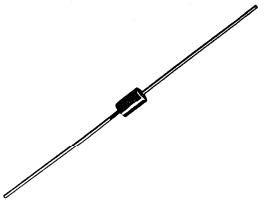
BYX10

AXIAL LEAD MOUNTED RECTIFIERS

. . . intended for low current rectifier applications.

SILICON RECTIFIER DIODES

1,600 VOLTS
0.5 AMP



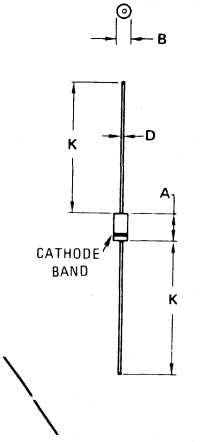
MAXIMUM RATINGS

Rating	Symbol	BYX10	Unit
Peak Working Reverse Voltage	V_{RWM}	800	Volts
Peak Repetitive Reverse Voltage	V_{RRM}	1600	Volts
Average Rectified Forward Current Resistive Load $V_{RWM} = V_{RWM}$ (max) $V_{RWM} = 60$ V	 $I_{F(AV)}$ $I_{F(AV)}$	 0.36 0.5	 Amp Amp
Repetitive Peak Forward Current	I_{FRM}	10	Amp
Non-Repetitive Peak Surge Current t = 10 ms, half sine wave T_J = 150°C prior to surge	I_{FSM}	30	Amp
Storage Junction Temperature Range	T_{stg}	— 65 + 150	°C
Junction Temperature	T_J	+ 150	°C

ELECTRICAL AND THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Forward Voltage I_F = 2 A, T_J = 25°C (see Note 1)	V_F		1.6	Volts
Reverse Current V_R = 800 V, T_J = 125°C V_R = 800 V, T_J = 25°C	 I_R I_R		 50 1	 μA μA

Note 1: Measured under pulse conditions to avoid excessive dissipation.

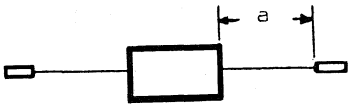


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04

THERMAL RESISTANCE (Influence of mounting method)

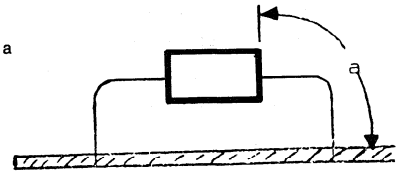
The quoted values apply when no other leads run to the tie-points. If leads of other dissipating components share the same tie-points, the thermal resistance will be higher than that quoted.



1. Mounted to solder tags at a lead-length
   a = 10 mm. $R_{th\ j\text{-}a}$ = 150°C/W

2. Mounted to solder tags at a = maximum lead-length
   $R_{th\ j\text{-}a}$ = 200°C/W

3. Mounted on printed-wiring with a small area of copper at any lead-length a
   $R_{th\ j\text{-}a}$ = 200°C/W



SOLDERING AND MOUNTING NOTES

1. Soldered joints must be at least 5 mm from the seal.

2. The maximum permissible temperature of the soldering iron or bath is 300°C, it must be in contact with the joint for no more than 3 seconds.

3. Avoid hot spots due to handling or mounting; the body of the device must not come into contact with or be exposed to a temperature higher than 150°C.

Curves and characteristics of MOTOROLA series 1N4001... 1N4007 shall apply analogously to BYX10.

BZX79C2V4 thru BZX79C200

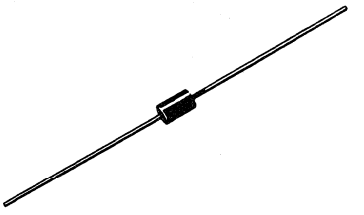
500 MILLIWATT HERMETICALLY SEALED GLASS SILICON ZENER DIODES

. . . A completely new line of 500 mW Zener Diodes offering the following advantages:

- Complete Voltage Range — 2.4 to 200 Volts
- DO-35 Package — Smaller than Conventional DO-7 Package
- Double Slug Type Construction
- Metallurgically Bonded Construction
- Pro-Electron Registration
- Oxide Passivated Die

GLASS ZENER DIODES

500 MILLIWATT
2.4 – 200 VOLTS



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
DC Power Dissipation @ $T_L \leq 50^oC$, Lead Length = 10 mm	P_D	500	mW
Derate above 50^oC		3.33	$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	^oC

MECHANICAL CHARACTERISTICS

CASE: Double slug type, hermetically sealed glass

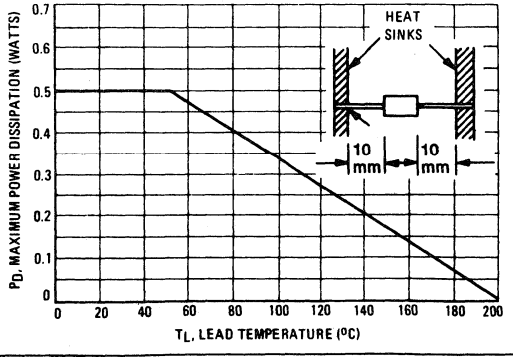
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230^oC, 2 mm from case for 10 seconds

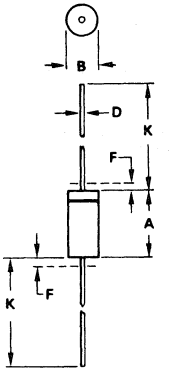
FINISH: All external surfaces are corrosion resistant with readily solderable leads.

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any

FIGURE 1 – STEADY STATE POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	12.70	–	0.500	–

All JEDEC dimensions and notes apply.

CASE 299-01
DO-35

NOTE:
1. POLARITY DENOTED BY CATHODE BAND.
2. LEAD DIAMETER IS NOT CONTROLLED WITHIN DIMENSION "F".

***ELECTRICAL CHARACTERISTICS** (T_L = 30°C unless otherwise noted.) (V_F = 1.5 Volts Max @ I_F = 100 mAdc for all types.)

Device Type (Note 2)	Zener Voltage (Note 1) Min.	Max.	I_{ZT} = (mA)	Impedance (Ohm) @ I_{ZT} f = 1000 Hz Max. (Note 3)	Leakage Current (μ A) Max.	@ V_R = (Volt)	Temp. Coefficient (Typical) (mV/°C) Min.	Max.	Capacitance (Typical) (pF) V_R = 0, f = 1 MHz
BZX79C2V4	2.2	2.6	5	100	100	1.0	— 3.5	?	255
BZX79C2V7	2.5	2.9	5	100	75	1.0	— 3.5	0	230
BZX79C3V0	2.8	3.2	5	95	50	1.0	— 3.5	0	215
BZX79C3V3	3.1	3.5	5	95	25	1.0	— 3.5	0	200
BZX79C3V6	3.4	3.8	5	90	15	1.0	— 3.5	0	185
BZX79C3V9	3.7	4.1	5	90	10	1.0	— 3.5	+ 0.3	175
BZX79C4V3	4.0	4.6	5	90	5	1.0	— 3.5	+ 1.0	160
BZX79C4V7	4.4	5.0	5	80	3	2.0	— 3.5	+ 0.2	130
BZX79C5V1	4.8	5.4	5	60	2	2.0	— 2.7	+ 1.2	110
BZX79C5V6	5.2	6.0	5	40	1	2.0	— 2.0	+ 2.5	95
BZX79C6V2	5.8	6.6	5	10	3	4.0	0.4	3.7	90
BZX79C6V8	6.4	7.2	5	15	2	4.0	1.2	4.5	85
BZX79C7V5	7.0	7.9	5	15	1	5.0	2.5	5.3	80
BZX79C8V2	7.7	8.7	5	15	.7	5.0	3.2	6.2	75
BZX79C9V1	8.5	9.6	5	15	.5	6.0	3.8	7.0	70
BZX79C10	9.4	10.6	5	20	.2	7.0	4.5	8.0	70
BZX79C11	10.4	11.6	5	20	.1	8.0	5.4	9.0	65
BZX79C12	11.4	12.7	5	25	.1	8.0	6.0	10.0	65
BZX79C13	12.4	14.1	5	30	.1	8.0	7.0	11.0	60
BZX79C15	13.8	15.6	5	30	.05	10.5	9.2	13.0	55
BZX79C16	15.3	17.1	5	40	.05	11.2	10.4	14.0	52
BZX79C18	16.8	19.1	5	45	.05	12.6	12.9	16.0	47
BZX79C20	18.8	21.2	5	55	.05	14.0	14.4	18.0	36
BZX79C22	20.8	23.3	5	55	.05	15.4	16.4	20.0	34
BZX79C24	22.8	25.6	5	70	.05	16.8	18.4	22.0	33
BZX79C27	25.1	28.9	2	80	.05	18.9		23.5	30
BZX79C30	28.0	32.0	2	80	.05	21.0		26.0	27
BZX79C33	31.0	35.0	2	80	.05	23.1		29.0	25
BZX79C36	34.0	38.0	2	90	.05	25.2		31.0	23
BZX79C39	37.0	41.0	2	130	.05	27.3		34.0	21
BZX79C43	40.0	46.0	2	150	.05	30.1		37.0	21
BZX79C47	44.0	50.0	2	170	.05	32.9		40.0	19
BZX79C51	48.0	54.0	2	180	.05	35.7		44.0	19
BZX79C56	52.0	60.0	2	200	.05	39.2		47.0	18
BZX79C62	58.0	66.0	2	215	.05	43.4		51.0	17
BZX79C68	64.0	72.0	2	240	.05	47.6		56.0	17
BZX79C75	70.0	79.0	2	255	.05	52.5		60.0	16.5
BZX79C82	77.0	87.0	2	280	.1	62.0	46	95	29
BZX79C91	85.0	96.0	2	300	.1	69.0	51	107	28
BZX79C100	94.0	106.0	1	500	.1	76.0	57	119	27
BZX79C110	104.0	116.0	1	650	.1	84.0	63	131	26
BZX79C120	114.0	127.0	1	800	.1	91.0	69	144	24
BZX79C130	124.0	141.0	1	950	.1	99.0	75	158	23
BZX79C150	138.0	156.0	1	1250	.1	114.0	87	185	21
BZX79C160	153.0	171.0	1	1400	.1	122.0	93	200	20
BZX79C180	168.0	191.0	1	1700	.1	137.0	105	228	18
BZX79C200	188.0	212.0	1	2000	.1	152.0	120	255	17

NOTE 1: Zener voltage is measured under pulse conditions such that Tj is no more than 2° C above T.A.

NOTE 2 — TOLERANCE AND VOLTAGE DESIGNATION
Tolerance designation — The type numbers listed indicate a tolerance of ± 5%. Device tolerances of ± 2% are indicated by a "B".

NOTE 3:
Z_{ZT} is measured by dividing the ac voltage drop across the device by the ac current applied. The specified limits are for I_Z(ac) = 0.1 I_Z(dc) with the ac frequency = 1.0 kHz.

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENTS (-55°C to +150°C temperature range)

FIGURE 2A – ZENER VOLTAGE 2.4 to 12 VOLTS

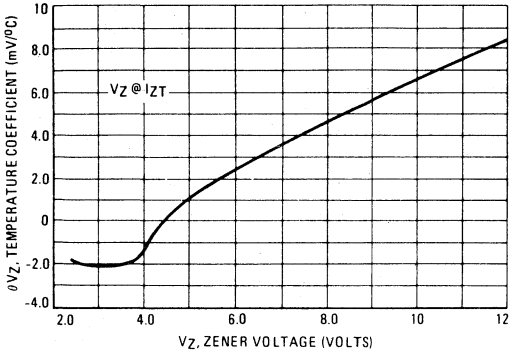


FIGURE 2B – ZENER VOLTAGE 12 to 200 VOLTS

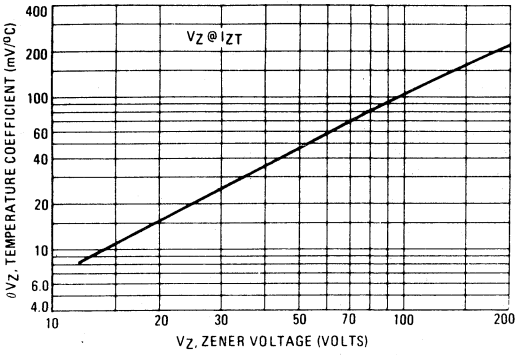


FIGURE 3 – EFFECT OF ZENER CURRENT ON ZENER IMPEDANCE

FIGURE 3A

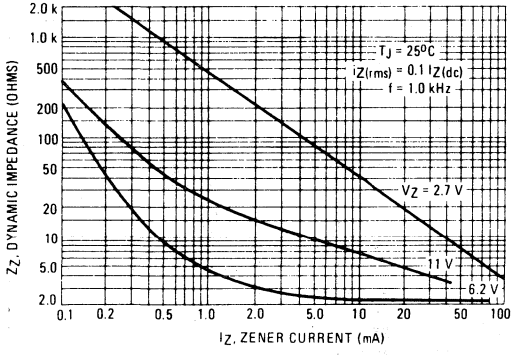


FIGURE 3B

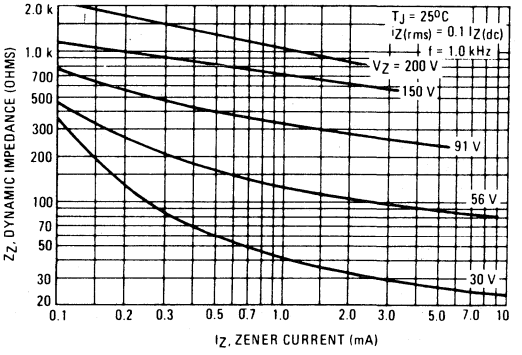
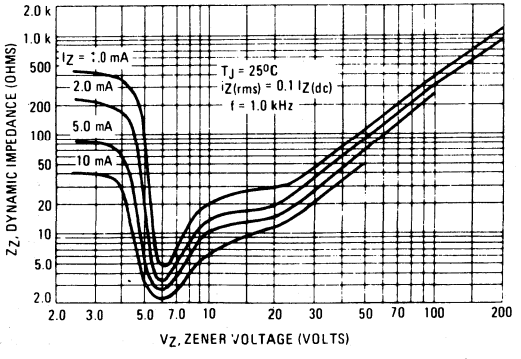


FIGURE 4 – EFFECT OF ZENER VOLTAGE ON ZENER IMPEDANCE

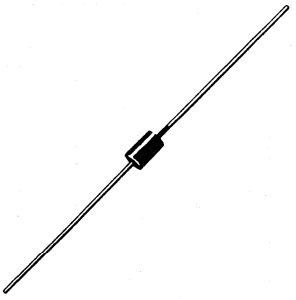


BZX83C2V7 thru BZX83C33
M-ZPD2.7 thru M-ZPD33

500 MILLIWATT HERMETICALLY SEALED GLASS SILICON ZENER DIODES

- Voltage Range 2.7 to 33 Volts according to the International E24 series (5%).
- DO-35 Package
- Double Slug Type Construction
- Metallurgically Bonded Construction
- Oxide Passivated Die

500 mW ZENER DIODES

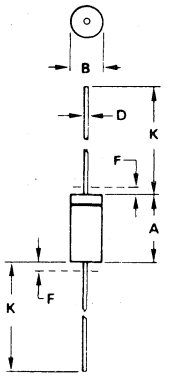


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ $T_L \leq 25°C$ Lead Length = 4 mm Derate above 25°C	P_D	500 3.33	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +175	°C

MECHANICAL CHARACTERISTICS

MARKING: Polarity Band. Letter C (5% tolerance), Nominal voltage
CASE: Double slug type, hermetically sealed glass
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230°C, 4 mm. from case for 10 seconds
FINISH: All external surfaces are corrosion resistant with readily solderable leads.
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.
MOUNTING POSITION: Any



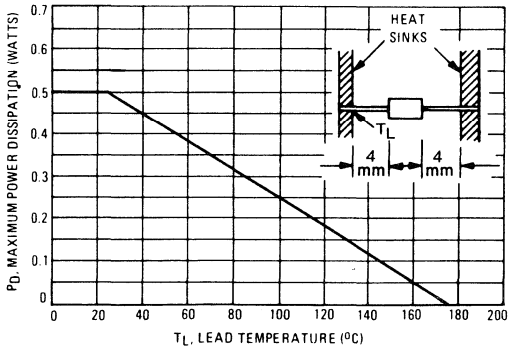
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	3.05	5.08	0.120	0.200
B	1.52	2.29	0.060	0.090
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	12.70	–	0.500	–

All JEDEC dimensions and notes apply.

CASE 299-01
DO-35

NOTE:
1. POLARITY DENOTED BY CATHODE BAND.
2. LEAD DIAMETER IS NOT CONTROLLED WITHIN DIMENSION "F"

FIGURE 1 – STEADY STATE POWER DERATING



ELECTRICAL CHARACTERISTICS (at T_L = 25 °C)

Motorola ZPD and BZX83C series. Forward Voltage V_F = 1V max at I_F = 50 mA.

Zener Voltage (Note 1) at I_{ZT} = 5 mA			Impedance (Ω) Max. (Note 2)		Typ. Temp. Coeff. at I_{ZT}	V_R min.	
Nominal	Min.	Max.	at I_{ZT}	at I_Z = 1 mA	%/o per °C	V	at I_R =
2.7	2.5	2.9	85	600	−0.09 . . . −0.04	1	100 μA
3.0	2.8	3.2	90	600	−0.09 . . . −0.03	1	60 μA
3.3	3.1	3.5	90	600	−0.08 . . . −0.03	1	30 μA
3.6	3.4	3.8	90	600	−0.08 . . . −0.03	1	20 μA
3.9	3.7	4.1	85	600	−0.07 . . . −0.03	1	10 μA
4.3	4.0	4.6	80	600	−0.06 . . . −0.01	1	5 μA
4.7	4.4	5.0	78	600	−0.05 . . . +0.02	1	2 μA
5.1	4.8	5.4	60	550	−0.03 . . . +0.04	0.8	100 nA
5.6	5.2	6.0	40	450	−0.02 . . . +0.06	1	100 nA
6.2	5.8	6.6	10	200	−0.01 . . . +0.07	2	100 nA
6.8	6.4	7.2	8	150	+0.02 . . . +0.07	3	100 nA
7.5	7.0	7.9	7	50	+0.03 . . . +0.07	5	100 nA
8.2	7.7	8.7	7	50	+0.04 . . . +0.07	6	100 nA
9.1	8.5	9.6	10	50	+0.05 . . . +0.08	7	100 nA
10	9.4	10.6	15	70	+0.05 . . . +0.08	7.5	100 nA
11	10.4	11.6	20	70	+0.05 . . . +0.09	8.5	100 nA
12	11.4	12.7	20	90	+0.06 . . . +0.09	9	100 nA
13	12.4	14.1	25	110	+0.07 . . . +0.09	10	100 nA
15	13.8	15.6	30	110	+0.07 . . . +0.09	11	100 nA
16	15.3	17.1	40	170	+0.08 . . . +0.095	12	100 nA
18	16.8	19.1	50	170	+0.08 . . . +0.10	14	100 nA
20	16.8	21.2	55	220	+0.08 . . . +0.10	15	100 nA
22	20.8	23.3	55	220	+0.08 . . . +0.10	17	100 nA
24	22.8	25.6	80	220	+0.08 . . . +0.10	18	100 nA
27	25.1	28.9	80	250	+0.08 . . . +0.10	20	100 nA
30	28.0	32.0	80	250	+0.08 . . . +0.10	22	100 nA
33	31.0	35.0	80	250	+0.08 . . . +0.10	24	100 nA

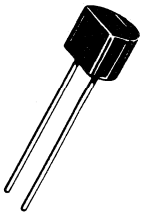
Note 1: Pulse test.
Note 2: f = 1 KHz, I_Z (ac) = 0.1 I_Z (dc).

SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in an inexpensive plastic package for low-cost, high-volume consumer requirements.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 Volts (Typ) @ I_F = 10 mA

SILICON HOT-CARRIER UHF MIXER DIODE



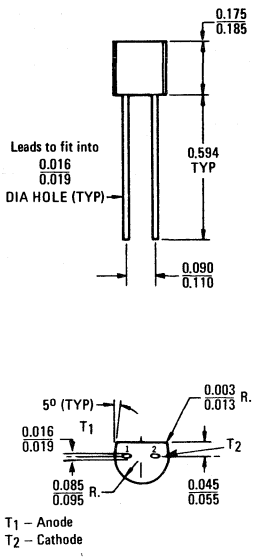
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.88	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F*	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	6.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.18	–	pF

*Matched sets available. Contact Motorola Sales Office with specific requirements.



CASE 182-1

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

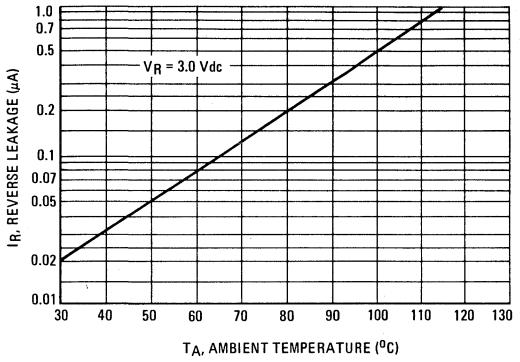


FIGURE 2 – FORWARD VOLTAGE

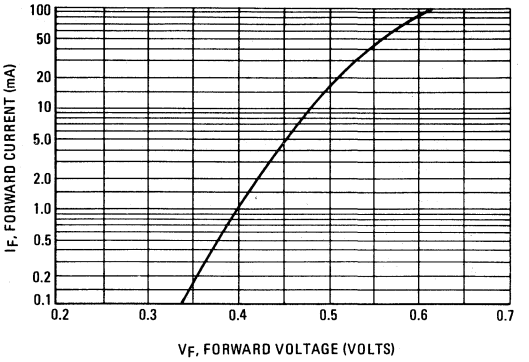


FIGURE 3 – CAPACITANCE

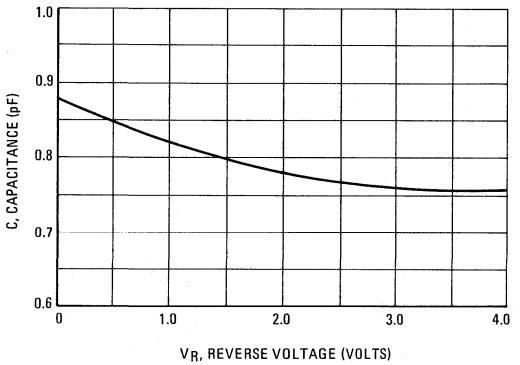


FIGURE 4 – NOISE FIGURE

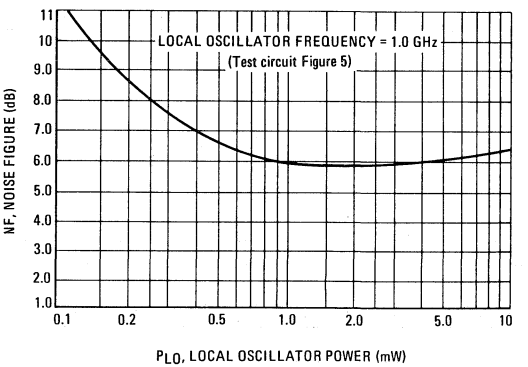
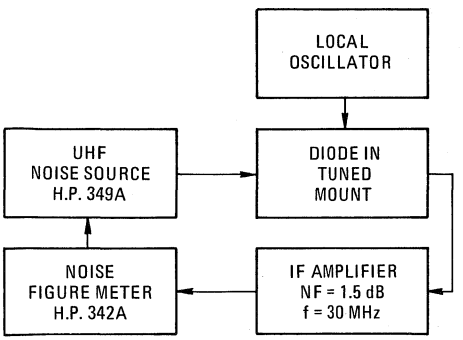


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

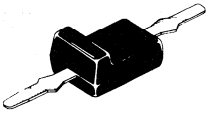
MBD102

SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in the low-inductance Mini-L package for low-cost, high-volume consumer requirements.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 volts (Typ) @ I_F = 10 mA
- Mini-L Ridge Clearly Identifies Cathode Lead for Easy Handling and Mounting

SILICON HOT-CARRIER UHF MIXER DIODE



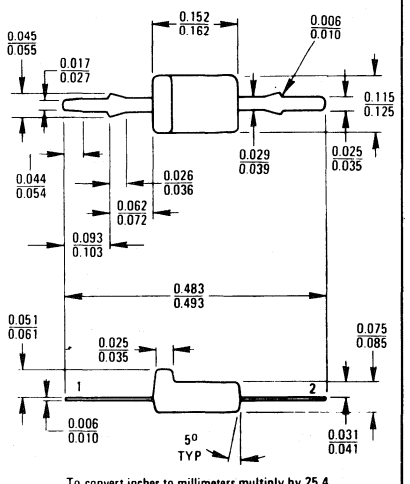
MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.8	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F(1)	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Measured at Lead Stop ≈ 1/8")	L_S	–	3.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz)	C_C	–	0.1	–	pF

(1) Matched sets available. Contact Motorola Sales Office with specific requirements.



To convert inches to millimeters multiply by 25.4

Pin 1. Cathode
2. Anode

CASE 226

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

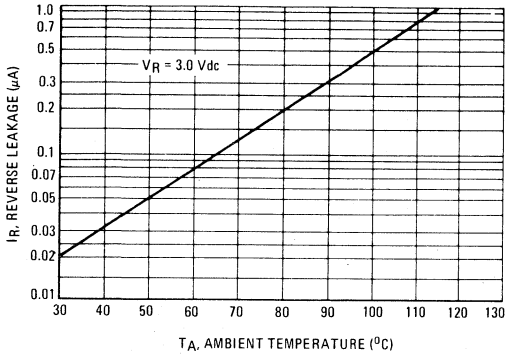


FIGURE 2 – FORWARD VOLTAGE

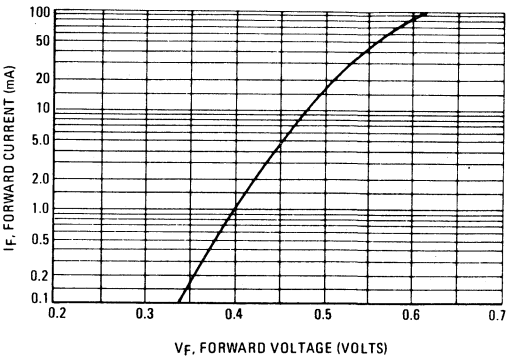


FIGURE 3 – DIODE CAPACITANCE

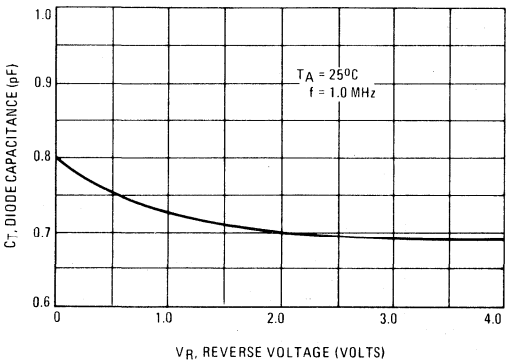


FIGURE 4 – NOISE FIGURE

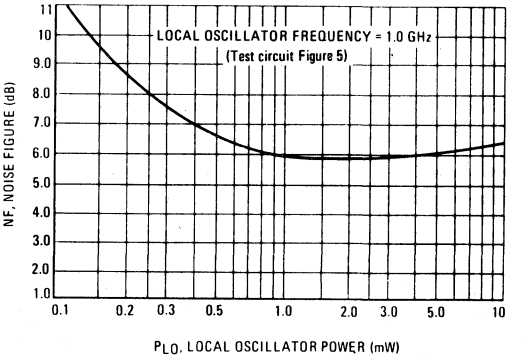
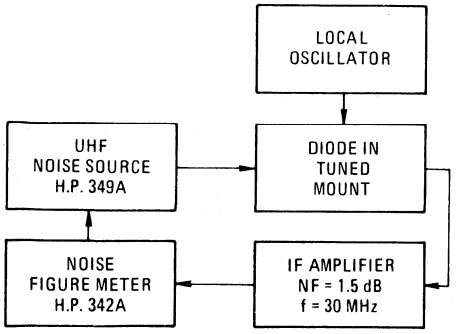


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

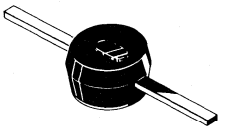
Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

SILICON HOT-CARRIER MICRO-I▲ DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure – 7.0 dB Max @ 1.0 GHz
- Very Low Capacitance – Less Than 1.0 pF @ Zero Volts
- High Forward Conductance – 0.48 Volts (Typ) @ I_F = 10 mA
- Supplied in Space Saving Miniature Package

SILICON HOT-CARRIER UHF MIXER MICRO-I DIODE



Device Marked with Yellow Top.

MAXIMUM RATINGS

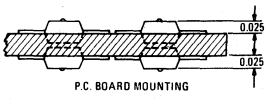
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	4.0	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	200 2.0	mW mW/°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T		0.88	1.0	pF
Forward Voltage (I_F = 10 mA)	V_F(1)	–	0.48	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	7.0	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA
Series Inductance (Note 3) (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	3.0	–	nH
Case Capacitance (Note 1) (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.15	–	pF

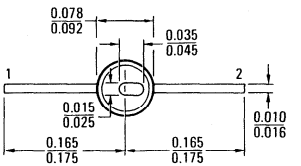
(1) Matched sets available. Contact Motorola Sales Office with specific requirements.

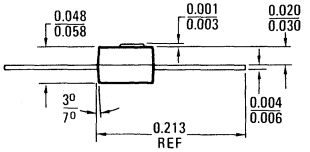
TYPICAL HIGH DENSITY MOUNTING TECHNIQUE



P.C. BOARD MOUNTING

Maximum Solder Temperature 250°C for 10s





STYLE 1:
PIN 1. ANODE
2. CATHODE

Optional Package with Raised Circular Tab Available; Specify Case 166-01.

CASE 166-02

▲Trademark of Motorola Inc.

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

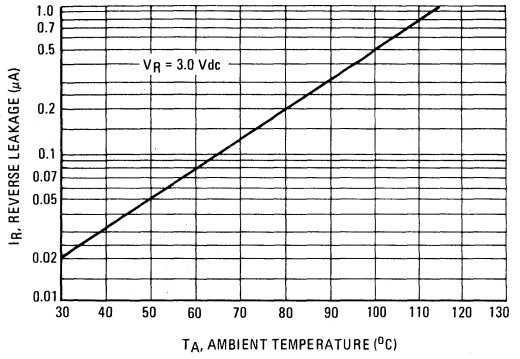


FIGURE 2 – FORWARD VOLTAGE

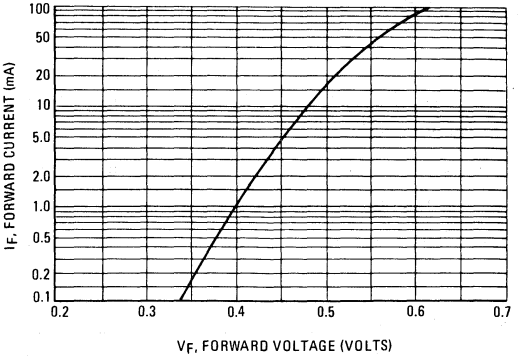


FIGURE 3 – CAPACITANCE

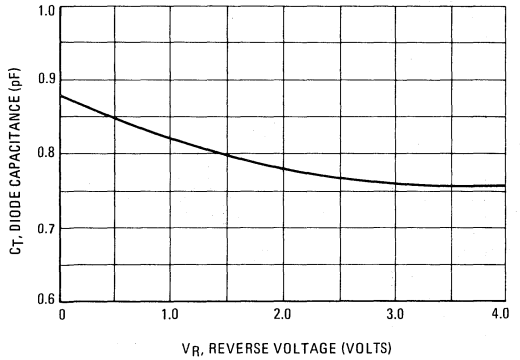


FIGURE 4 – NOISE FIGURE

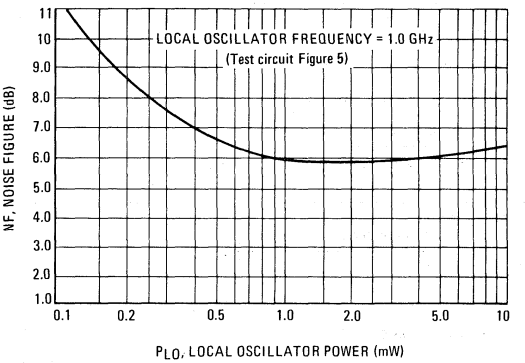
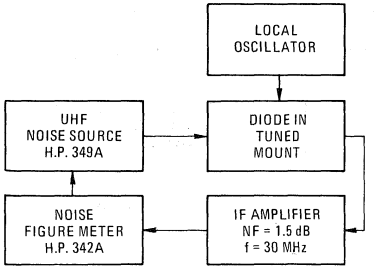


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

MDA920A1 thru MDA920A9

Designers Data Sheet

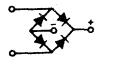
MINIATURE INTEGRAL DIODE ASSEMBLIES

. . . passivated, diffused-silicon dice interconnected and transfer molded into voidless hybrid rectifier circuit assemblies.

- Large Inrush Surge Capability – 45 A (For 1.0 Cycle)
- Efficient Thermal Management Provides Maximum Power Handling in Minimum Space

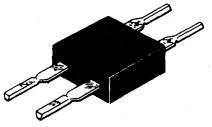
Designers Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.



SINGLE-PHASE FULL-WAVE BRIDGE

1.5 AMPERES
25–1000 VOLTS



MAXIMUM RATINGS

Rating (Per Leg)	Symbol	A1	A2	A3	A4	A5	A6	A7	A8	A9	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	25	50	100	200	300	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitative Load	 Vdc Vdc	 15 25	 30 50	 62 100	 124 200	 185 300	 250 400	 380 600	 500 800	 620 1000	 Volts Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	18	35	70	140	210	280	420	560	700	Volts
Average Rectified Forward Current (single phase bridge resistive load, 60 Hz, see Figure 6, $T_A = 50^oC$	I_O	1.5									Amp
Non-Repetitive Peak Surge Current, (see Figure 2) rated load, $T_J = 175^oC$	I_{FSM}	45 for 1 cycle									Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +175									^oC

ELECTRICAL CHARACTERISTICS

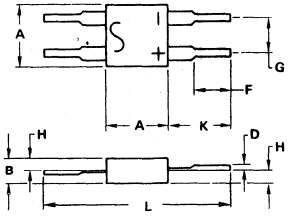
Characteristic	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (Per Leg) (I_F = 2.4 Amp, $T_J = 25^oC$) Figure 1	V_F	1.2	Volts
Maximum Reverse Current (Rated dc Voltage across ac terminals, $T_J = 25^oC$)	I_R	20	μA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Effective Bridge Thermal Resistance, Junction to Ambient (Full-Wave Bridge Operation, Typical Printed Circuit Board Mounting)	$R_{\theta JA}$	50	$^oC/W$

MECHANICAL CHARACTERISTICS

CASE: Transfer-molded plastic encapsulation.
POLARITY: Terminal-designation embossed on case +DC output
-DC output
~AC input
MOUNTING POSITION: Any
WEIGHT: 1.0 gram (approx)
TERMINALS: Readily solderable connections, corrosion resistant.



NOTES:
1. LEAD DIM "D" TO BE MEASURED WITHIN "F"
2. LEADS FORMED TO FIT INTO HOLE 0.94 mm (0.037) MIN.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.73	0.240	0.265
B	2.29	2.79	0.090	0.110
D	0.51	0.94	0.020	0.037
F	3.56	6.35	0.140	0.250
G	3.68	3.94	0.145	0.155
H	1.02	1.27	0.040	0.050
K	6.60	10.16	0.260	0.400
L	19.30	27.05	0.760	1.065

CASE 109-03

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE (PER LEG)

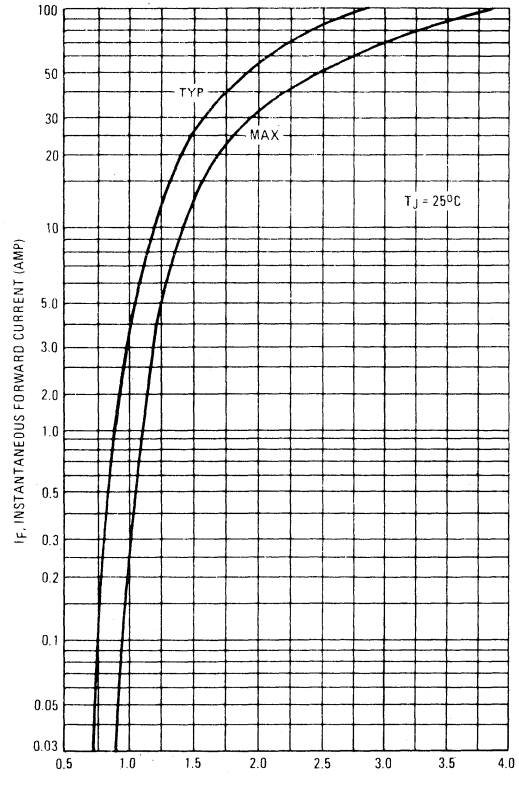


FIGURE 2 – MAXIMUM SURGE CAPABILITY

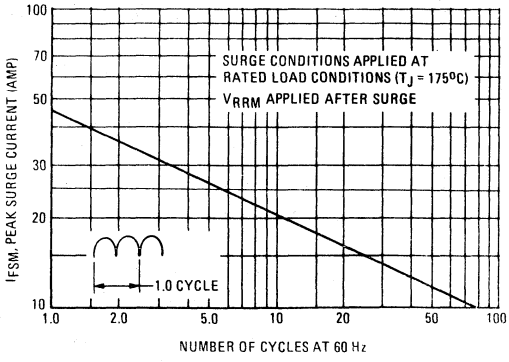


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

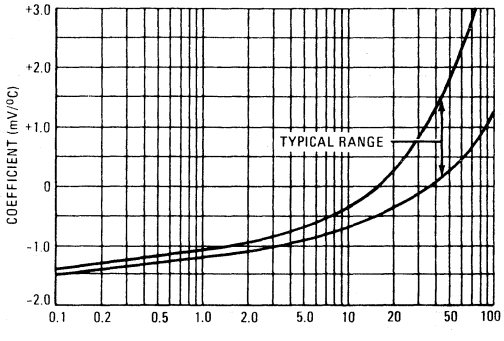


FIGURE 4 – TYPICAL THERMAL RESPONSE

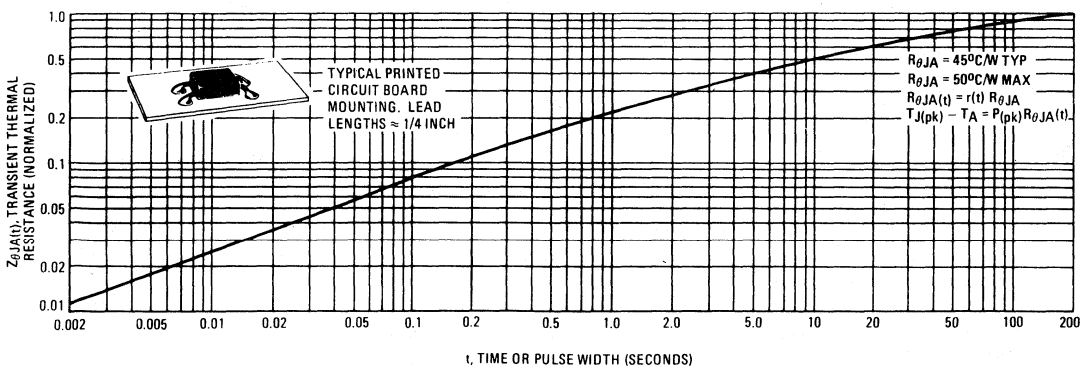


FIGURE 5 – POWER DISSIPATION

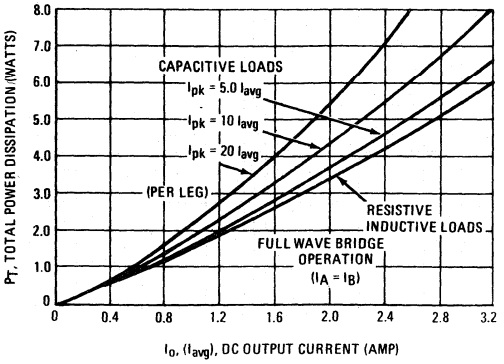


FIGURE 6 – CURRENT DERATING

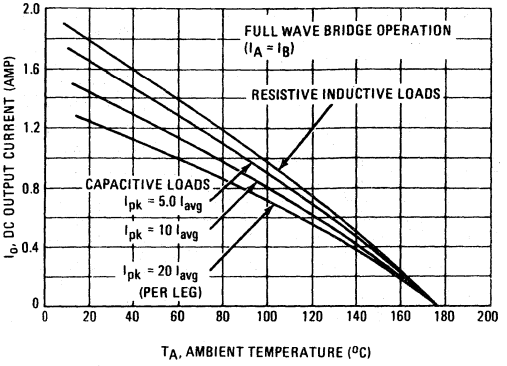
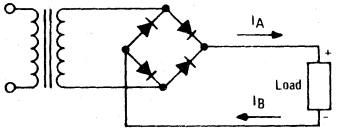
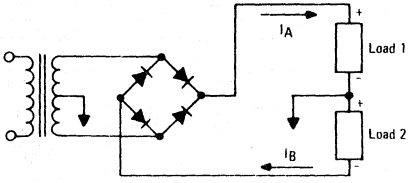


FIGURE 7 – BASIC CIRCUIT USES FOR BRIDGE RECTIFIERS



CIRCUIT A



CIRCUIT B

APPLICATION NOTE

The Data of Figure 4 applies for typical wire terminal or printed circuit board mounting conditions in still air. Under these or similar conditions, the thermal resistance between the diode junctions and the leads at the edge of the case is a small fraction of the thermal resistance from junction to ambient. Consequently, the lead temperature is very close to the junction temperature. Therefore, it is recommended that the lead temperature be measured when the diodes are operating in prototype equipment, in order to determine if operation is within the diode temperature ratings. The lead having the highest thermal resistance to the ambient will yield readings closest to the junction temperature. By measuring temperature as outlined, variations of junction to ambient thermal resistance, caused by the amount of surface area of the terminals or printed circuit board and the degree of air convection, as well as proximity of other heat sources cease to be important design considerations.

Bridge rectifiers are used in two basic circuit configurations as shown by circuits A and B of Figure 7. The current derating data of Figure 6 applies to the standard bridge circuit (A), where $I_A = I_B$. The derating data considers the thermal response of the junction and is based upon the criteria that the junction temperature must not exceed rated $T_{J(max)}$ when peak reverse voltage is applied. However, because of the slow thermal response and the close thermal coupling between the individual semiconductor die in the MDA920A assembly, the maximum ambient temperature is given closely by

$$T_A = T_{J(max)} - R_{\theta JA} P_T$$

where P_T is the total average power dissipation in the assembly.

For the circuit of Figure B, use of the above formula will yield suitable rating information. For example to determine $T_{A(max)}$ for the conditions:

$I_A = 0.5$ A, $I_{pk} = 10\ I_{avg}$
$I_B = 1.0$ A, $I_{pk} = 18\ I_{avg}$

From Figure 5: For I_A, read $P_{TA} \approx 0.8$ W
For I_B, read $P_{TB} \approx 2.2$ W

$P_T = (P_{TA} + P_{TB}) \div 2 = 1.5$ W

(Division by 2 is necessary as data from Figure 5 is for full-wave bridge operation.) $\therefore T_{A(max)} = 175^{o} - (50)(1.5) = 100^{o}C$.

FIGURE 8 – FORWARD RECOVERY TIME

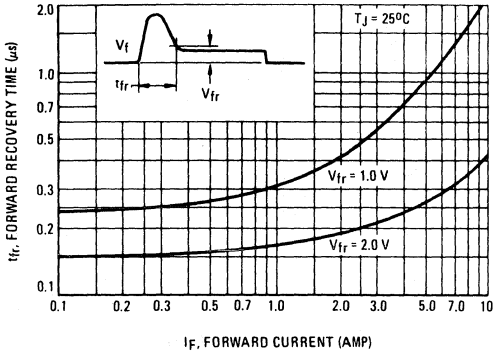


FIGURE 9 – REVERSE RECOVERY TIME

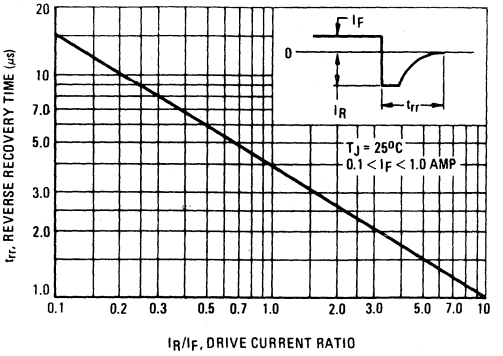


FIGURE 10 – RECTIFICATION WAVEFORM EFFICIENCY

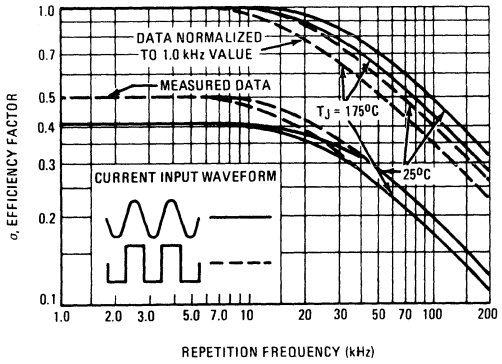
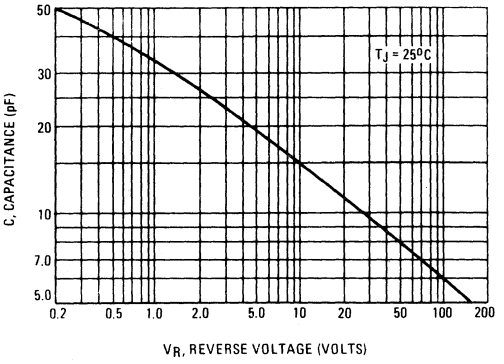
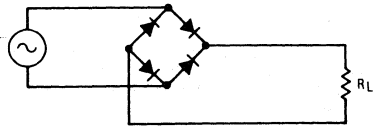


FIGURE 11 – CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 12 – SINGLE-PHASE FULL-WAVE BRIDGE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 10 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_{o(dc)}}{R_L}}{\frac{V^2_{o(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{o(dc)}}{V^2_{o(ac)} + V^2_{o(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{4V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{2R_L}} \cdot 100\% = \frac{8}{\pi^2} \cdot 100\% = 81.2\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 100\% \quad (3)$$

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 9) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 10.

It should be emphasized that Figure 10 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 10.

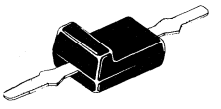
MPN3401
MPN3402

SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in an inexpensive low-inductance plastic package for low cost, high-volume consumer and industrial requirements.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Both 1 pF and 2 pF Devices for Design Selectivity
- Very Low Series Resistance at 100 MHz — 0.34 Ohms (Typ) @ I_F = 10 mAdc
- Low Inductance Mini-L Package
- Mini-L Ridge Clearly Identifies Cathode Lead for Easy Handling and Mounting

SILICON PIN SWITCHING DIODE



MPN3401 – Blue Plastic with Brown Color Stripe
MPN3402 – Blue Plastic with Red Color Stripe

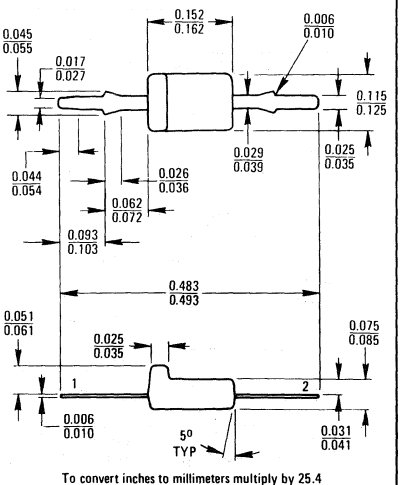
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	35	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	35	–	–	Volts
Diode Capacitance (Note 1) MPN3401 (V_R = 20 Vdc, f = 1.0 MHz) MPN3402	C_T	– –	– –	1.0 2.0	pF
Series Resistance (Figure 5) MPN3401 (I_F = 10 mA) MPN3402	R_S	– –	– –	0.7 0.6	Ohms
Reverse Leakage Current (V_R = 25 Vdc)	I_R	–	–	0.1	μA
Series Inductance (Note 2) (f = 250 MHz) (Measured at Lead Stop ≈ 1/8")	L_S	–	3.0	–	nH
Case Capacitance (f = 1.0 MHz)	C_C	–	0.1	–	pF

NOTES
1. C_T is measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
2. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).



To convert inches to millimeters multiply by 25.4

Pin 1. Cathode
2. Anode

CASE 226

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

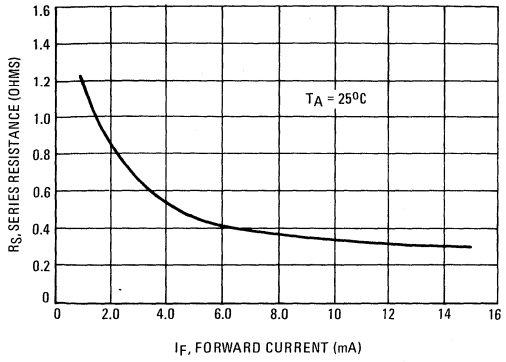


FIGURE 2 – FORWARD VOLTAGE

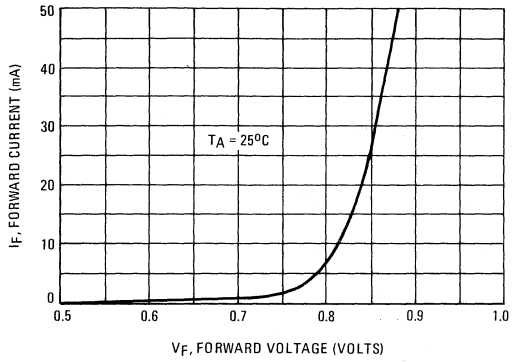


FIGURE 3 – DIODE CAPACITANCE

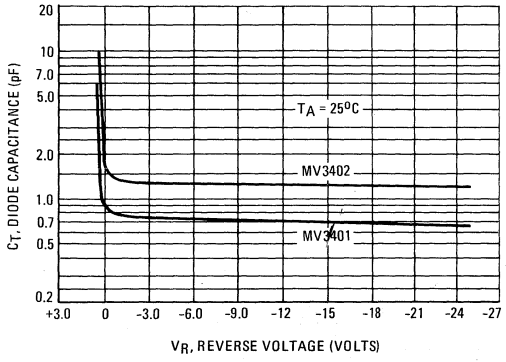


FIGURE 4 – LEAKAGE CURRENT

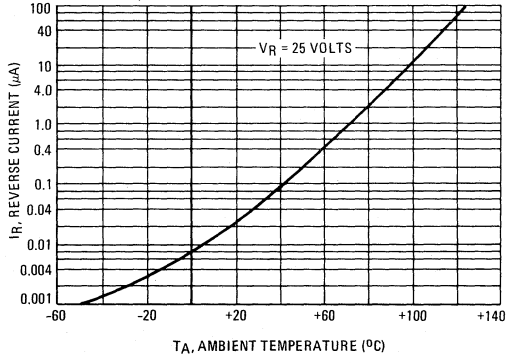
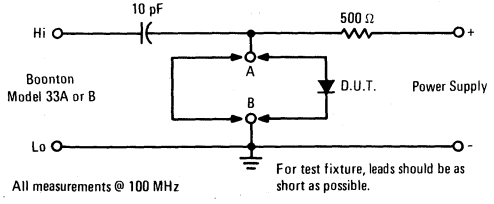


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\,G}{C^2}$$

Where:
G – in micromhos,
C – in pF,
R_S – in ohms

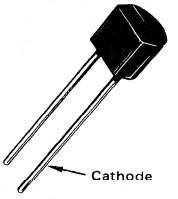
MPN3404

SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a cost effective TO-92 type plastic package for economical, high-volume consumer and industrial requirements.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Series Resistance @ 100 MHz – R_S = 0.7 Ohms (Typ) @ I_F = 10 mAdc
- Sturdy TO-92 Style Package for Handling Ease

SILICON PIN SWITCHING DIODE



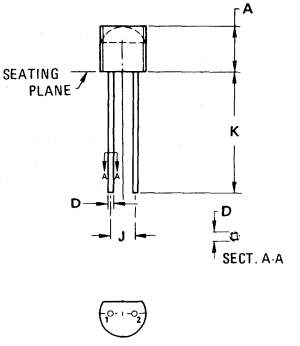
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	20	–	–	Volts
Diode Capacitance (Note 1) (V_R = 15 Vdc, f = 1.0 MHz)	C_T	–	1.3	2.0	pF
Series Resistance (Figure 5) (I_F = 10 mA)	R_S	–	0.7	0.85	Ohms
Reverse Leakage Current (V_R = 15 Vdc)	I_R	–	–	0.1	μA
Series Inductance (Note 2) (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	6.0	–	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.18	–	pF

NOTES
1. C_T is measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
2. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 182-03

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

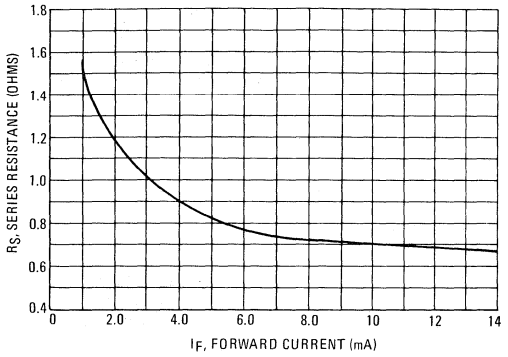


FIGURE 2 – FORWARD VOLTAGE

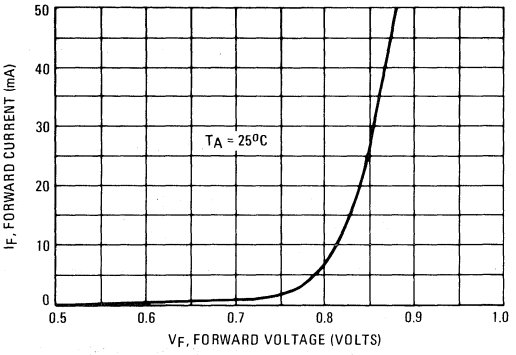


FIGURE 3 – DIODE CAPACITANCE

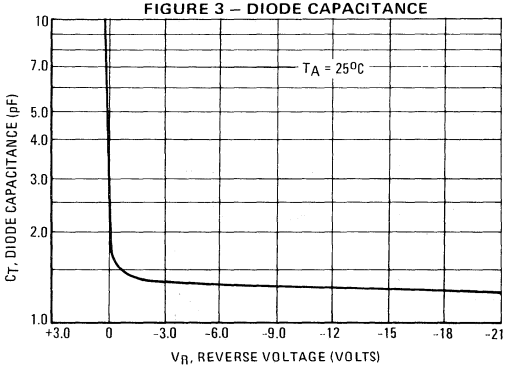


FIGURE 4 – LEAKAGE CURRENT

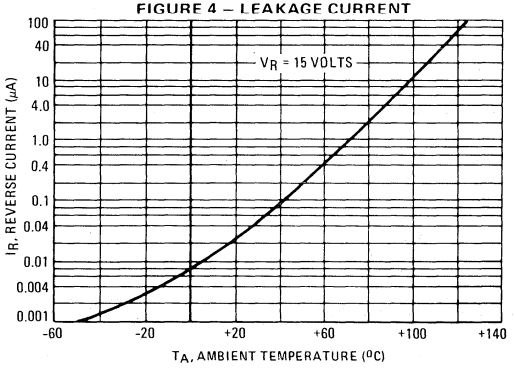
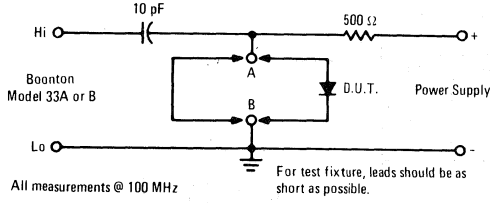


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



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$$R_S = \frac{2.533\,G}{C^2}$$

Where:
G – in micromhos,
C – in pF,
R_S – in ohms

MR501 • MR502 • MR504
MR506 • MR508 • MR510

Designers Data Sheet

MINIATURE SIZE, AXIAL LEAD MOUNTED STANDARD RECOVERY POWER RECTIFIERS

. . . designed for use in power supplies and other applications having need of a device with the following features:

- High Current to Small Size
- High Surge Current Capability
- Low Forward Voltage Drop
- Void-Free Economical Plastic Package
- Available in Volume Quantities

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	MR 501	MR 502	MR 504	MR 506	MR 508	MR 510	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	150	250	450	650	850	1050	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 95°C, PC Board Mounting) (1) (EIA Standard Conditions L = 1/32", T_L = 85°C)	I_O	3.0 8.0						Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)						Amp
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	-65 to +175						°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mounting, See Note 2 on Page 4).	$R_{\theta JA}$	28	°C/W

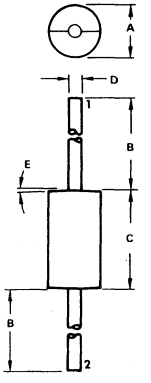
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (3) (i_F = 9.4 Amp, T_J = 175°C) (i_F = 9.4 Amp, T_J = 25°C)	v_F	– –	0.9 1.04	1.0 1.1	Volts
Reverse Current (rated dc voltage) (3) T_J = 25°C T_J = 100°C	I_R	– –	0.1 2.8	5.0 25	μA

(1) Derate for reverse power dissipation. See Note on Page 2.
(2) Derate as shown in Figure 1.
(3) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
▲Trademark of Motorola Inc.

STANDARD RECOVERY POWER RECTIFIERS

100-1000 VOLTS
3 AMPERE



	INCHES		MILLIMETERS	
A	0.190	0.210	4.83	5.33
B	1.062	1.072	26.97	27.23
C	0.370	0.380	9.40	9.65
D	0.048	0.052	1.22	1.32
E	2°		2°	

CASE 267

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Indicated by Cathode Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 200 volts. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (175°C or the temperature at which thermal runaway occurs, whichever is lowest.)

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figure solves for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where $T_J = 175°C$, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figure 1 as a difference in the rate of change of the slope in the vicinity of 165°C. The data of Figure 1 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the rectifiers reverse characteristics.

Example: Find $T_{A(max)}$ for MR510 operated in a 400 Volt dc supply using a full wave center-tapped circuit with capacitive filter such that $I_{DC} = 6.0$ A, ($I_{F(AV)} = 3.0$ A), $I_{(PK)}/I_{(AV)} = 10$, Input Voltage = 283 V(rms) (line to center tap), $R_{\theta JA} = 28°C/W$.

Step 1: Find $V_{R(equiv)}$. Read F = 1.11 from Table 1 ∴
$V_{R(equiv)} = 1.41(283)(1.11) = 444$ V

Step 2: Find T_R from Figure 1. Read $T_R = 167°C$ @ $V_R = 444$ V & $R_{\theta JA} = 28°C/W$.

Step 3. Find $P_{F(AV)}$ from Figure 8. Read $P_{F(AV)} = 4$ W @ $\frac{I_{PK}}{I_{AV}} = 10$ & $I_{F(AV)} = 3.0$ A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)} = 167-(28)(4) = 55°C$.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave Center-Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.45	1.11	0.45	0.55	0.90	1.11
Square Wave	0.61	1.22	0.61	0.61	1.22	1.22

*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE

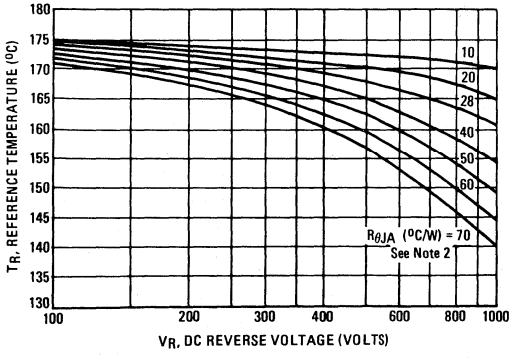
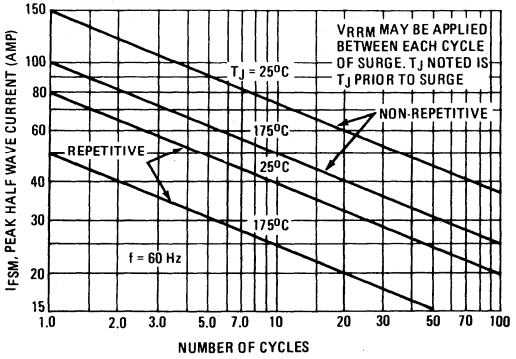


FIGURE 2 – MAXIMUM SURGE CAPABILITY



CURRENT DERATING

(Reverse Power Loss Neglected)

FIGURE 3 – PC BOARD MOUNTING

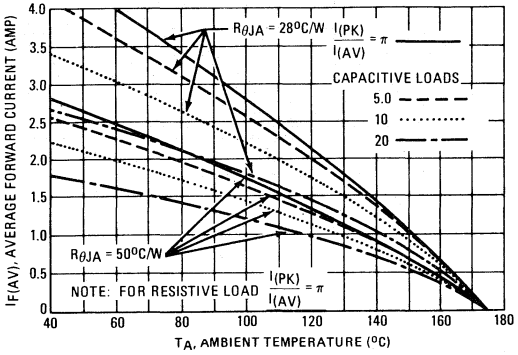


FIGURE 4 – SEVERAL LEAD LENGTHS

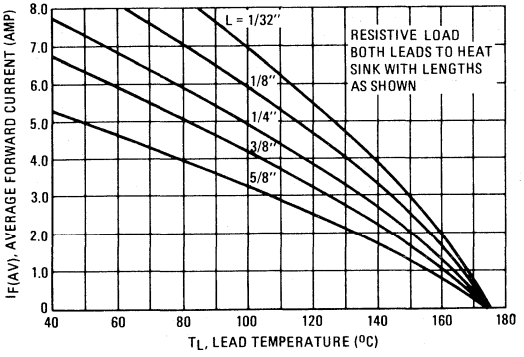


FIGURE 5 – 1/8" LEAD LENGTH

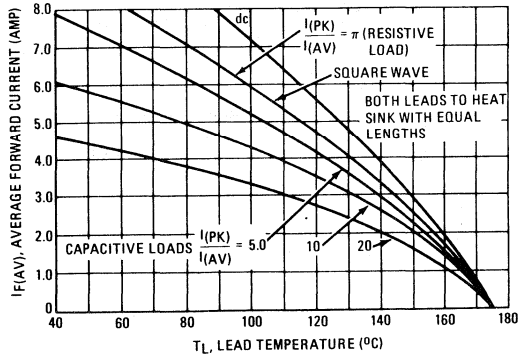


FIGURE 6 – MAXIMUM FORWARD VOLTAGE

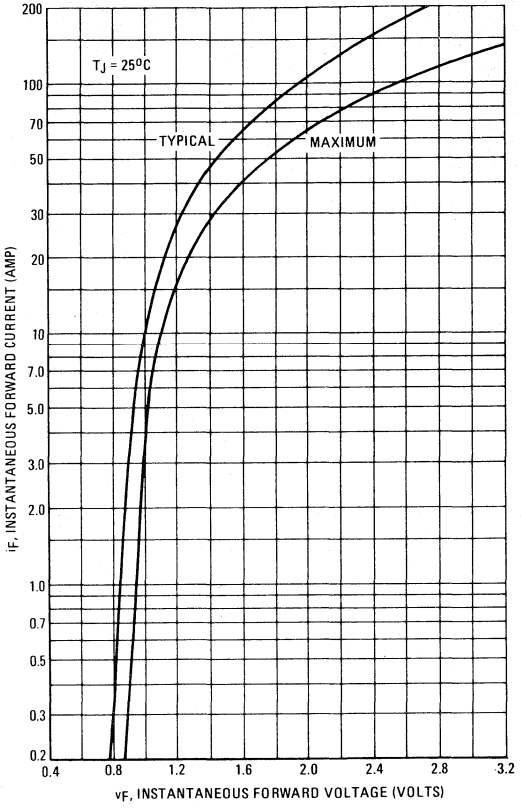


FIGURE 7 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

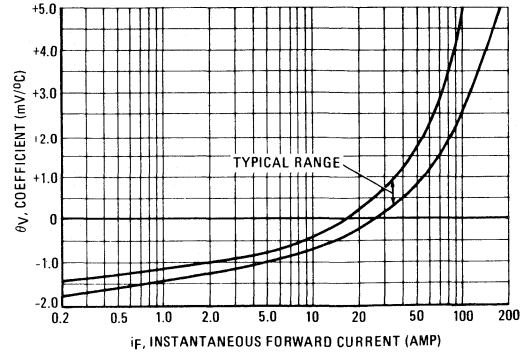


FIGURE 8 – FORWARD POWER DISSIPATION

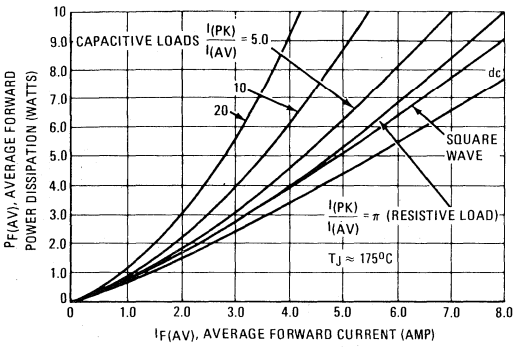
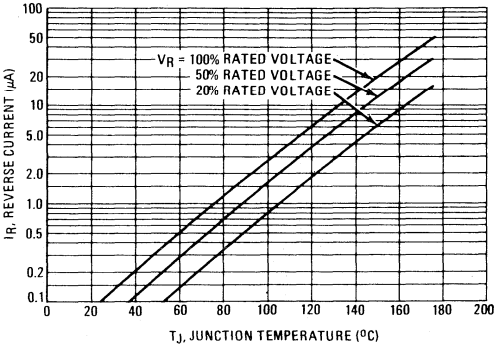


FIGURE 9 – TYPICAL REVERSE CURRENT



THERMAL CHARACTERISTICS

FIGURE 10 – THERMAL RESPONSE

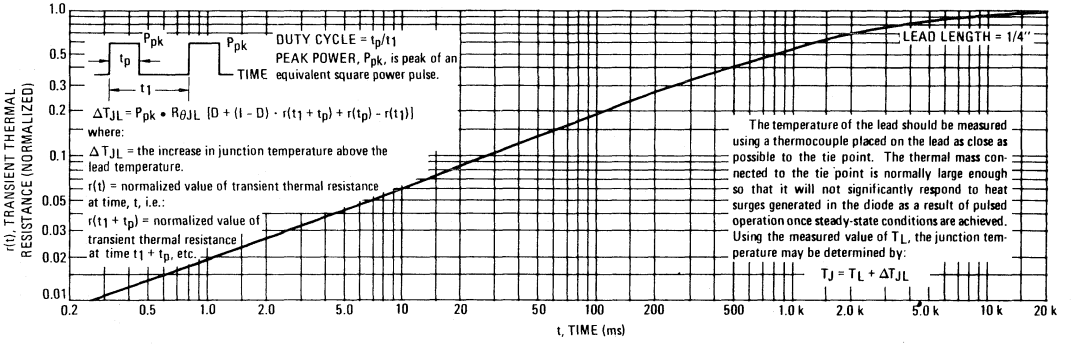
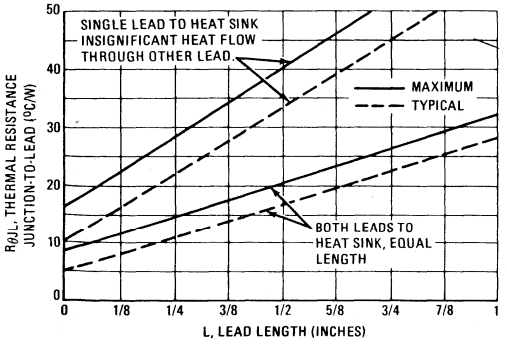


FIGURE 11 – STEADY-STATE THERMAL RESISTANCE



NOTE 2 – AMBIENT MOUNTING DATA

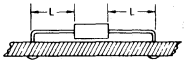
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

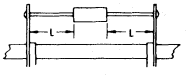
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 1 1/2" x 1-1/2" Copper Surface

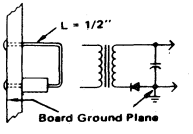
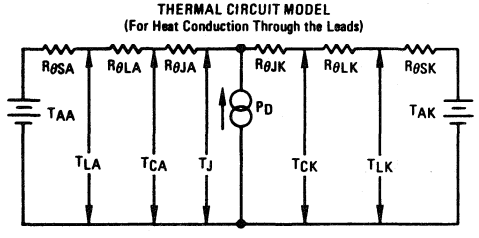


FIGURE 12 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)
Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} \approx R_{\theta JL}$

TYPICAL DYNAMIC CHARACTERISTICS
(T_J = 25°C)

FIGURE 13 – FORWARD RECOVERY TIME

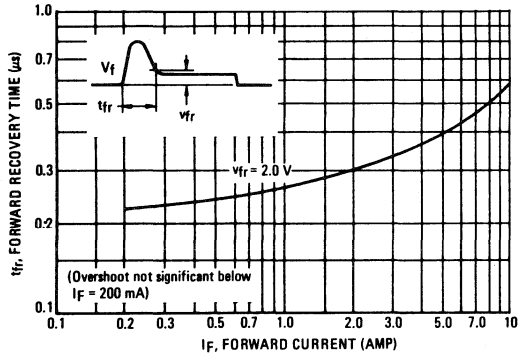


FIGURE 14 – REVERSE RECOVERY TIME

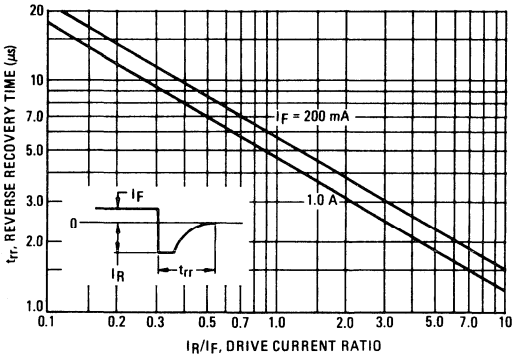


FIGURE 15 – RECTIFICATION WAVEFORM EFFICIENCY

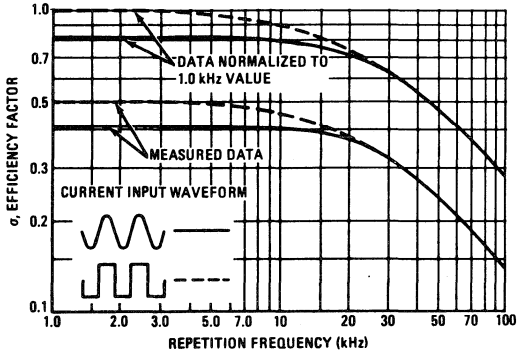
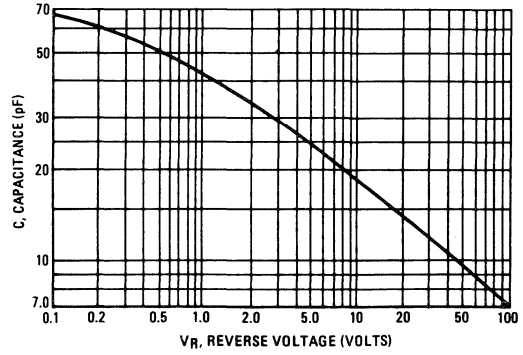
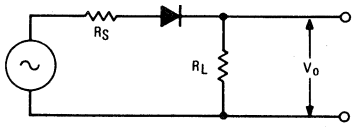


FIGURE 16 – JUNCTION CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 17 – SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 15 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_o(dc)}{R_L}}{\frac{V^2_o(rms)}{R_L}} \cdot 100\% = \frac{V^2_o(dc)}{V^2_o(ac) + V^2_o(dc)} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 14) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 15.

It should be emphasized that Figure 15 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_o with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the figure.

MR751 • MR752
MR754 • MR756

Designers Data Sheet

HIGH CURRENT LEAD MOUNTED RECTIFIERS

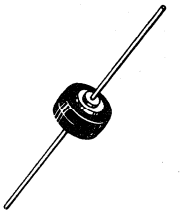
- Current Capacity Comparable To Chassis Mounted Rectifiers
- Very High Surge Capacity
- Insulated Case

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

HIGH CURRENT LEAD MOUNTED SILICON RECTIFIERS

100–600 VOLTS DIFFUSED JUNCTION

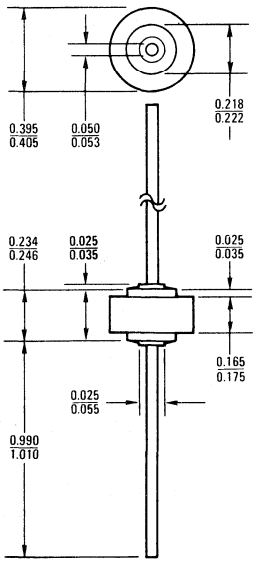


MAXIMUM RATINGS

Characteristic	Symbol	MR751	MR752	MR754	MR756	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	100	200	400	600	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz peak)	V_{RSM}	120	240	480	720	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	70	140	280	420	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz.) See Figures 5 and 6	I_O	22(T_L = 60°C, 1/8" Lead Lengths) 6.0(T_A = 60°C, P.C. Board mounting)				Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	400 (for 1 cycle)				Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175				°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (I_F = 100 Amp, T_J = 25°C)	v_F	1.25	Volts
Maximum Forward Voltage Drop (I_F = 6.0 Amp, T_A = 25°C, 3/8 inch leads)	V_F	0.90	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	0.25 1.0	mA



CASE 194-02

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded

MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C 3/8" from case for 10 seconds at 5.0 lbs. tension

FINISH: All external surfaces are corrosion-resistant, leads are readily solderable

POLARITY: Indicated by diode symbol

WEIGHT: 2.5 Grams (approx)

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE

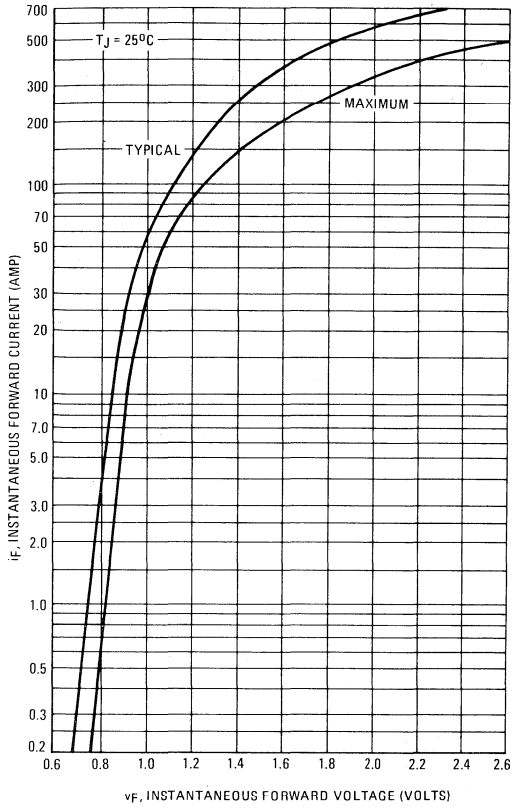


FIGURE 2 – MAXIMUM SURGE CAPABILITY

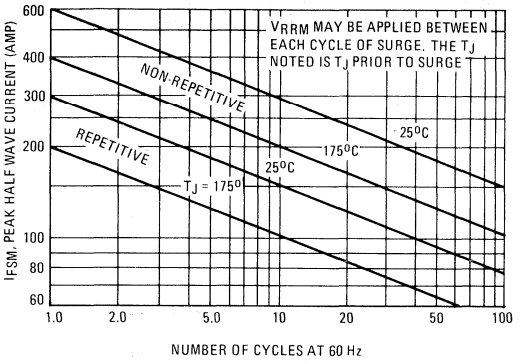


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

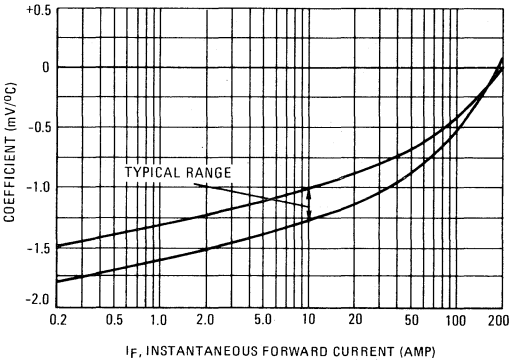


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE

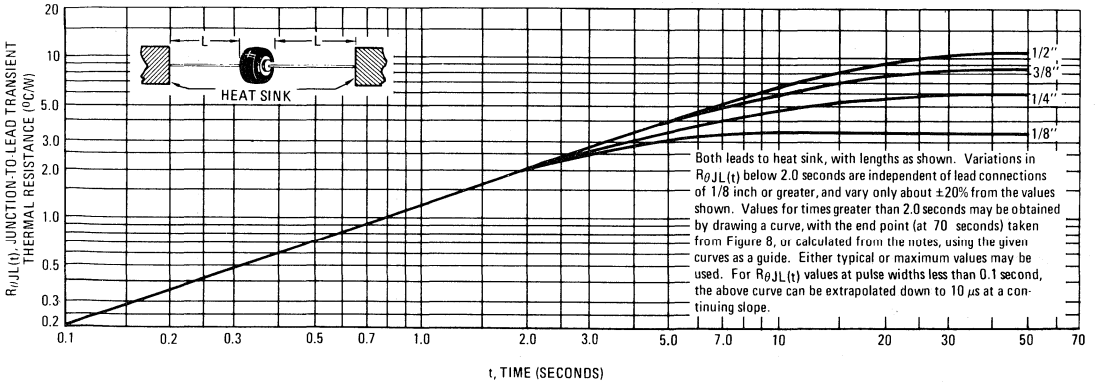


FIGURE 5 – MAXIMUM CURRENT RATINGS

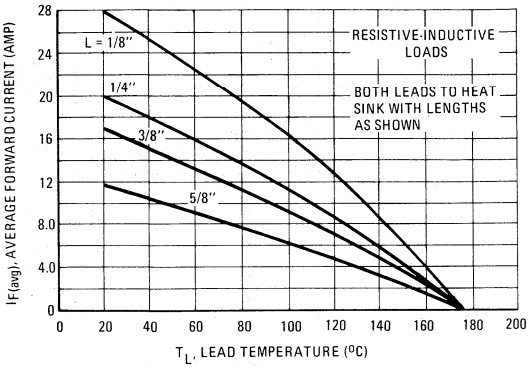


FIGURE 6 – MAXIMUM CURRENT RATINGS

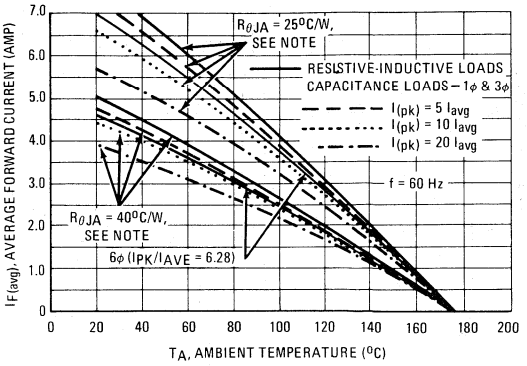


FIGURE 7 – POWER DISSIPATION

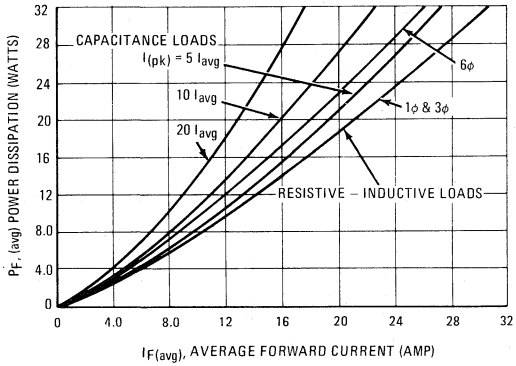
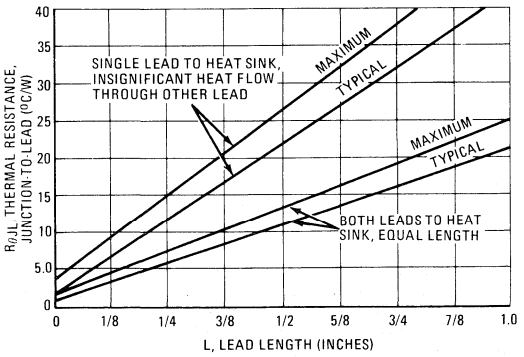


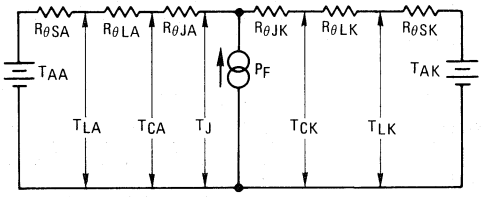
FIGURE 8 – STEADY STATE THERMAL RESISTANCE



NOTES

THERMAL CIRCUIT MODEL

(For Heat Conduction Through The Leads)



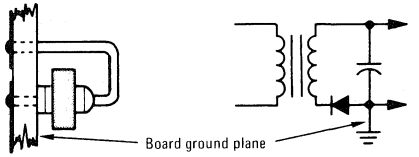
Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. Lowest values occur when one side of the rectifier is brought as close as possible to the heat sink as shown below. Terms in the model signify:

T_A = Ambient Temperature — $R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
T_L = Lead Temperature — $R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
T_C = Case Temperature — $R_{\theta J}$ = Thermal Resistance, Junction to Case
T_J = Junction Temperature — P_F = Power Dissipation
(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:
$R_{\theta L}$ = 40°C/W/IN. Typically and 44°C/W/IN Maximum
$R_{\theta J}$ = 2°C/W Typically and 4°C/W Maximum

Since $R_{\theta J}$ is so low, measurements of the case temperature, T_C, will be approximately equal to junction temperature in practical lead mounted applications. When used as a 60 Hz rectifier, the slow thermal response holds $T_{J(PK)}$ close to $T_{J(AVG)}$. Therefore maximum lead temperature may be found from: $T_L = 175^{\circ} - R_{\theta JL} P_F$. P_F may be found from Figure 7.

The recommended method of mounting to a P.C. board is shown on the sketch, where $R_{\theta JA}$ is approximately 25°C/W for a 1-1/2" x 1-1/2" copper surface area. Values of 40°C/W are typical for mounting to terminal strips or P.C. boards where available surface area is small.



Recommended mounting for half wave circuit

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 9 – RECTIFICATION EFFICIENCY

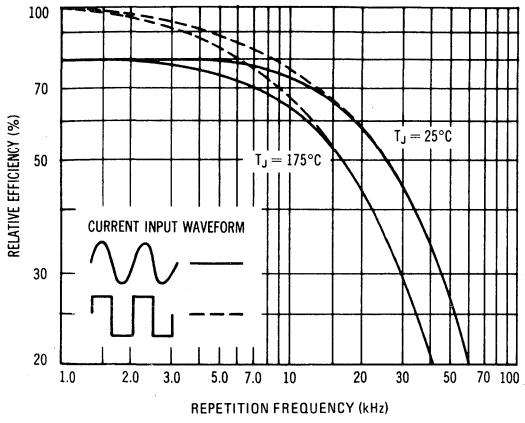


FIGURE 10 – REVERSE RECOVERY TIME

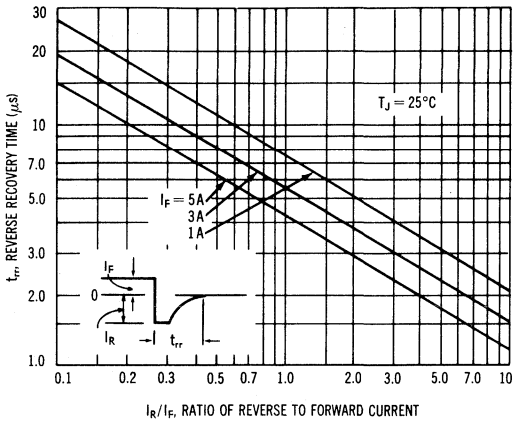


FIGURE 11 – JUNCTION CAPACITANCE

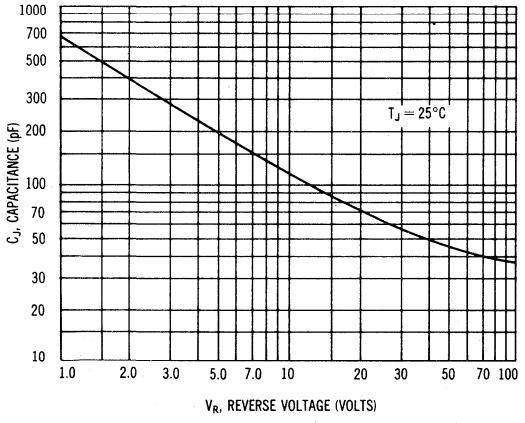


FIGURE 12 – FORWARD RECOVERY TIME

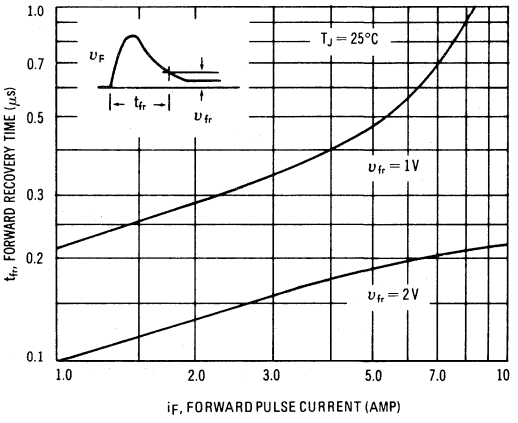
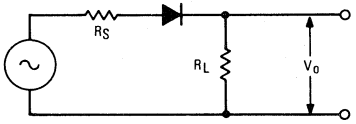


FIGURE 13 – SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 9 was calculated using the formula:

$$\sigma = \frac{P_{(dc)}}{P_{(rms)}} = \frac{\frac{V^2_{o(dc)}}{R_L}}{\frac{V^2_{o(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{o(dc)}}{V^2_{o(ac)} + V^2_{o(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 10) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 9.

It should be emphasized that Figure 9 shows waveform efficiency only; it does not provide a measure of diode losses. Data was obtained by measuring the ac component of V_0 with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 9.

MR810 thru MR814
MR816 thru MR818

Designers▲ Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 100 nanoseconds providing high efficiency at frequencies to 250 kHz.

FAST RECOVERY POWER RECTIFIERS
50-1000 VOLTS
1 AMPERE

DESIGNER'S DATA FOR "WORST CASE" CONDITIONS

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristic boundaries — are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	MR810	MR811	MR812	MR813	MR814	MR816	MR817	MR818	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	300	400	500	800	1000	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	100	200	300	400	500	800	1000	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	210	280	420	560	700	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75°C)	I_O	1.0								Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions) (T_A = 75°C)	I_{FSM}	30								Amps
Operating Junction Temperature Range	T_J	-65 to +150								°C
Storage Temperature Range	T_{stg}	-65 to +175								°C

THERMAL CHARACTERISTICS

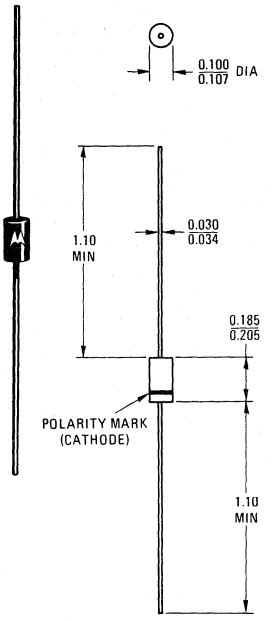
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Primted Circuit Board Mounting)	$R_{\theta JA}$	65	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (I_F = 3.14 Amp, T_J = 150°C)	v_F	–	1.1	1.2	Volts
Forward Voltage (I_F = 1.0 Amp, T_A = 25°C)	V_F	–	1.0	1.1	Volts
Reverse Current (rated dc voltage) T_A = 25°C T_A = 100°C	I_R	– –	1.0 50	10 100	μA

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21) (I_F = 20 mA, I_R = 2.0 mA, Tektronix S-Plug-In) (Figure 22)	t_{rr}	– –	500 1.0	750 3.0	ns μs
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	$I_{RM(REC)}$	–	–	3.0	Amp



All JEDEC dimensions and notes apply

CASE 59
DO-41

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded

FINISH: External leads are gold plated, leads are readily solderable

POLARITY: Cathode indicated by Polarity band

WEIGHT: 0.4 Grams (Approximately)

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE

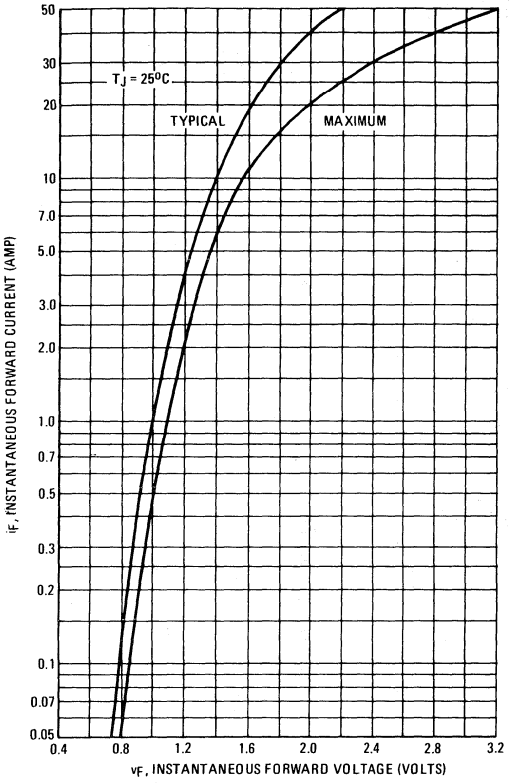


FIGURE 2 – MAXIMUM SURGE CAPABILITY

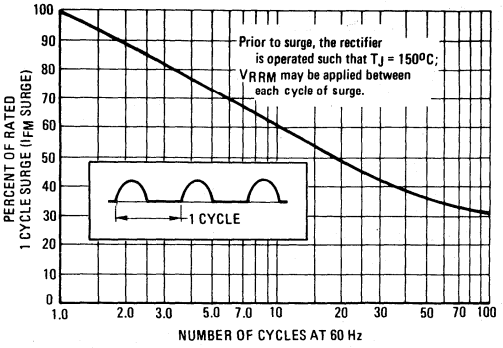


FIGURE 3 – TEMPERATURE COEFFICIENT

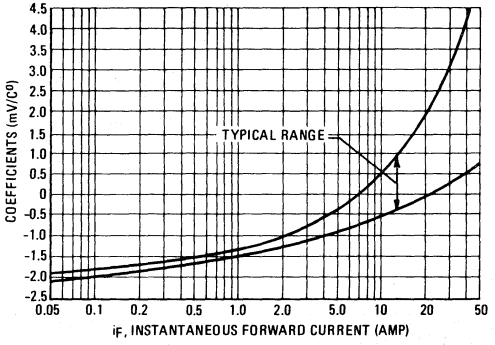


FIGURE 4 – FORWARD POWER DISSIPATION

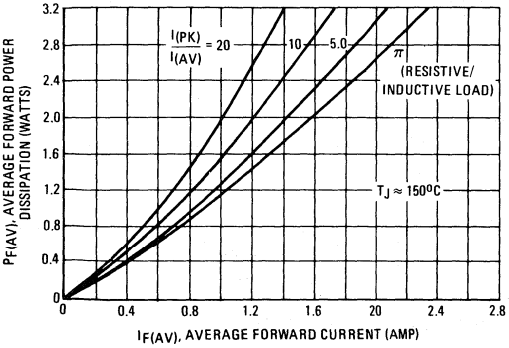
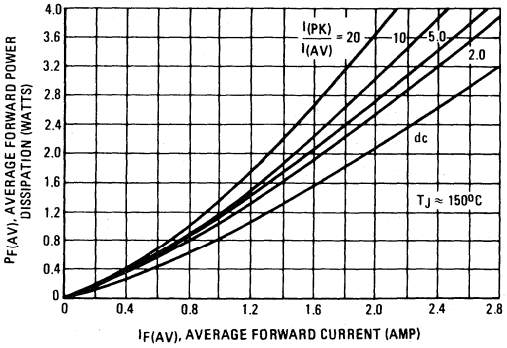


FIGURE 5 – FORWARD POWER DISSIPATION



MAXIMUM CURRENT RATINGS
(SEE NOTES 1 and 2)

SINE WAVE INPUT

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

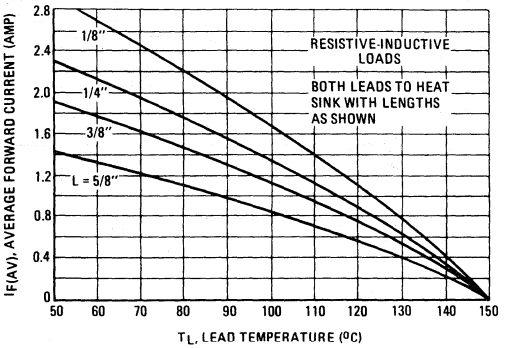


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

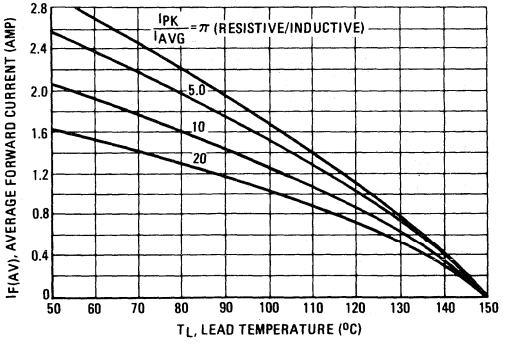
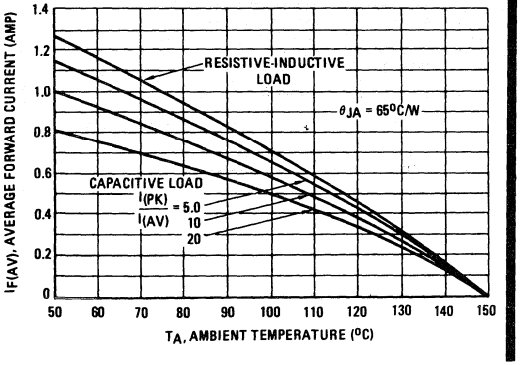


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUT

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

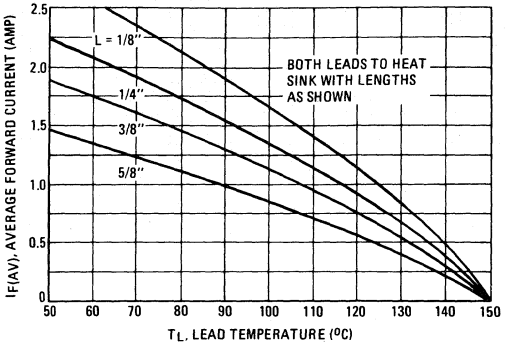


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

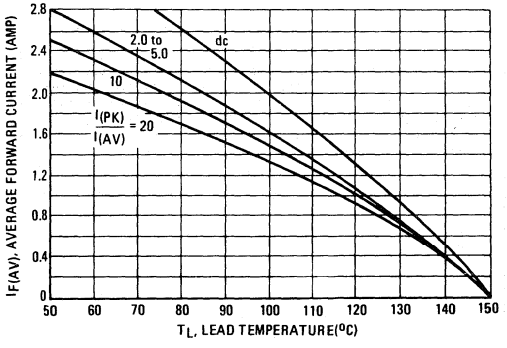


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

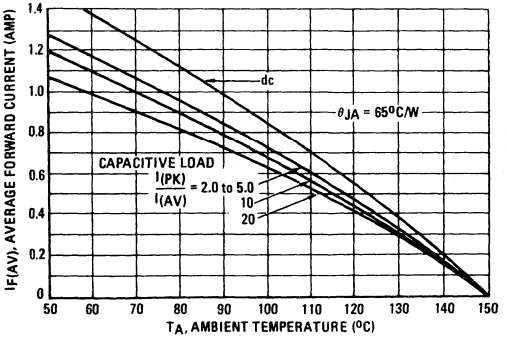


FIGURE 12 – THERMAL RESPONSE

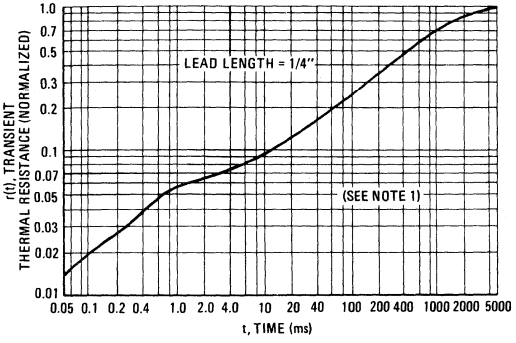
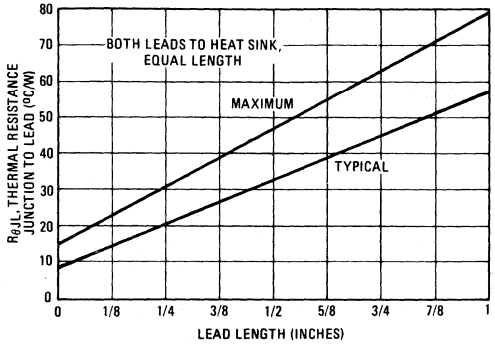
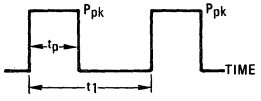


FIGURE 13 – THERMAL RESISTANCE



NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC}\left[D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)\right]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 12, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

NOTE 2

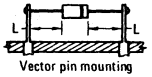
Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1

MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3

P. C. Board with 1-1/2" x 1-1/2" copper surface

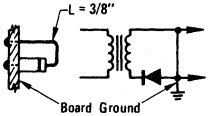
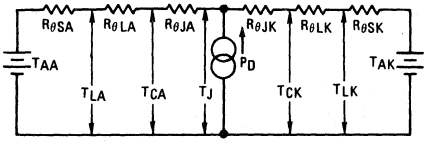


FIGURE 14 – THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$T_L = 150° - \Delta T_{JL}$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \simeq R_{\theta JL} \bullet P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 15 – FORWARD RECOVERY TIME

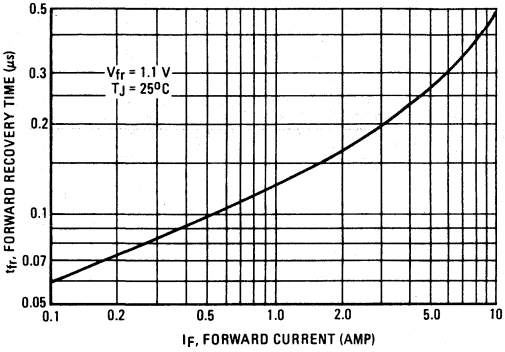
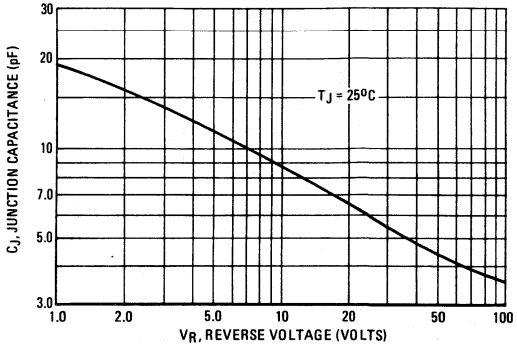


FIGURE 16 – JUNCTION CAPACITANCE



TYPICAL RECOVERED STORED CHARGE DATA
(SEE NOTE 3)

FIGURE 17 – T_J = 25°C

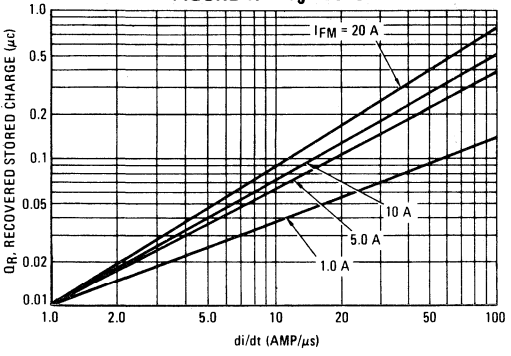


FIGURE 18 – T_J = 75°C

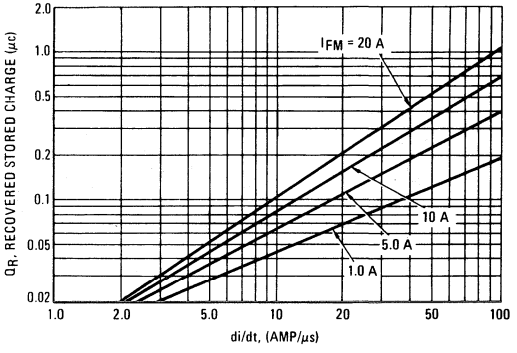


FIGURE 19 – T_J = 100°C

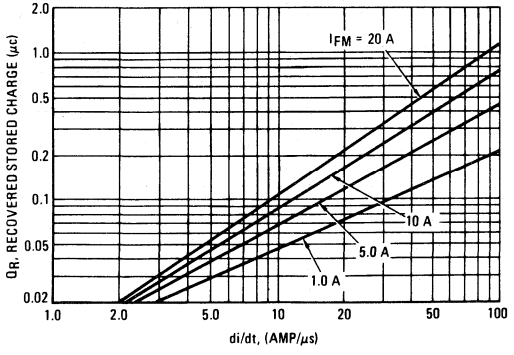


FIGURE 20 – T_J = 150°C

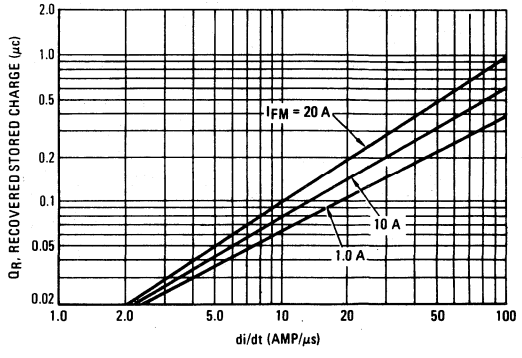


FIGURE 21 – REVERSE RECOVERY CIRCUIT

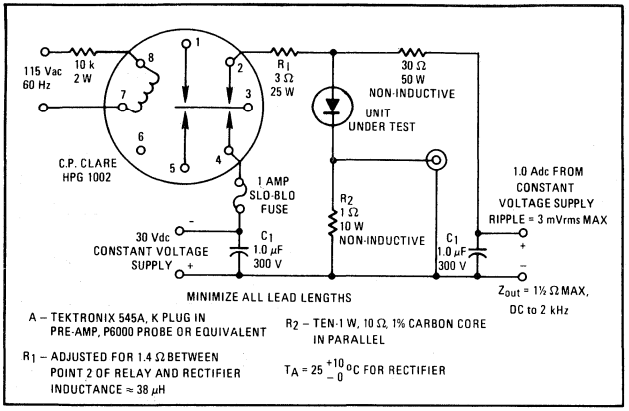
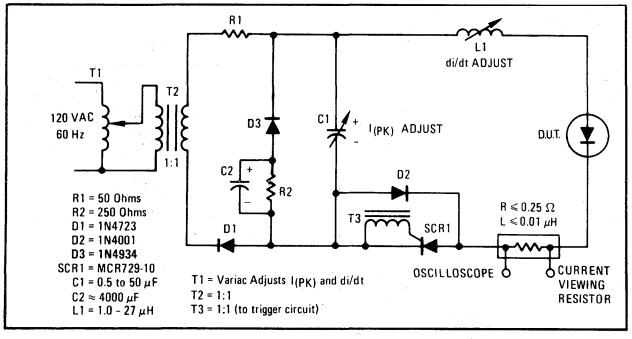


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT



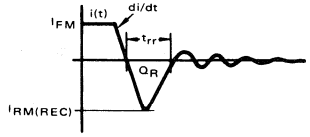
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

FIGURE 23 – TYPICAL REVERSE LEAKAGE

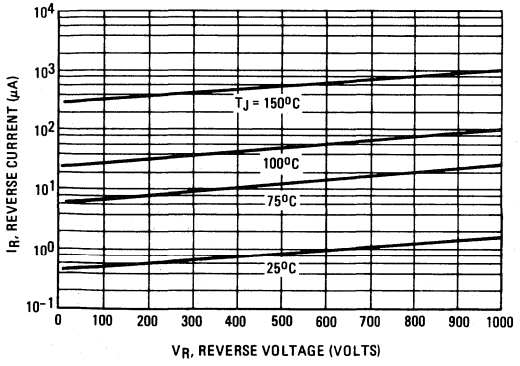
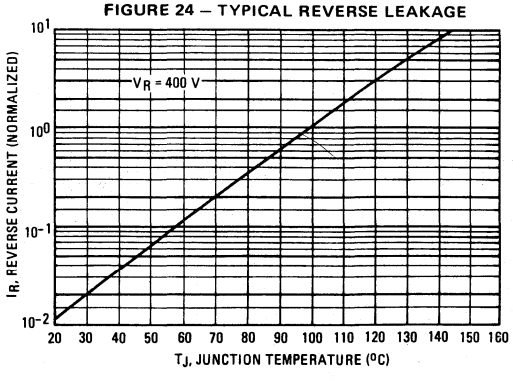


FIGURE 24 – TYPICAL REVERSE LEAKAGE



MR850 • MR851 • MR852
MR854 • MR856

Designers Data Sheet

SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 100 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	MR850	MR851	MR852	MR854	MR856	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	75	150	250	450	650	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	Volts
Average Rectified Forward Current (Single phase resistive load, T_A = 90°C) (1)	I_O	3.0					Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	100 (one cycle)					Amp
Operating and Storage Junction Temperature Range (2)	T_J,T_{stg}	-65 to +175					°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Recommended Printed Circuit Board Mouting, See Note 6, Page 8)	$R_{\theta JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

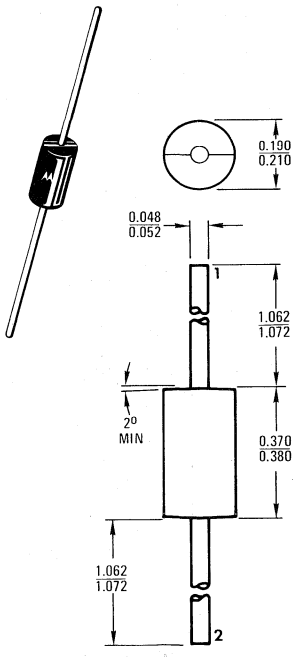
Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Forward Voltage (I_F = 9.4 Amp, T_J = 175°C)	v_F	–	0.9	1.1	Volts
Forward Voltage (I_F = 3.0 Amp, T_J = 25°C)	V_F	–	1.04	1.25	Volts
Reverse Current (rated dc voltage) T_J = 25°C	I_R	–	2.0	10	μA
T_J = 100°C MR850		–	–	150	
T_J = 100°C MR851		–	60	150	
T_J = 100°C MR852		–	–	200	
T_J = 100°C MR854		–	–	250	
T_J = 100°C MR856		–	100	300	

REVERSE RECOVERY CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25) (I_F = 15 Amp, di/dt = 10 A/μs, Figure 26)	t_{rr}	– –	100 150	200 300	ns
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc, Figure 25)	$I_{RM(REC)}$	–	–	2.0	Amp

(1) Must be derated for reverse power dissipation. See Note 2, Page 3.
(2) Derate as shown in Figure 1
▲Trademark of Motorola Inc.

FAST RECOVERY POWER RECTIFIERS
50-600 VOLTS
3 AMPERE



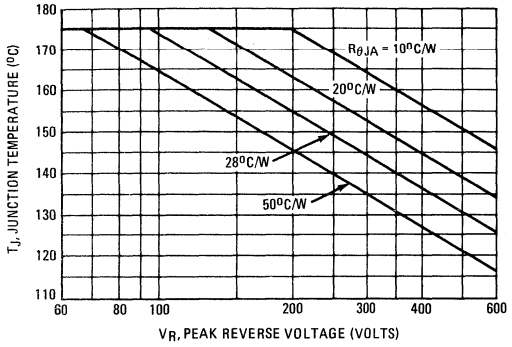
CASE 267

MECHANICAL CHARACTERISTICS

Case: Void Free, Transfer Molded
Finish: External Leads are Plated, Leads are readily Solderable
Polarity: Cathode Indicated by Polarity Band
Weight: 1.1 Grams (Approximately)
Maximum Lead Temperature for Soldering Purposes:
300°C, 1/8" from case for 10 s at 5.0 lb. tension

MAXIMUM CURRENT AND TEMPERATURE RATINGS

FIGURE 1 – MAXIMUM ALLOWABLE JUNCTION TEMPERATURE



NOTE 1
MAXIMUM JUNCTION TEMPERATURE DERATING

When operating this rectifier at junction temperatures over 120°C, reverse power dissipation and the possibility of thermal runaway must be considered. The data of Figure 1 is based upon worst case reverse power and should be used to derate $T_{J(max)}$ from its maximum value of 175°C. See Note 2 for additional information on derating for reverse power dissipation.

When current ratings are computed from $T_{J(max)}$ and reverse power dissipation is also included, ratings vary with reverse voltage as shown on Figures 2 thru 5.

RESISTIVE LOAD RATINGS

Printed Circuit Board Mounting – See Note 6, Page 8

FIGURE 2 – SINE WAVE INPUT

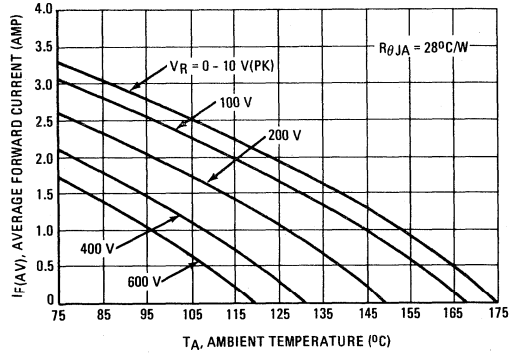


FIGURE 3 – SQUARE WAVE INPUT

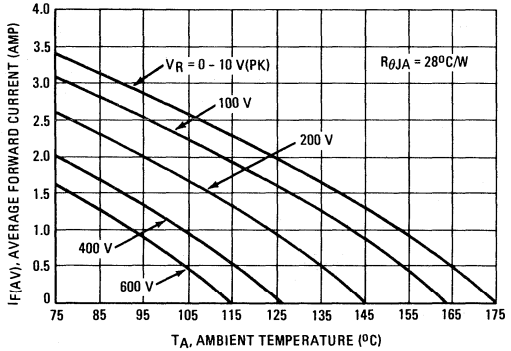


FIGURE 4 – SINE WAVE INPUT

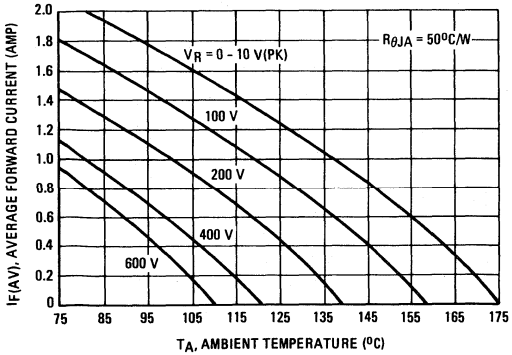
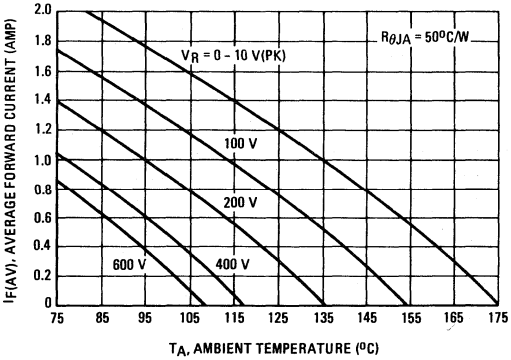


FIGURE 5 – SQUARE WAVE INPUT



MAXIMUM CURRENT RATINGS

Current derating data is based upon the thermal response data of Figure 29 and the forward power dissipation data of Figures 19 and 20. Since reverse power dissipation is not considered in Figures 6 thru 11, additional derating for reverse voltage and for junction to ambient thermal resistance must be applied. See Note 2.

SINE WAVE INPUTS

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

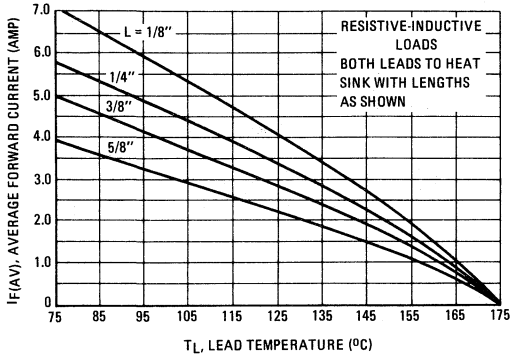


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

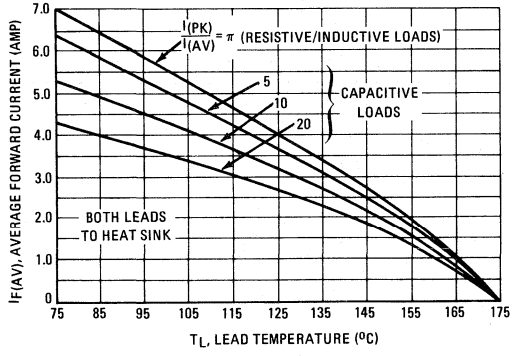
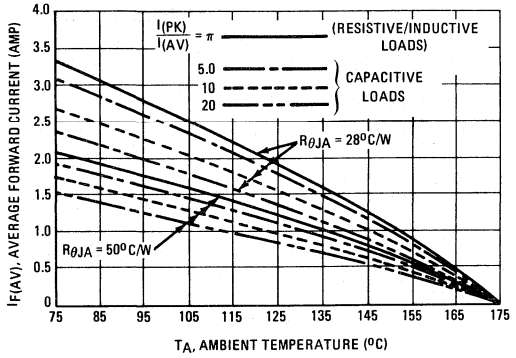


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUTS

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

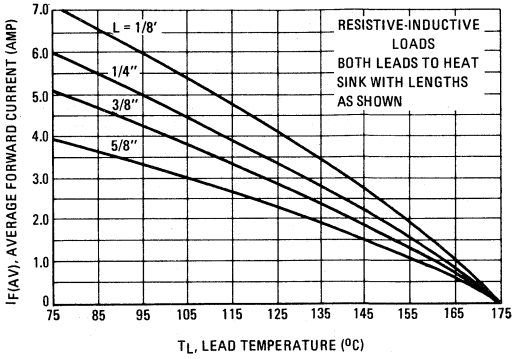


FIGURE 9 – 1/8" LEAD LENGTH, VARIOUS LOADS

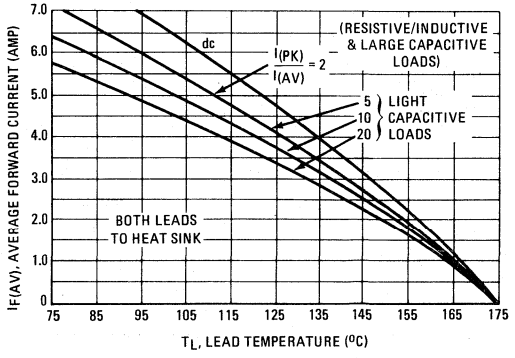
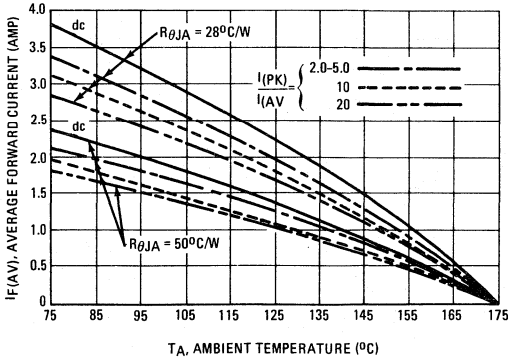


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



REVERSE POWER DISSIPATION AND CURRENT

NOTE 2
DERATING FOR REVERSE POWER DISSIPATION

In this rectifier, power loss due to reverse current is generally not negligible. For reliable circuit design, the maximum junction temperature must be limited to either 175°C or the temperature which results in thermal runaway. Proper derating may be accomplished by use of equation 1 or equation 2.

Equation 1 $T_A = T_1 - (175 - T_{J(max)}) - P_R R_{\theta JA}$

Where: T_1 = Maximum Allowable Ambient Temperature neglecting reverse power dissipation (from Figures 10 or 11)

$T_{J(max)}$ = Maximum Allowable Junction Temperature to prevent thermal runaway or 175°C, which ever is lower. (See Figure 1).

P_R = Reverse Power Dissipation (From Figure 12 or 13, adjusted for $T_{J(max)}$ as shown below)

$R_{\theta JA}$ = Thermal Resistance, Junction to Ambient.

When thermal resistance, junction to ambient, is over 20°C/W, the effect of thermal response is negligible. Satisfactory derating may be found by using:

Equation 2 $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$

P_F = Forward Power Dissipation (See Figures 19 & 20)

Other terms defined above.

The reverse power given on Figures 12 and 13 is calculated for $T_J = 150°C$. When T_J is lower, P_R will decrease; its value can be found by multiplying P_R by the normalized reverse current from Figure 14 at the temperature of interest.

The reverse power data is calculated for half wave rectification circuits. For full wave rectification using either a bridge or a center-tapped transformer, the data for resistive loads is equivalent when Vp is the line to line voltage across the rectifiers. For capacitive loads, it is recommended that the dc case on Figure 13 be used, regardless of input waveform, for bridge circuits. For capacitively loaded full wave center-tapped circuits, the 20:1 data of Figure 12 should be used for sine wave inputs and the capacitive load data of Figure 13 should be used for square wave inputs regardless of $I_{(pk)}/I_{(av)}$. For these two cases, Vp is the voltage across one leg of the transformer.

Example 1 Find maximum ambient temperature for I_{AV} = 2 A, capacitive load of I_{PK}/I_{AV} = 20, Input Voltage = 60 V (rms), sine wave, $R_{\theta JA}$ = 28°C/W, half wave circuit.

Solution 1 (using Equation 1)

Step 1: Find Vp; $V_P = \sqrt{2}\, V_{in}$ = 85 V, $V_{R(pk)}$ = 170

Step 2: Find $T_{J(max)}$ from Figure 1. Read $T_{J(max)}$ = 157°C

Step 3: Find $P_{R(max)}$ from Figure 12. Read P_R = 360 mW @ 150°C

Step 4: Find I_R normalized from Figure 14. Read $I_{R(norm)}$ = 1.5

Step 5: Correct P_R to $T_{J(max)}$. $P_R = I_{R(norm)} \times P_R$ (Figure 12) P_R = 1.5 x 360 = 540 mW

Step 6: Find $T_A = T_1$ from Figure 10. Read T_1 = 94°C

Step 7: Compute T_A from $T_A = T_1 - (175 - T_{J(max)} - P_R R_{\theta JA}$
$T_A = 94 - (175 - 157) - (0.54)(28)$
T_A = 61°C

Solution 2 (using Equation 2)

Steps 1 thru 5 are as Solution 1

Step 6: Find P_F from Figure 19. Read P_F = 3.0 W

Step 7: Compute T_A from $T_A = T_{J(max)} - (P_R + P_F) R_{\theta JA}$
$T_A = 157 - (0.54 + 3)28$
T_A = 58°C

The discrepancy occurs because thermal response is factored into solution 1, and advantage is taken of the cooling time after the power pulse and before reverse voltage achieves its maximum. 61°C is a satisfactory ambient temperature.

FIGURE 12 – REVERSE POWER DISSIPATION, SINE WAVE

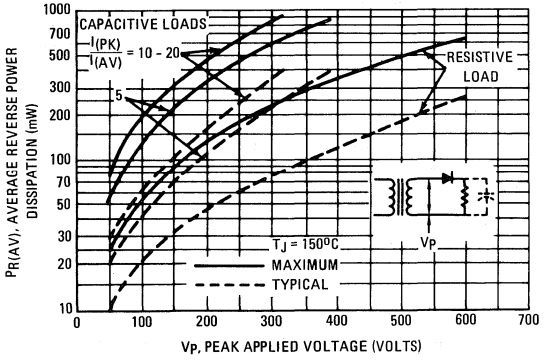


FIGURE 13 – REVERSE POWER DISSIPATION, SQUARE WAVE

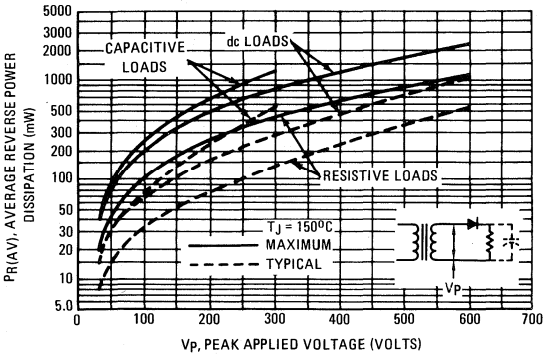


FIGURE 14 – NORMALIZED REVERSE CURRENT

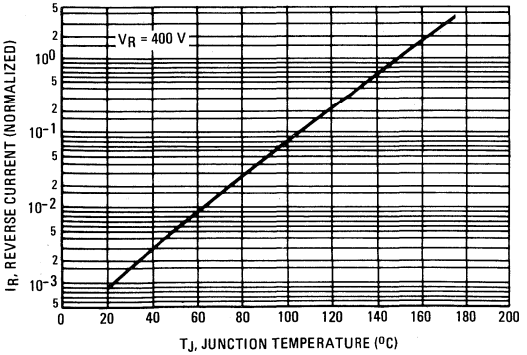
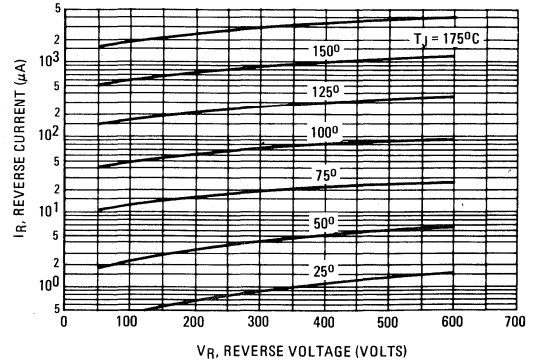


FIGURE 15 – TYPICAL REVERSE CURRENT



STATIC CHARACTERISTICS

FIGURE 16 – FORWARD VOLTAGE

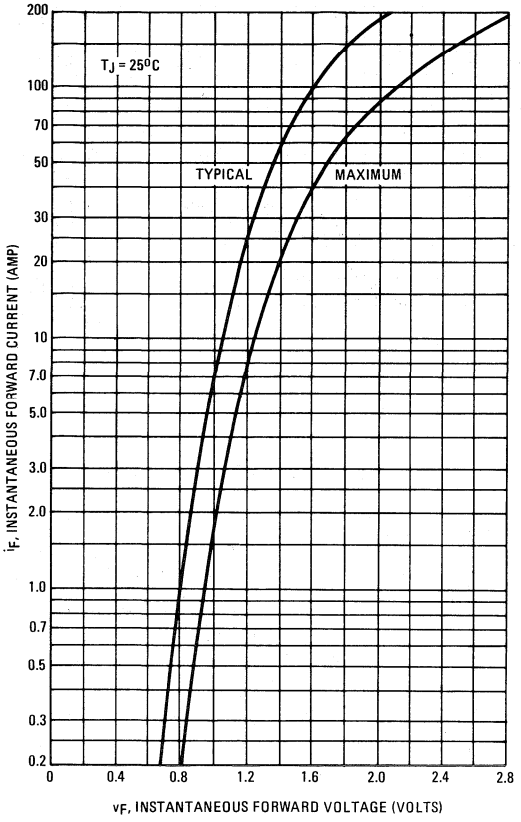


FIGURE 17 – MAXIMUM SURGE CAPABILITY

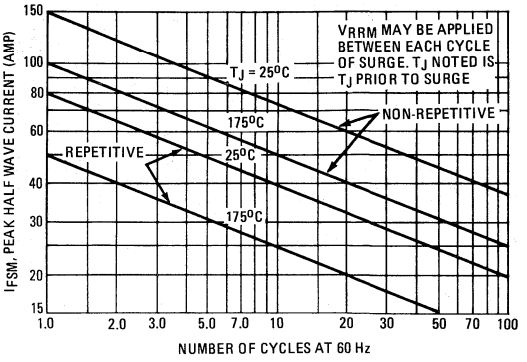
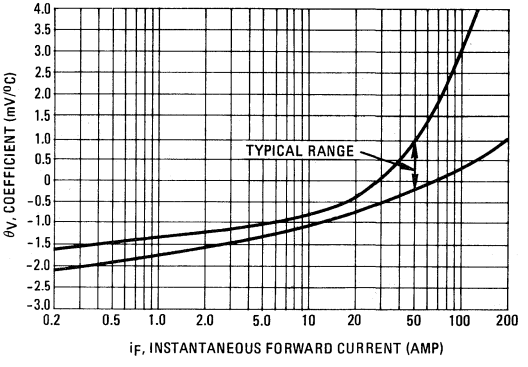
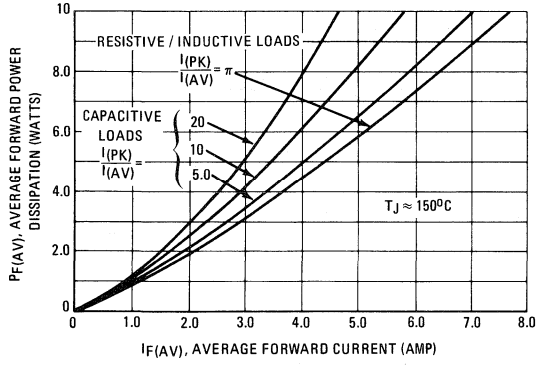


FIGURE 18 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



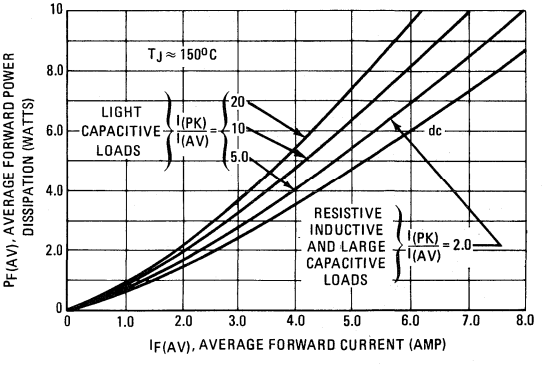
SINE WAVE INPUT

FIGURE 19 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 20 – FORWARD POWER DISSIPATION



TYPICAL RECOVERED STORED CHARAGE DATA

FIGURE 21 – T_J = 25°C (See Note 3)

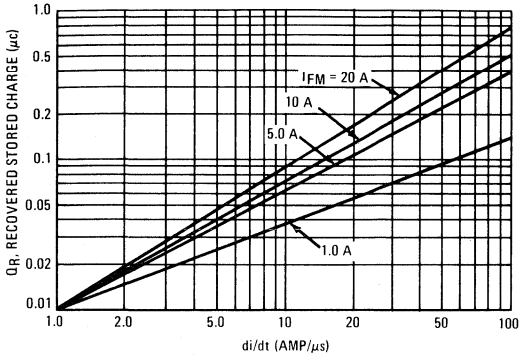


FIGURE 22 – T_J = 75°C

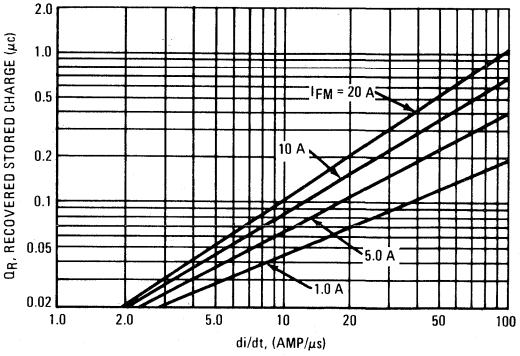


FIGURE 23 – T_J = 100°C

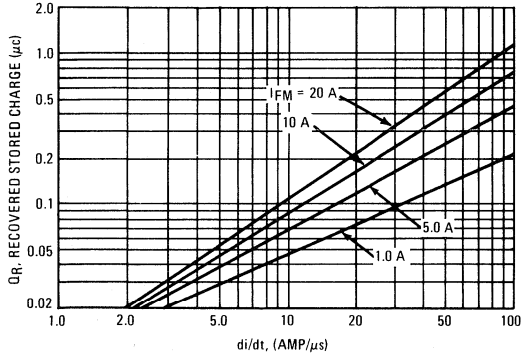
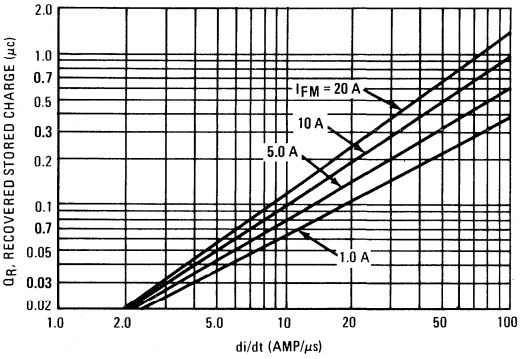


FIGURE 24 – T_J = 150°C



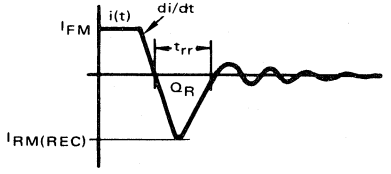
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



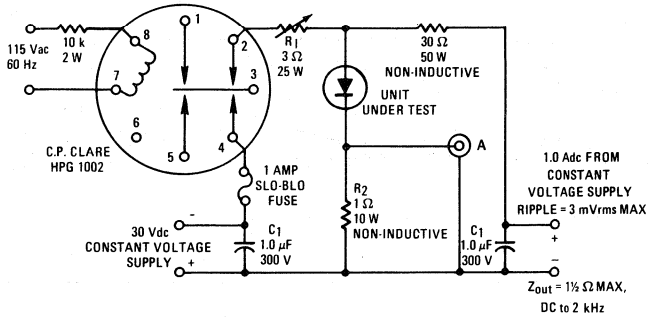
From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

DYNAMIC CHARACTERISTICS

FIGURE 25 – REVERSE RECOVERY CIRCUIT



MINIMIZE ALL LEAD LENGTHS

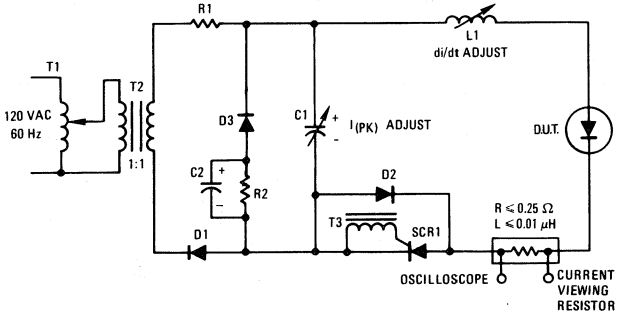
A – TEKTRONIX 545A, K PLUG IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 – ADJUSTED FOR 1.4 Ω BETWEEN POINT 2 OF RELAY AND RECTIFIER INDUCTANCE ≈ 38 μH

R_2 – TEN-1 W, 10 Ω, 1% CARBON CORE IN PARALLEL

$T_A = 25^{+10}_{-0}$°C FOR RECTIFIER

FIGURE 26 – JEDEC REVERSE RECOVERY CIRCUIT



R1 = 50 Ohms
R2 = 250 Ohms
D1 = 1N4723
D2 = 1N4001
D3 = 1N4934
SCR1 = MCR729-10
C1 = 0.5 to 50 μF
C2 ≈ 4000 μF
L1 = 1.0 - 27 μH

T1 = Variac Adjusts $I_{(PK)}$ and di/dt
T2 = 1:1
T3 = 1:1 (to trigger circuit)

FIGURE 27 – FORWARD RECOVERY TIME

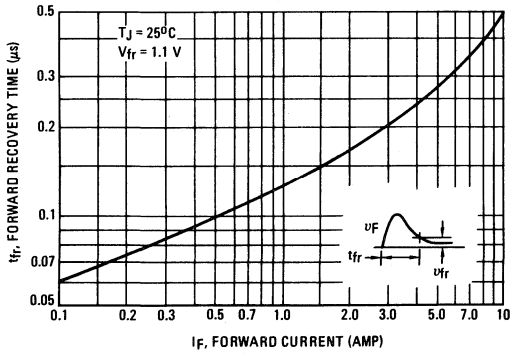


FIGURE 28 – JUNCTION CAPACITANCE

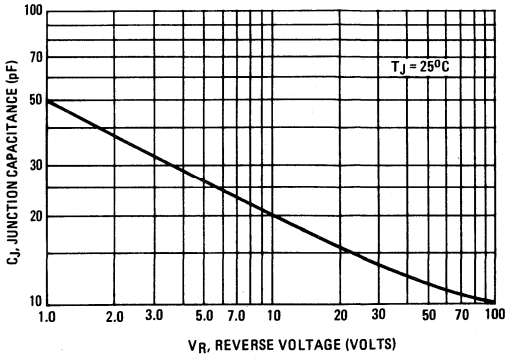


FIGURE 29 – THERMAL RESPONSE

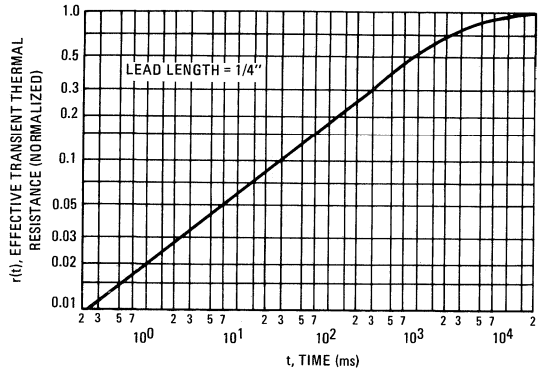
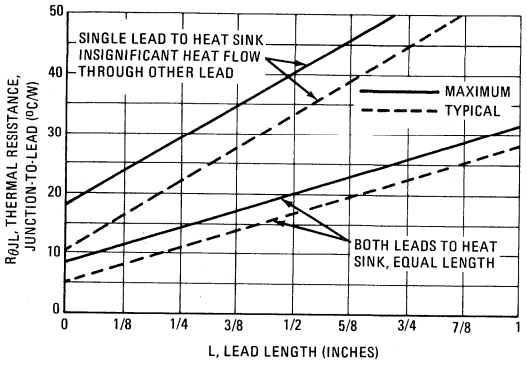


FIGURE 30 – STEADY-STATE THERMAL RESISTANCE



NOTE 4

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

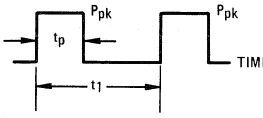
$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk} \cdot R_{\theta JL} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where r(t) = normalized value of transient thermal resistance at time t from Figure 29, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.



DUTY CYCLE = t_p/t_1
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

NOTE 5

Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 46°C/W/IN. Typically and 48°C/W/IN Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

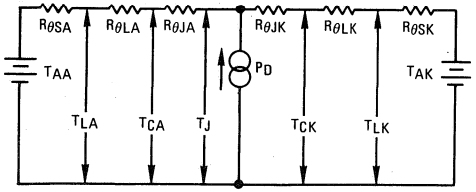
$$T_L = T_{J(max)} - \Delta T_{JL}$$

where

ΔT_{JL} can be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \cdot P_D$; P_D is the sum of forward and reverse power dissipation shown in Figures 2 and 4 for sine wave operation and Figures 3 and 5 for square wave operation.

THERMAL CIRCUIT MODEL
(For Heat Conduction Through the Leads)



NOTE 6

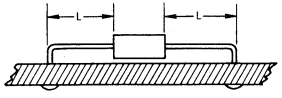
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

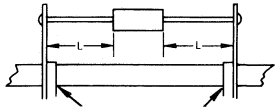
MOUNTING METHOD	LEAD LENGTH, L (IN)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.

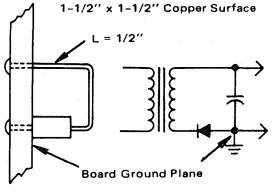


MOUNTING METHOD 2
Vector Pin Mounting



MOUNTING METHOD 3

P.C. Board with 1-1/2" x 1-1/2" Copper Surface



SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIRIER

. . . Designed for special applications such as power supplies, inverters, choppers, low RF interference and free wheeling diodes.

FAST RECOVERY SILICON POWER RECTIFIER

50-1000 VOLTS
3 AMPERES

MAXIMUM RATINGS

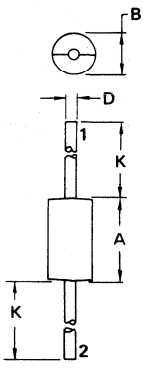
Rating	Sym.	MR 910	MR 911	MR 912	MR 913	MR 914	MR 916	MR 917	MR 918	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse DC Bloking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	300	400	600	800	1000	V
Non Repetitive Peak Reverse Voltage	V_{RSM}	100	200	300	400	500	800	1000	1200	V
Average Rectified Forward Current (T_A = 90 °C)	10	← 3.0 →								A
Non Repetitive Peak Surge Current	I_{FSM}	← 100 →								A
Operating Junction & Storage t°	T_j T_{stg}	← 65 to +150 →								°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal resistance, Junction to Ambient	$R\theta_{JA}$	28	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Forward Voltage (I_F = 3.0 A, T_j = 25 °C)	V_F		1.0	1.25	V
Reverse Current (rated DC Volt) (T_j = 25 °C) (T_j = 100 °C)	I_R		 3 100	 10 300	μA
Reverse Recovery Time	t_{rr}		300	750	nS
Reverse Recovery Current (I_F = 1 A, to V_R = 30)	$I_{RM\ (Rec)}$			3.0	Amp



STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.65	0.370	0.380
B	4.83	5.33	0.190	0.210
D	1.22	1.32	0.048	0.052
K	26.97	27.23	1.062	1.072

CASE 267-01

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded
FINISH: External leads are plated and readily solderable
POLARITY: Cathode indicated by Polarity band
WEIGHT: 1.1 grams (approximately)

MV104

VVC

SILICON EPICAP▲ DIODES

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configurations for minimum signal distortion and detuning. This device is supplied in the popular TO-92 plastic package for high volume, economical requirements of consumer and industrial applications.

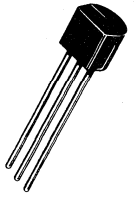
- Guaranteed Capacitance Range — 37-42 pF @ V_R = 3.0 Vdc
- Dual Diodes — Save Space and Reduce Cost
- TO-92 Package for Easy Handling and Mounting
- Guaranteed Matching* Tolerance From Diode to Diode and Group to Group
- Monolithic Chip Provides Near Perfect Matching — Guaranteed ±1% (Max) Over Specified Tuning Range.

*Upon request, diodes are available in matched sets of any number or in matched groups. All diodes in a set or group can be matched for capacitance to ±1.5% or 0.1 pF (whichever is greater) over the specified tuning range.

DUAL VOLTAGE-VARIABLE CAPACITANCE DIODES

37–42 pF

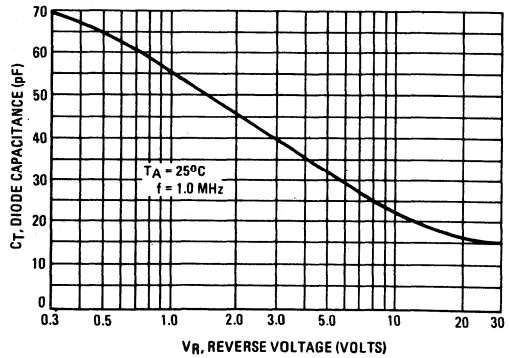
32 VOLTS

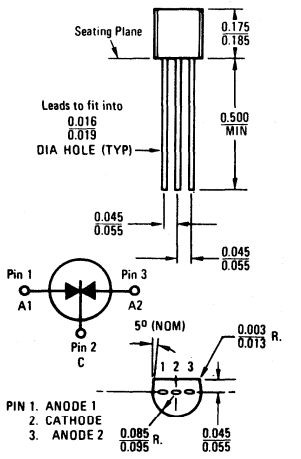


MAXIMUM RATINGS (Each Device)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	32	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — DIODE CAPACITANCE (Each Device)





To convert inches to millimeters multiply by 25.4

All JEDEC dimensions and notes apply

CASE 29-01 (15)
TO-92

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	32	–	–	Vdc
Reverse Voltage Leakage Current T_A = 25°C (V_R = 30 Vdc) T_A = 60°C	I_R	– –	– –	50 500	nAdc
Series Inductance (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	6.0	–	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.18	–	pF
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	400	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF		Q, Figure of Merit V_R = 3.0 Vdc f = 100 MHz	C_R, Capacitance Ratio C_3/C_{30} f = 1.0 MHz	
Device	Min	Max	Min	Min	Max
MV104	37	42	100	2.5	2.8

TYPICAL CHARACTERISTICS (Each Device)

FIGURE 2 – FIGURE OF MERIT

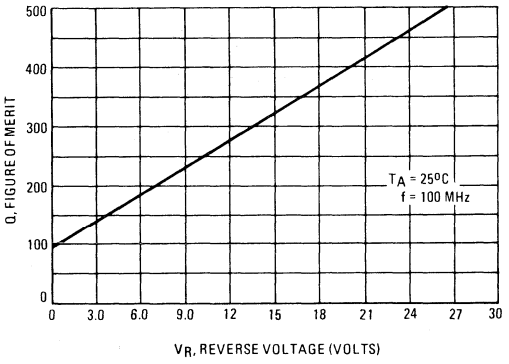


FIGURE 3 – FIGURE OF MERIT

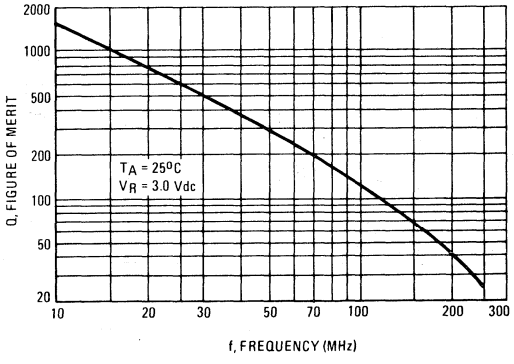


FIGURE 4 – DIODE CAPACITANCE

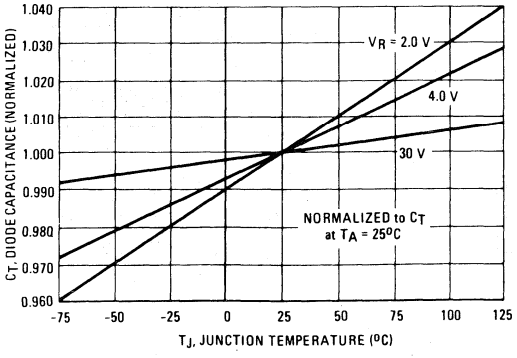
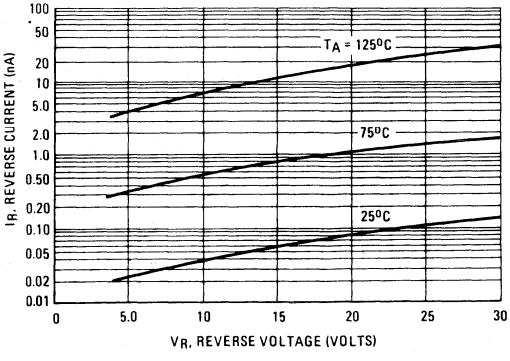


FIGURE 5 – REVERSE CURRENT



MV209

VVC

SILICON EPICAP▲ DIODE

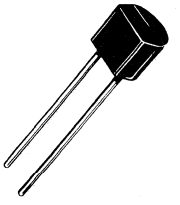
. . . designed for VHF TV tuning, AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q With Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Guaranteed Matching(1) Tolerance From Diode to Diode and Group to Group
- Supplied in One-Piece, Unibloc▲ Package for High Reliability.

(1)Upon request, diodes are available in matched sets of any number or in matched groups. All diodes in a set or group can be matched for capacitance to ±3% or 0.1 pF (whichever is greater) along the entire specified tuning range.

VOLTAGE VARIABLE CAPACITANCE DIODE

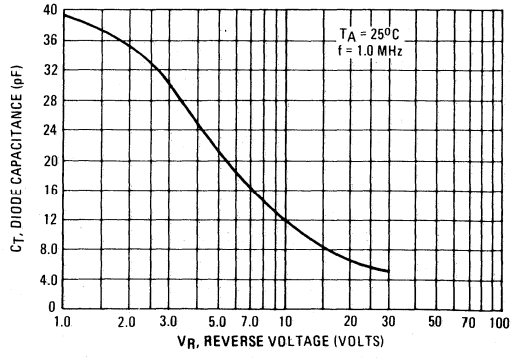
26-32 pF

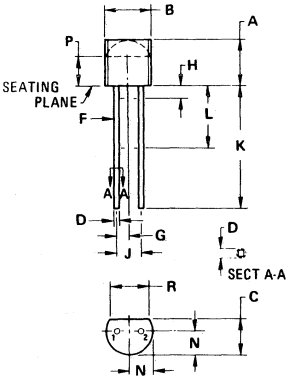


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE





STYLE 2:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply.

CASE 182-02

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc)	I_R	–	–	0.1	μAdc
Series Inductance (Note 1) (f = 250 MHz, Lead Length ≈ 1/8")	L_S	–	6.0	–	nH
Case Capacitance (Note 2) (f = 1.0 MHz)	C_C	–	0.2	–	pF
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	400	ppm/°C

	C_t, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 3)	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz (Note 4)	
Device	Min	Nom	Max	Min	Min	Max
MV209	26	29	32	200	5.0	6.5

FIGURE 2 – FIGURE OF MERIT

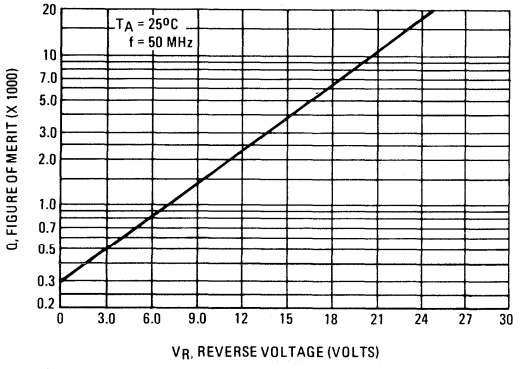


FIGURE 3 – LEAKAGE CURRENT

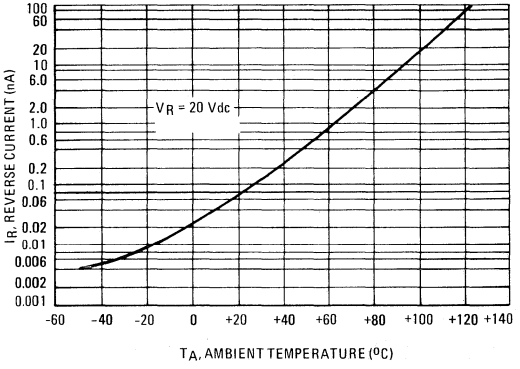
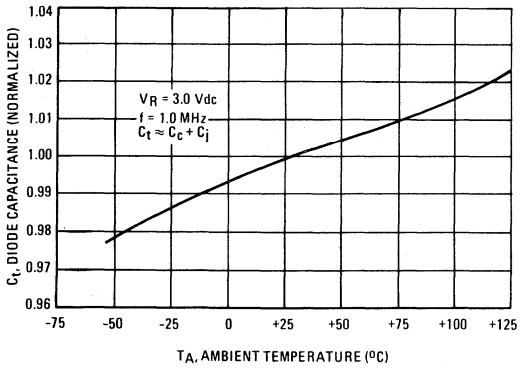


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_t measured at 3.0 Vdc divided by C_t measured at 25 Vdc.

MV1401 • MV1403
MV1404 • MV1405

VVC

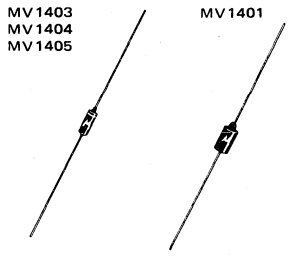
SILICON HYPER-ABRUPT JUNCTION
TUNING DIODES

. . . designed with a capacitance change of greater than TEN TIMES for a bias change ranging from 2 to 10 volts. Provides tuning over broad frequency ranges, tuning AM radio broadcast band, general AFC and tuning applications in lower RF frequencies.

- High Q with Guaranteed Minimum Values
- Broad Capacitance Selection from 120-550 pF (Nominal Values)
- Available in Two Standard Glass Packages

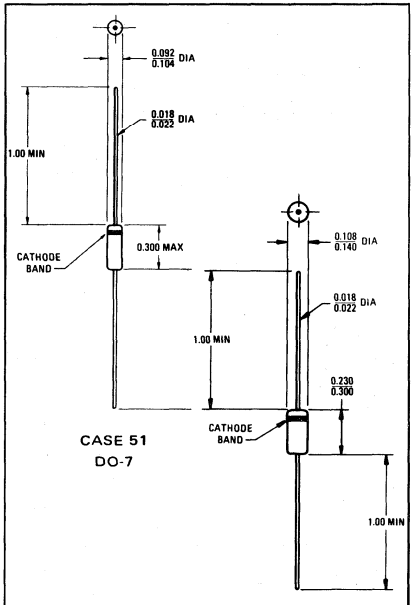
HIGH TUNING RATIO
VOLTAGE – VARIABLE
CAPACITANCE DIODES

120-550 pF
12 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	12	Volts
Forward Current	I_F	250	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	12	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 10 Vdc, T_A = 25°C)	I_R	–	–	0.10	μAdc
Series Inductance (f = 250 MHz, Lead Length ≈ 1/16")	L_S	–	5.0	–	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	–	0.25	–	pF

	C_T, Diode Capacitance						Q, Figure of Merit	TR, Tuning Ratio	
	V_R = 1.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz	C_1/C_{10} f = 1.0 MHz	C_2/C_{10} f = 1.0 MHz
Device	Min	Nom	Max	Min	Nom	Max	Min	Min	Min
MV1401	468	550	633	–	–	–	200	14	–
MV1403	–	–	–	140	175	210	200	–	10
MV1404	–	–	–	96	120	144	200	–	10
MV1405	–	–	–	200	250	300	200	–	10

PARAMETER TEST METHODS

1. **L_S, SERIES INDUCTANCE**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter).

2. **C_C, CASE CAPACITANCE**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. **C_T, DIODE CAPACITANCE**
   ($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

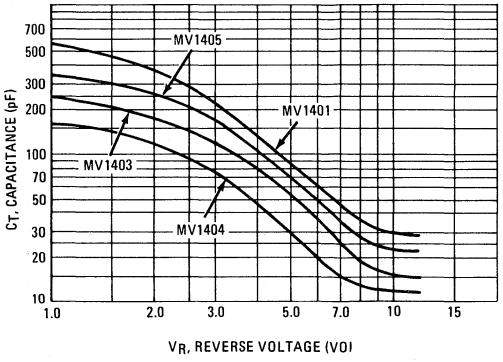
4. **TR, TUNING RATIO**
   TR is the ratio of C_T measured at 2.0 Vdc (1.0 Vdc for MV1401) divided by C_T measured at 10 Vdc.

5. **Q, FIGURE OF MERIT**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8). Use Lead Length ≈1/16".

FIGURE 1 – DIODE CAPACITANCE versus REVERSE VOLTAGE



MVAM115
MVAM125

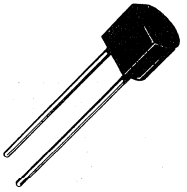
VVC

SILICON TUNING DIODE

. . . designed for electronic tuning of AM receivers.

- High Capacitance Ratio – C_R = 15 (Min)
- Guaranteed Diode Capacitance – C_t = 440 pF (Min) – 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz
- Guaranteed Figure of Merit – Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz

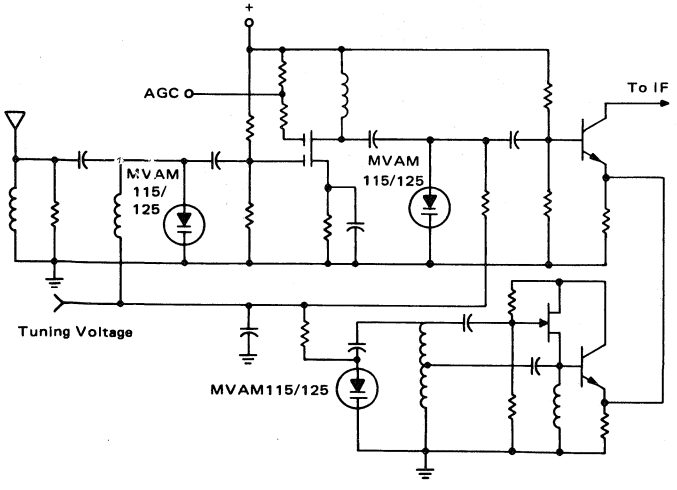
VARACTOR DIODES FOR AM TUNING

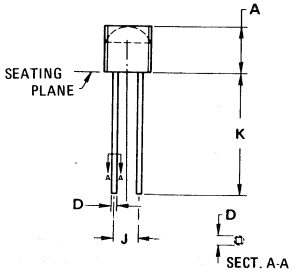


MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage	MVAM125 MVAM115	V_R	28 18	Volts
Forward Current		I_F	50	mA
Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	280 2.8	mW mW/°C
Operating and Storage Junction Temperature Range		T_J,T_{stg}	-65 to +125	°C

FIGURE 1 – TYPICAL AM RADIO APPLICATION





STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 182-03

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic – All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage (I_R = 10 μAdc)	MVAM125	$V_{(BR)}$	28	–	–	Vdc
	MVAM115		18	–	–	
Reverse Current		I_R	–	–	100	nAdc
(V_R = 25 V)	MVAM125					
(V_R = 15 V)	MVAM115					
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = -40°C to +85°C)		TC_C	–	435	–	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length 1/16")		C_C	–	0.18	–	pF
Diode Capacitance (2) (V_R = 1.0 Vdc, f = 1.0 MHz)		C_t	440	500	560	pF
Figure of Merit (V_R = 1.0 Vdc, f = 1.0 MHz)		Q	150	–	–	–
Capacitance Ratio (f = 1.0 MHz)	MVAM115	C1/C15	15	–	–	–
	MVAM125	C1/C25	15	–	–	

Notes:

(1) The effect of increasing temperature 1.0°C, at any operating point, is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from -40°C to +100°C.

(2) Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to ±1.5% or 0.1 pF (whichever is greater) at all points along the specified tuning range.

FIGURE 2 – CAPACITANCE versus REVERSE VOLTAGE

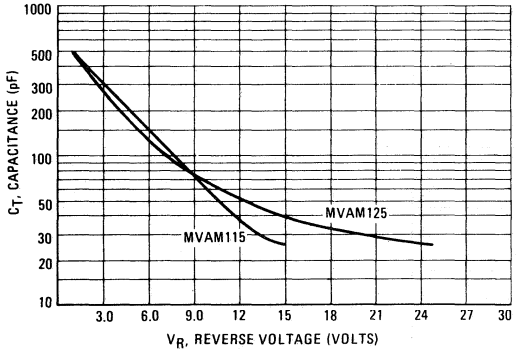
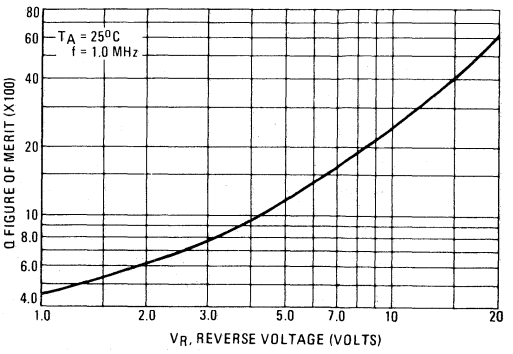


FIGURE 3 – FIGURE OF MERIT



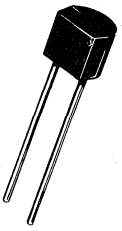
MVS240

MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE REFERENCE DIODE

Highly reliable temperature compensated monolithic integrated circuit voltage stabilizer designed for use in television and FM radios that use variable capacitance diode tuners.

- Low Dynamic Operating Impedance
- Low Operating Voltage Change over Temperature Range
- $\frac{\Delta V_Z}{\Delta T}$ = -0.20 mV/°C (Typ) @ I_{ZT} = 5.0 mA

24 VOLT STABILIZER



MAXIMUM RATINGS

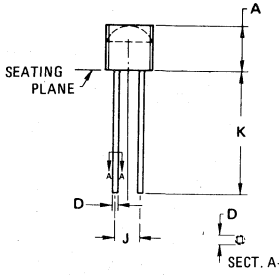
Rating	Symbol	Value	Unit
Operating Current for 24 Vz	I_Z	26	mA
Power Dissipation @ T_A = 25°C	P_D	625	mW
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.083	°C/mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	0.200	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage (I_{ZT} = 5.0 mA)	V_Z	23	24	25	Volts
Operating Voltage Change (I_{ZT} = 5.0 mA, 0 to 70°C)	$\frac{\Delta V_Z}{\Delta T}$	-1.55	-0.20	+1.55	mV/°C
Operating Dynamic Impedance (I_Z = 5.0 mA)	Z_z	—	9.0	25	Ohms



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	—	0.500	—

CASE 182-03

FIGURE 1 – POWER DERATING

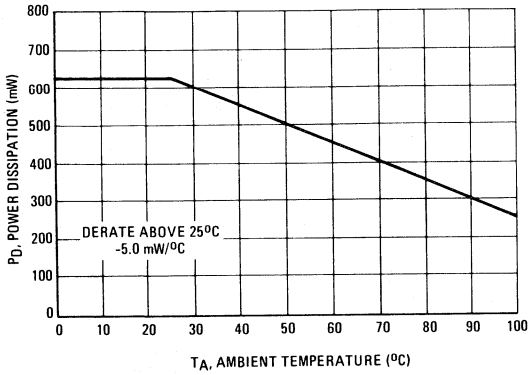


FIGURE 2 – CURRENT DERATING

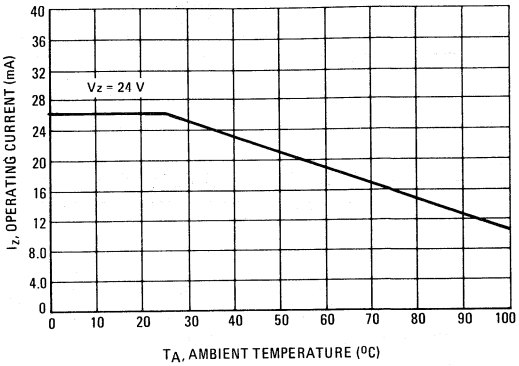


FIGURE 3 – OPERATING VOLTAGE CHANGE

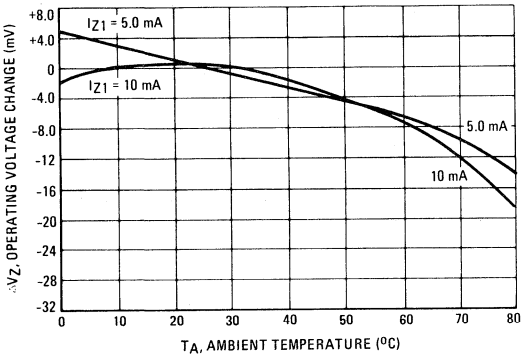


FIGURE 4 – OPERATING VOLTAGE CHANGE TEST CIRCUIT

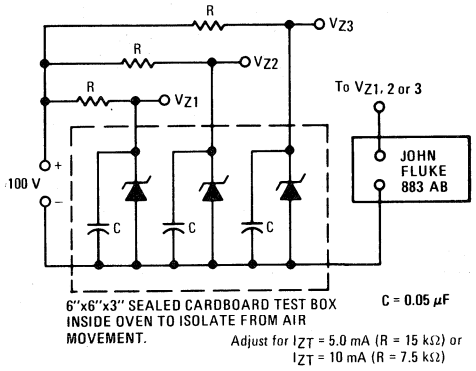


FIGURE 5 – OPERATING IMPEDANCE TEST CIRCUIT

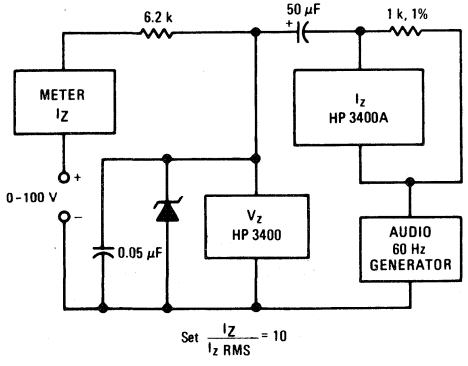
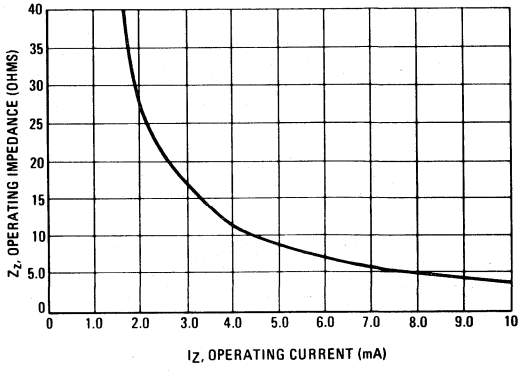


FIGURE 6 – OPERATING IMPEDANCE



MVS460

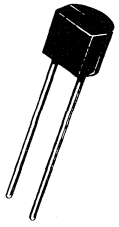
MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE REFERENCE DIODE

Highly reliable temperature compensated monolithic integrated circuit voltage stabilizer designed for use in television and FM radios that use variable capacitance diode tuners.

- Low Dynamic Operating Impedance
- Low Operating Voltage Change over Temperature Range
- Available in the Following Voltage Ranges:

31 to 32 volts	MVS460-1	red top
32 to 34 volts	MVS460-2	yellow top
34 to 35 volts	MVS460-3	green top

TUNING DIODE REGULATOR



MAXIMUM RATINGS

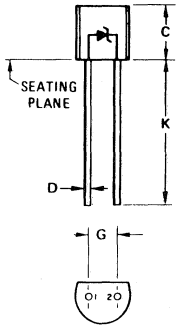
Rating	Symbol	Value	Unit
Operating Current for 33 V_Z	I_Z	18	mA
Power Dissipation @ $T_A = 25^oC$	P_D	625	mW
Operating Junction Temperature	T_J	150	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.083	$^oC/mW$
Thermal Resistance, Junction to Ambient	θ_{JA}	0.200	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage (I_{ZT} = 5.0 mA)	V_Z	31	33	35	Volts
Operating Voltage Change (I_{ZT} = 5.0 mA, 0 to 70°C)	$\frac{\Delta V_Z}{\Delta T}$	-3.1	-2.3	+1.55	mV/°C
Operating Dynamic Impedance (I_Z = 5.0 mA)	Z_z	–	9.0	25	Ohms



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
C	0.175	0.185	4.45	4.70
D	0.016	0.019	0.406	0.483
G	0.090	0.110	2.29	2.79
K	0.594		15.09	

CASE 182-01

FIGURE 1 – POWER DERATING

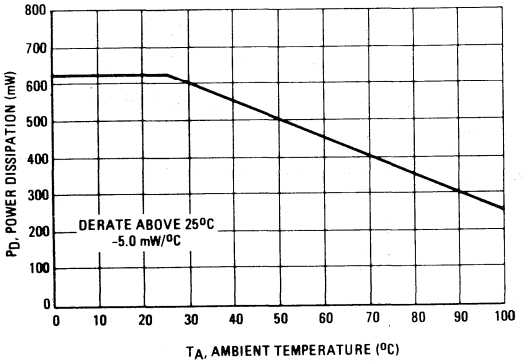


FIGURE 2 – CURRENT DERATING

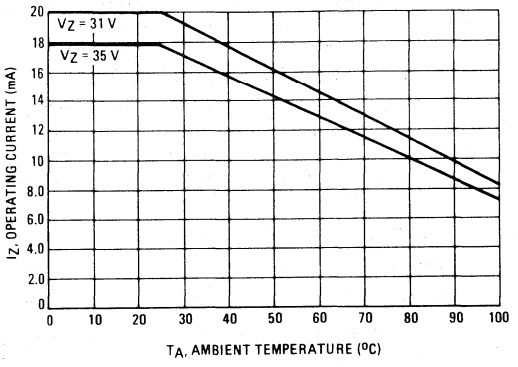


FIGURE 3 – OPERATING VOLTAGE CHANGE

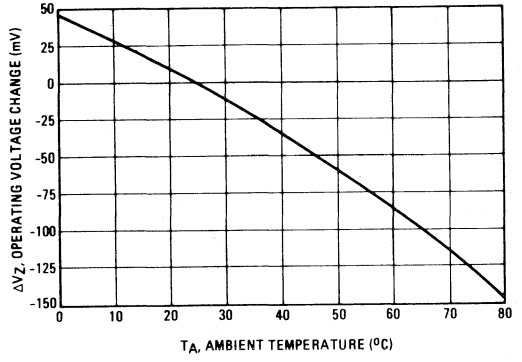


FIGURE 4 – OPERATING VOLTAGE CHANGE TEST CIRCUIT

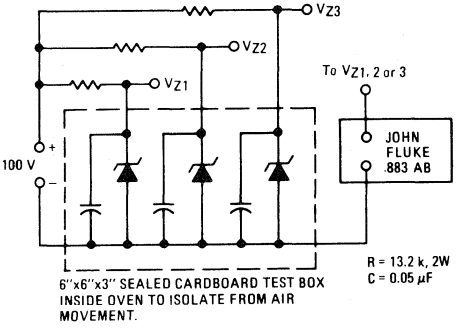


FIGURE 5 – OPERATING IMPEDANCE TEST CIRCUIT

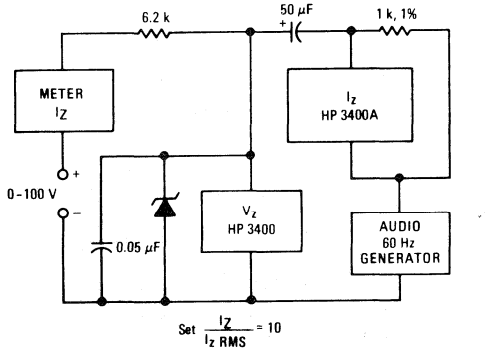
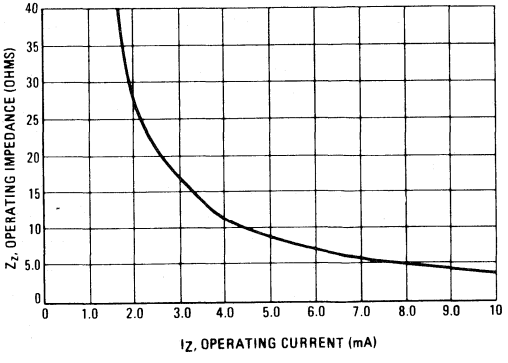


FIGURE 6 – OPERATING IMPEDANCE



MZD3.9 thru MZD200

Designers▲ Data Sheet

1.3 WATT SURMETIC▲ 30 SILICON ZENER DIODES

. . . a complete series of 1.3 Watt Zener Diodes with limits and operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- To 80 Watts Surge Rating @ 1.0 ms
- Maximum Limits Guaranteed on Six Electrical Parameters
- Package No Larger Than the Conventional 400 mW Package

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.3 7.4	Watt mW/°C
DC Power Dissipation @ T_L = 75°C Lead Length = 10 mm Derate above 75°C	P_D	3.0 24	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

FINISH: All external surfaces are corrosion resistant and leads are readily solderable and weldable

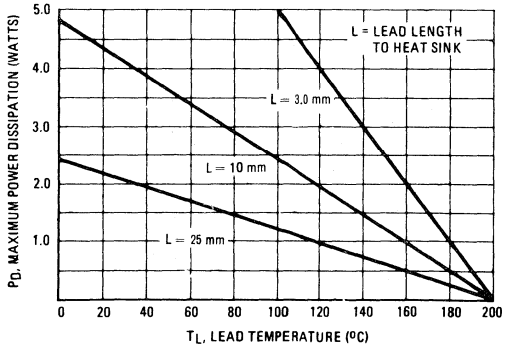
POLARITY: Cathode indicated by polarity band. When operated in zener mode, cathode will be positive with respect to anode

MOUNTING POSITION: Any

WEIGHT: 0.4 gram (approx)

Note 1: Lead Temperature not less than 2.0 mm from case for 10 seconds: 230°C.

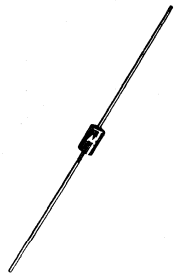
FIGURE 1 – POWER-TEMPERATURE DERATING CURVE

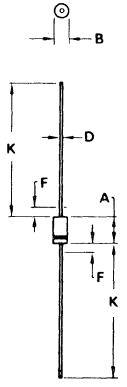


▲Trademark of Motorola Inc.

1.3 WATT, 5%
ZENER REGULATOR DIODES

3.9-200 VOLTS





NOTE:
1. POLARITY DENOTED BY CATHODE BAND

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	–	1.27	–	0.050
K	27.94	–	1.100	–

All JEDEC dimensions and notes apply.

CASE 59-03
DO-41
"SURMETIC"

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.) V_F = 1.5 V max, I_F = 200 mA for all types.

Type No. (Note 1)	Zener Voltage (Note 2) Min	Zener Voltage (Note 2) Max	Test Current I_{ZT} mA	Zener Impedance at I_{ZT} f = 1000 Hz Typ	Zener Impedance at I_{ZT} f = 1000 Hz Max	Blocking Voltage I_R = 1.0 μA	Typical T_C %/°C	Surge Current @ T_L = 25°C i_R – mA (Note 3)
MZD3.9	3.7	4.1	100	3.8	7.0	–	-0.060	1380
MZD4.3	4.0	4.6	100	3.8	7.0	–	±0.055	1260
MZD4.7	4.4	5.0	100	3.8	7.0	–	±0.030	1190
MZD5.1	4.8	5.4	100	2.0	5.0	–	±0.030	1070
MZD5.6	5.2	6.0	100	1.0	2.0	1.5	+0.038	970
MZD6.2	5.8	6.6	100	1.0	2.0	1.5	+0.045	890
MZD6.8	6.4	7.2	100	1.0	2.0	2.0	+0.050	810
MZD7.5	7.0	7.9	100	1.0	2.0	2.0	+0.058	730
MZD8.2	7.7	8.7	100	1.0	2.0	3.5	+0.062	660
MZD9.1	8.5	9.6	50	2.0	4.0	3.5	+0.068	605
MZD10	9.4	10.6	50	2.0	4.0	5.0	+0.075	550
MZD11	10.4	11.6	50	4.0	7.0	5.0	+0.076	500
MZD12	11.4	12.7	50	4.0	7.0	7.0	+0.077	454
MZD13	12.4	14.1	50	5.0	10	7.0	+0.079	414
MZD15	13.8	15.8	50	5.0	10	10	+0.082	380
MZD16	15.3	17.1	25	6.0	15	10	+0.083	344
MZD18	16.8	19.1	25	6.0	15	10	+0.085	304
MZD20	18.8	21.2	25	6.0	15	10	+0.086	285
MZD22	20.8	23.3	25	6.0	15	12	+0.087	250
MZD24	22.8	25.6	25	7.0	15	12	+0.088	225
MZD27	25.1	28.9	25	7.0	15	14	+0.090	205
MZD30	28.0	32	25	8.0	15	14	+0.091	190
MZD33	31	35	25	8.0	15	17	+0.092	170
MZD36	34	38	10	21	40	17	+0.093	150
MZD39	37	41	10	21	40	20	+0.094	135
MZD43	40	46	10	24	45	20	+0.095	125
MZD47	44	50	10	24	45	24	+0.095	115
MZD51	48	54	10	25	60	24	+0.096	110
MZD56	52	60	10	25	60	28	+0.096	95
MZD62	58	66	10	25	80	28	+0.097	90
MZD68	64	72	10	25	80	34	+0.097	80
MZD75	70	79	10	30	100	34	+0.098	70
MZD82	77	88	10	30	100	41	+0.098	65
MZD91	85	96	5.0	60	200	41	+0.099	60
MZD100	94	106	5.0	60	200	50	+0.110	55
MZD110	104	116	5.0	80	250	50	+0.110	50
MZD120	114	127	5.0	80	250	60	+0.110	45
MZD130	124	141	5.0	110	300	60	+0.110	–
MZD150	138	156	5.0	110	300	75	+0.110	–
MZD160	153	171	5.0	150	350	75	+0.110	–
MZD180	168	191	5.0	150	350	90	+0.110	–
MZD200	188	212	5.0	150	350	90	+0.110	–

NOTE 1 – TOLERANCE AND TYPE NUMBER DESIGNATION

The type numbers listed have a standard tolerance on the nominal zener voltage of ±5%.

A suffix "C" indicates a ±2% tolerance; suffix "D" indicates a ±1% tolerance.

NOTE 2 – ZENER VOLTAGE (V_Z) MEASUREMENT

The zener voltage is measured after the test current (I_{ZT}) has been applied for 40 ± 10 milliseconds, while maintaining a lead temperature (T_L) of 30°C at a point of 10 mm from the diode body.

NOTE 3 – (I_R) NON-REPETITIVE SURGE CURRENT

Maximum peak, non-repetitive reverse surge current of half square wave or equivalent sine wave pulse of 50 ms duration, superimposed on the test current (I_{ZT}).

FIGURE 2 – TYPICAL THERMAL RESPONSE L, LEAD LENGTH = 10 mm

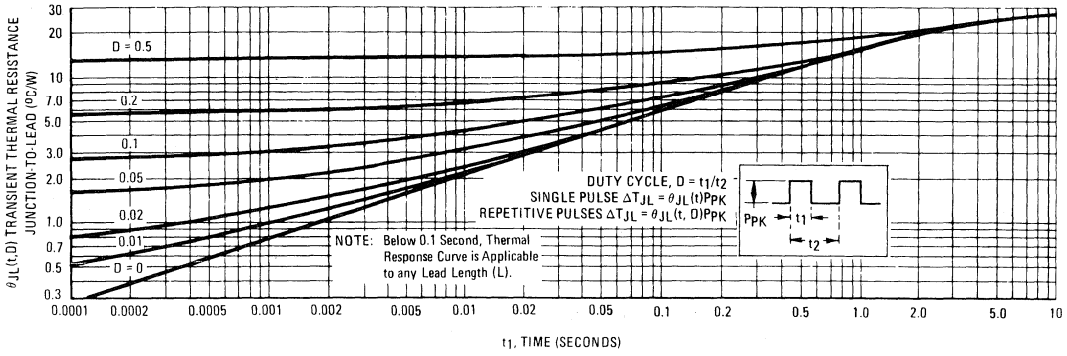


FIGURE 3 – TYPICAL THERMAL RESISTANCE

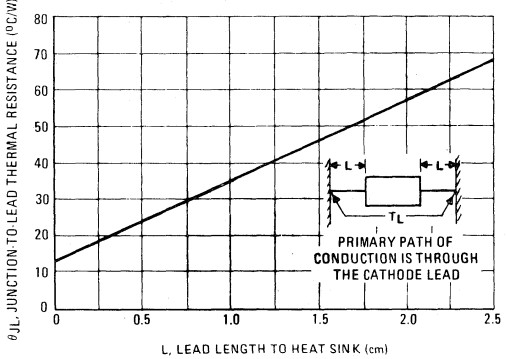


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE POWER

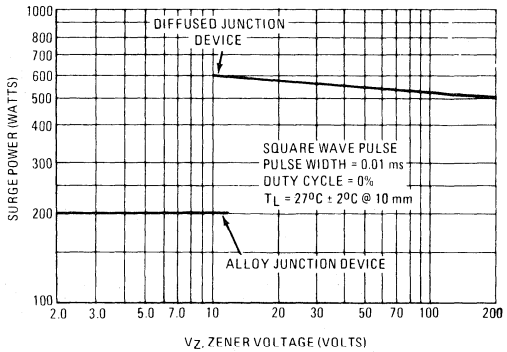
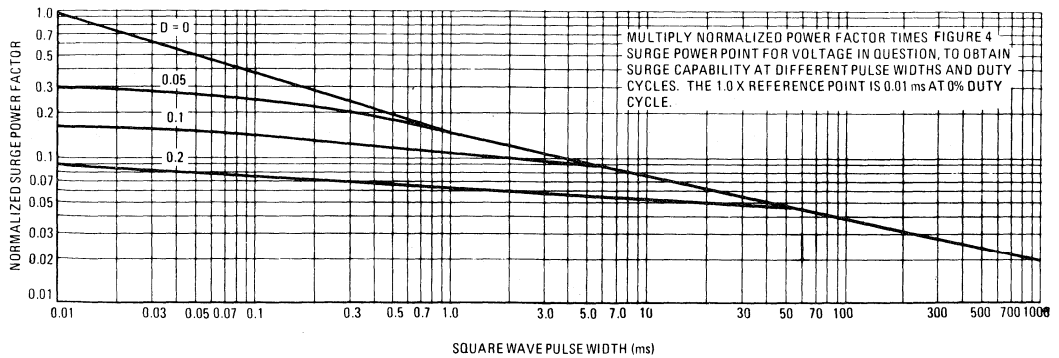


FIGURE 5 – SURGE POWER FACTOR



TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% OF THE UNITS ARE IN THE RANGES INDICATED)

FIGURE 6 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS TO 12 VOLTS

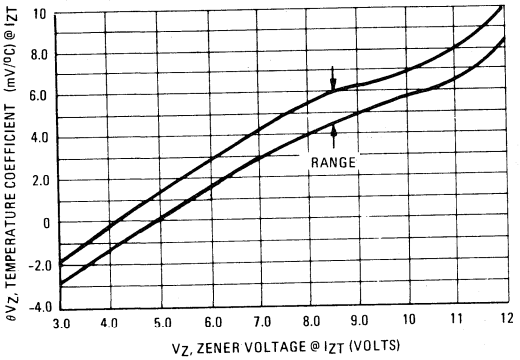


FIGURE 7 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 200 VOLTS

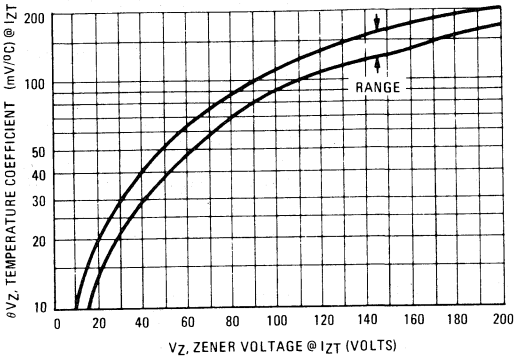
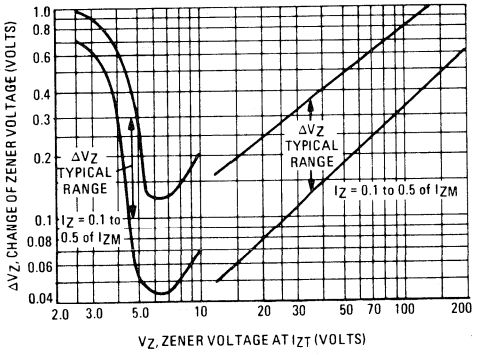


FIGURE 8 – VOLTAGE REGULATION



1N4001 thru 1N4007

Designers▲ Data Sheet

"SURMETIC"▲ RECTIFIERS

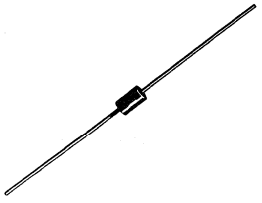
. . . subminiature size, axial lead mounted rectifiers for general-purpose low-power applications.

Designers Data for "Worst Case" Conditions

The Designers▲ Data Sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

LEAD MOUNTED SILICON RECTIFIERS

50-1000 VOLTS DIFFUSED JUNCTION



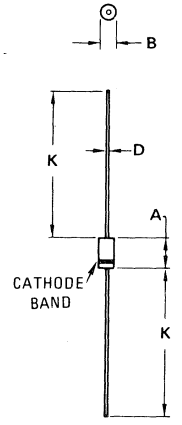
*MAXIMUM RATINGS

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 8, T_A = 75°C)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	I_{FSM}	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

*ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 1.0 Amp, T_J = 25°C) Figure 1	v_F	0.93	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$V_{F(AV)}$	–	0.8	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	 0.05 1.0	 10 50	μA
Maximum Full-Cycle Average Reverse Current (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads	$I_{R(AV)}$	–	30	μA

*Indicates JEDEC Registered Data.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59-04
Does Not Conform to DO-41 Outline.

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" from case for 10 seconds at 5 lbs. tension
FINISH: All external surfaces are corrosion-resistant, leads are readily solderable
POLARITY: Cathode indicated by color band
WEIGHT: 0.40 Grams (approximately)

▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE

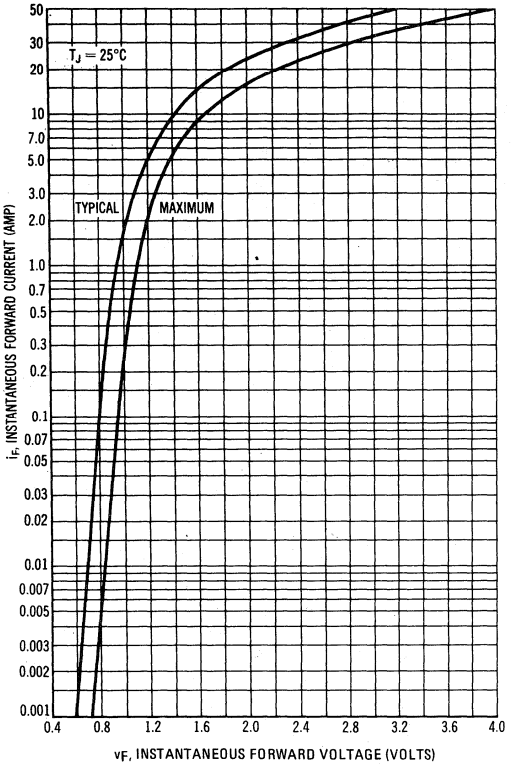


FIGURE 2 – NON-REPETITIVE SURGE CAPABILITY

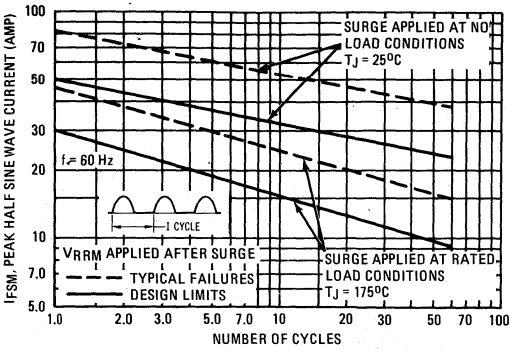


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT

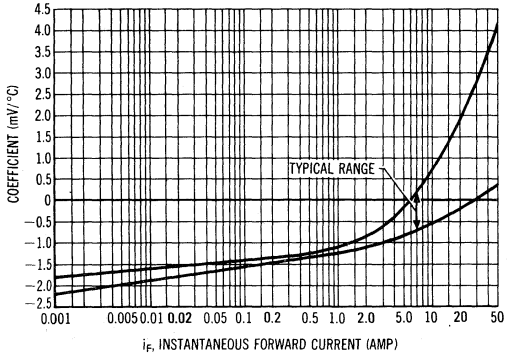
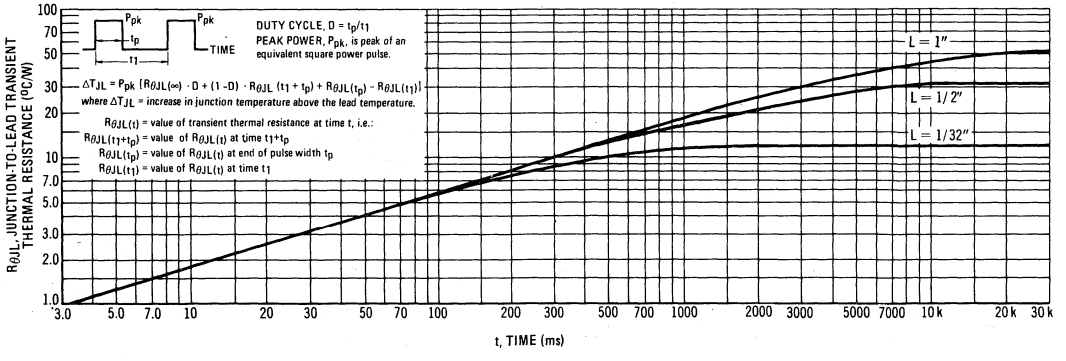


FIGURE 4 – TYPICAL TRANSIENT THERMAL RESISTANCE



The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

CURRENT DERATING DATA

FIGURE 5 – FORWARD POWER DISSIPATION

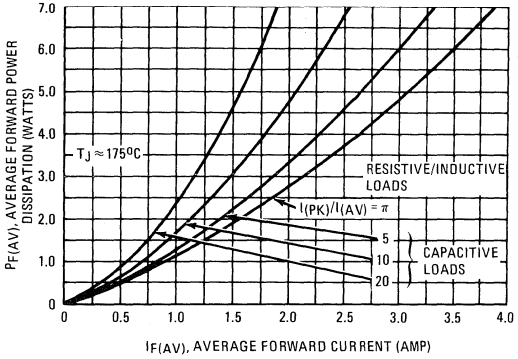


FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

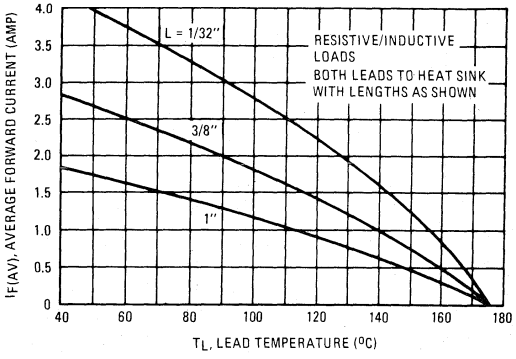


FIGURE 7 – 3/8" LEAD LENGTH, VARIOUS LOADS

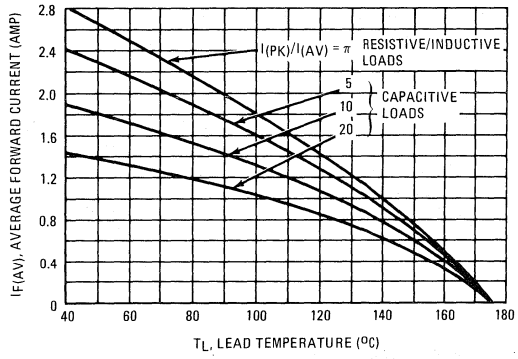


FIGURE 8 – PRINTED CIRCUIT BOARD MOUNTING – VARIOUS LOADS

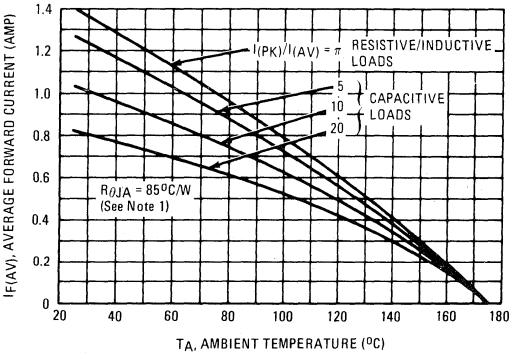
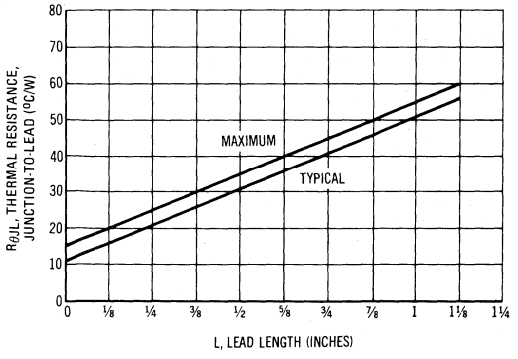


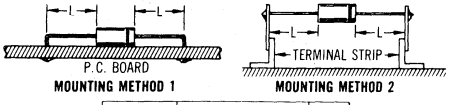
FIGURE 9 – STEADY-STATE THERMAL RESISTANCE



NOTE 1

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR



MOUNTING METHOD 1 MOUNTING METHOD 2

MOUNTING METHOD	LEAD LENGTH, L (IN.)			$R_{\theta JA}$
	1/32	3/8	1	
1	—	75	85	°C/W
2	55	72	85	°C/W

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 10 – FORWARD RECOVERY TIME

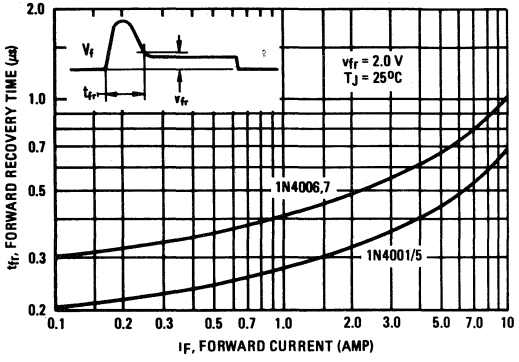


FIGURE 11 – REVERSE RECOVERY TIME

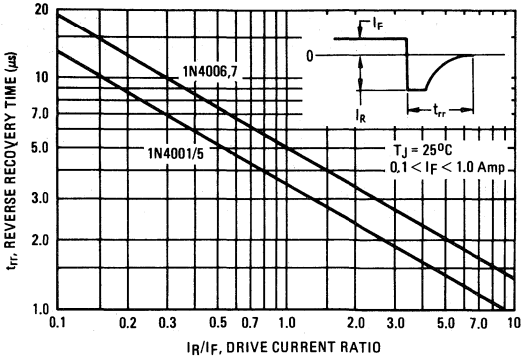


FIGURE 12 – JUNCTION CAPACITANCE

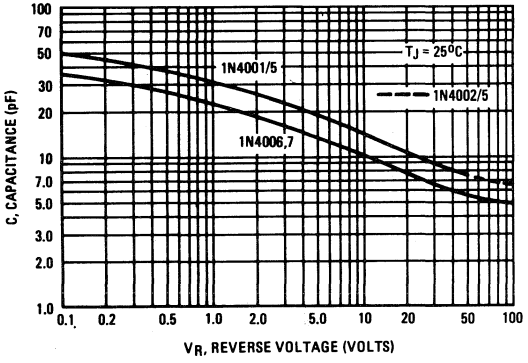


FIGURE 13 – RECTIFICATION WAVEFORM EFFICIENCY FOR SINE WAVE

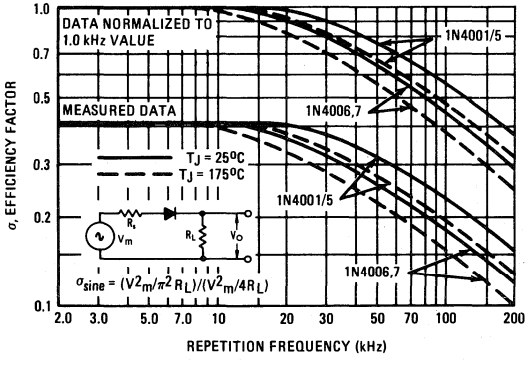
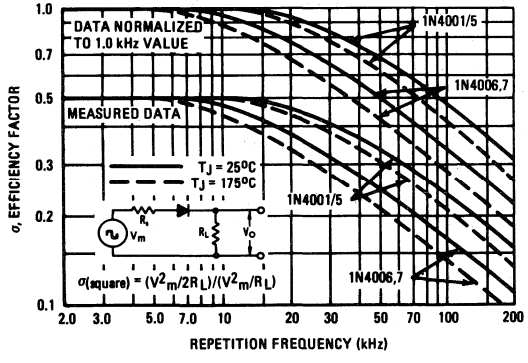


FIGURE 14 – RECTIFICATION WAVEFORM EFFICIENCY FOR SQUARE WAVE



RECTIFIER EFFICIENCY NOTE

The rectification efficiency factor σ shown in Figures 13 and 14 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \bullet 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \bullet 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes 40%; for a square wave input of amplitude V_m, the efficiency factor becomes 50%. (A full wave circuit has twice these efficiencies).

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 11) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current thereby reducing the value of the efficiency factor σ, as shown in Figures 13 and 14.

It should be emphasized that Figures 13 and 14 show waveform efficiency only; they do not account for diode losses. Data was obtained by measuring the ac component of V_O with a true rms voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for the Figures.

1N4933 thru 1N4937
MR2271

Designers▲ Data Sheet

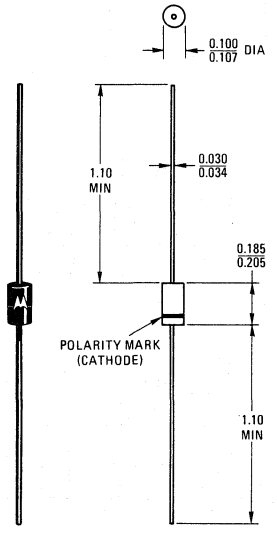
SUBMINIATURE SIZE, AXIAL LEAD MOUNTED FAST RECOVERY POWER RECTIFIERS

. . . designed for special applications such as dc power supplies, inverters, converters, ultrasonic systems, choppers, low RF interference and free wheeling diodes. A complete line of fast recovery rectifiers having typical recovery time of 100 nanoseconds providing high efficiency at frequencies to 250 kHz.

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristics boundaries — are given to facilitate "worst case" design.

FAST RECOVERY POWER RECTIFIERS
50-600 VOLTS
1 AMPERE



All JEDEC dimensions and notes apply

CASE 59
DO-41

***MAXIMUM RATINGS**

Rating	Symbol	1N4933	1N4934	1N4935	MR2271	1N4936	1N4937	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	300	400	600	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	75	150	250	350	450	650	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	210	280	420	Volts
Average Rectified Forward Current (Single phase, resistive load, T_A = 75°C)	I_O	1.0						Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	30						Amps
Operating Junction Temperature Range	T_J	-65 to +150						°C
Storage Temperature Range	T_{stg}	-65 to +175						°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient (Typical Printed Circuit Board Mounting)	$R_{\theta JC}$	65	°C/W

***ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Min	Typ	Max	Unit
*Instantaneous Forward Voltage (I_F = 3.14 Amp, T_J = 150°C)	V_F	–	1.0	1.2	Volts
Forward Voltage (I_F = 1.0 Amp, T_A = 25°C)	V_F	–	1.0	1.1	Volts
*Reverse Current (rated dc voltage) T_A = 25°C	I_R	–	1.0	5.0	μA
T_A = 100°C		–	50	100	

***REVERSE RECOVERY CHARACTERISTICS**

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Recovery Time (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	t_{rr}	–	100	200	ns
(I_{FM} = 15 Amp, di/dt = 10 A/μs) (Figure 22)		–	150	300	
Reverse Recovery Current (I_F = 1.0 Amp to V_R = 30 Vdc) (Figure 21)	$I_{RM(REC)}$	–	1.0	2.0	Amp

MECHANICAL CHARACTERISTICS

CASE: Void Free, Transfer Molded
FINISH: External leads are gold plated, leads are readily solderable
POLARITY: Cathode indicated by Polarity band.
WEIGHT: 0.4 Gram (Approximately)

*Indicates JEDEC Registered Data for 1N4933 Series
▲Trademark of Motorola Inc.

FIGURE 1 – FORWARD VOLTAGE

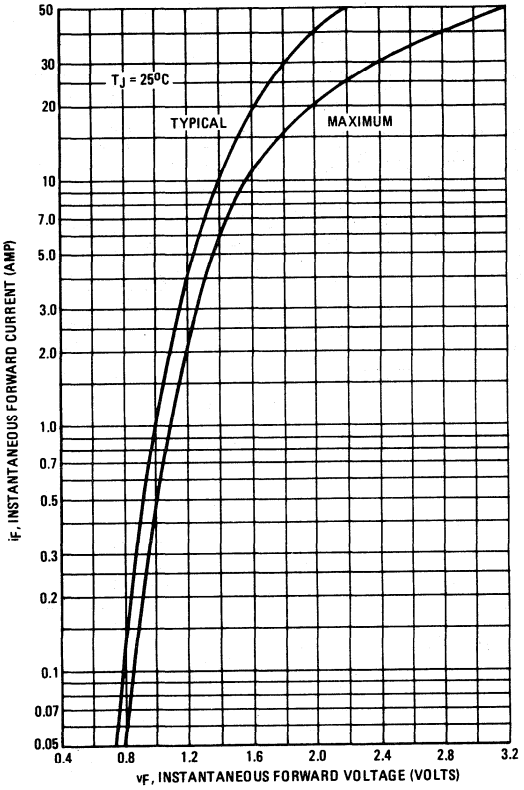


FIGURE 2 – MAXIMUM SURGE CAPABILITY

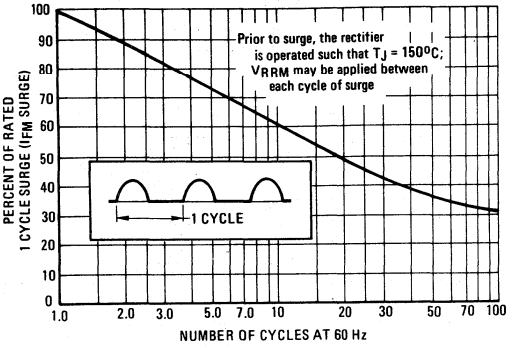
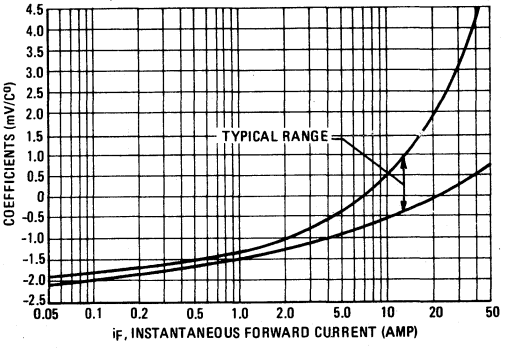
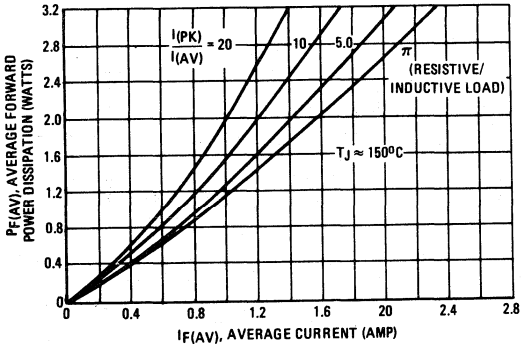


FIGURE 3 – FORWARD VOLTAGE TEMPERATURE COEFFICIENT



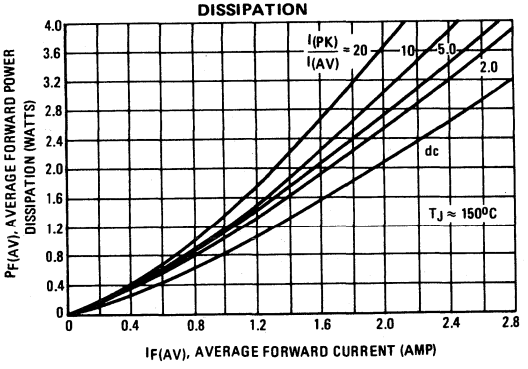
SINE WAVE INPUT

FIGURE 4 – FORWARD POWER DISSIPATION



SQUARE WAVE INPUT

FIGURE 5 – FORWARD POWER DISSIPATION



MAXIMUM CURRENT RATINGS

SINE WAVE INPUT

FIGURE 6 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

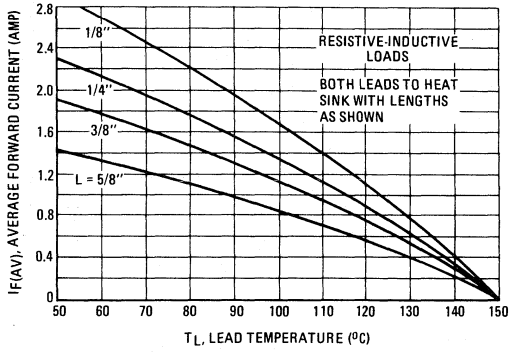


FIGURE 8 – 1/8" LEAD LENGTH, VARIOUS LOADS

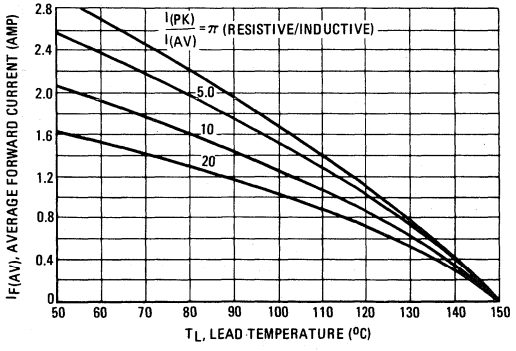
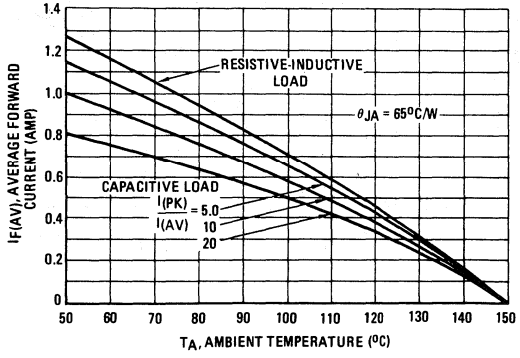


FIGURE 10 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS



SQUARE WAVE INPUT

FIGURE 7 – EFFECT OF LEAD LENGTHS, RESISTIVE LOAD

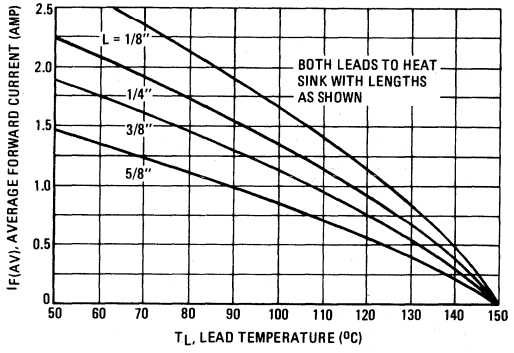


FIGURE 9 – 1/8" LEAD LENGTHS, VARIOUS LOADS

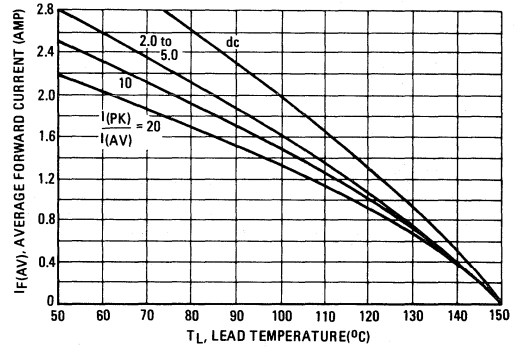


FIGURE 11 – PRINTED CIRCUIT BOARD MOUNTING, VARIOUS LOADS

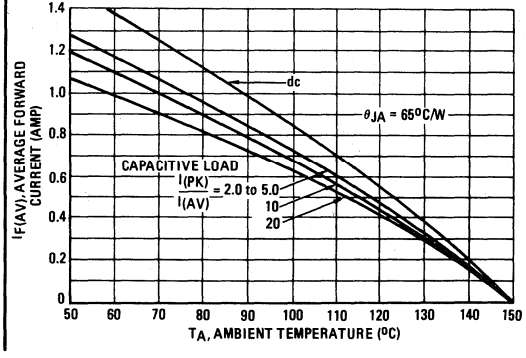


FIGURE 12 – THERMAL RESPONSE

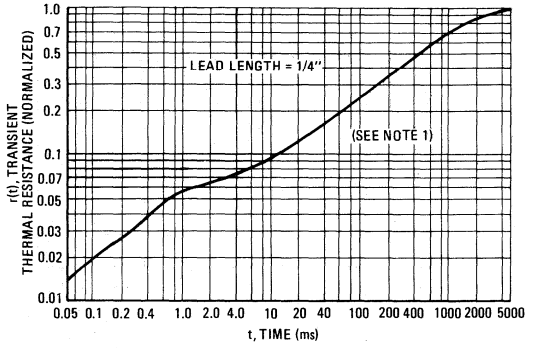
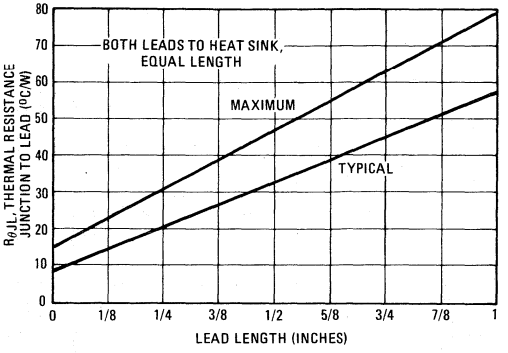
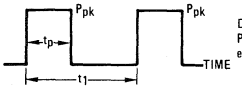


FIGURE 13 – THERMAL RESISTANCE



NOTE 1



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the case should be measured using a thermocouple placed on the case at the temperature reference point (see Note 3). The thermal mass connected to the case is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_C, the junction temperature may be determined by:

$$T_J = T_C + \Delta T_{JC}$$

where ΔT_{JC} is the increase in junction temperature above the case temperature. It may be determined by:

$$\Delta T_{JC} = P_{pk} \cdot R_{\theta JC} [D + (1 - D) \cdot r(t_1 + t_p) + r(t_p) - r(t_1)]$$

where

r(t) = normalized value of transient thermal resistance at time, t, from Figure 3, i.e.:

$r(t_1 + t_p)$ = normalized value of transient thermal resistance at time $t_1 + t_p$.

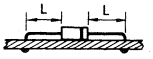
NOTE 2

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

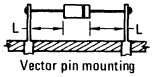
TYPICAL VALUES FOR θ_{JA} IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	65	72	82	92	°C/W
2	74	81	91	101	°C/W
3	40				°C/W

MOUNTING METHOD 1



MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 3

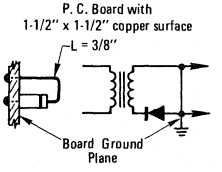
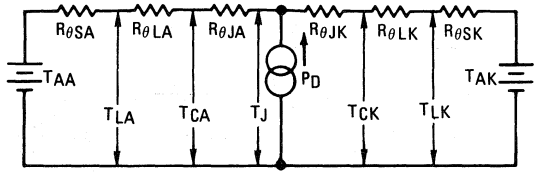


FIGURE 14 – THERMAL CIRCUIT MODEL
(For Heat Conduction Through The Leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:

$R_{\theta L}$ = 112°C/W/IN. Typically and 128°C/W/IN Maximum

$R_{\theta J}$ = 18°C/W Typically and 30°C/W Maximum

The maximum lead temperature may be calculated as follows:

$$T_L = 150^o - \Delta T_{JL}$$

ΔT_{JL} can be calculated as shown in NOTE 1 or it may be approximated as follows:

$\Delta T_{JL} \approx R_{\theta JL} \bullet P_F$; P_F may be formulated for sine-wave operation from Figure 3 or from Figure 4 for square-wave operation.

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 15 – FORWARD RECOVERY TIME

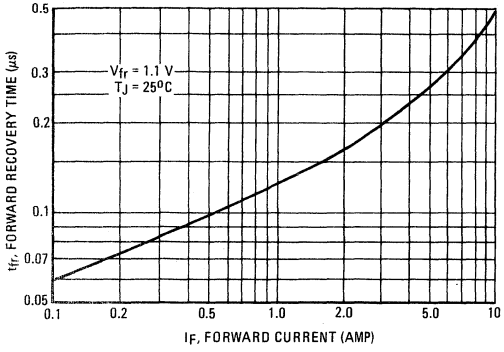
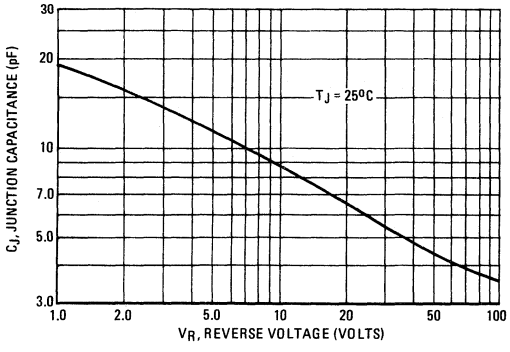


FIGURE 16 – JUNCTION CAPACITANCE



TYPICAL RECOVERED STORED CHARGED DATA

FIGURE 17 – T_J = 25°C

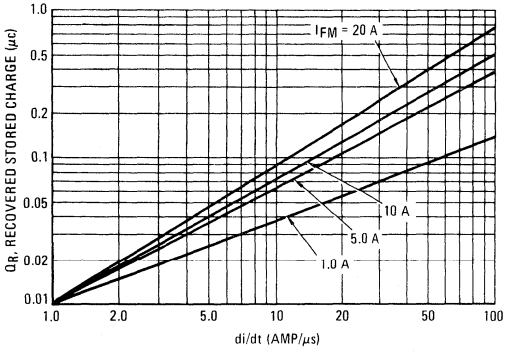


FIGURE 18 – T_J = 75°C

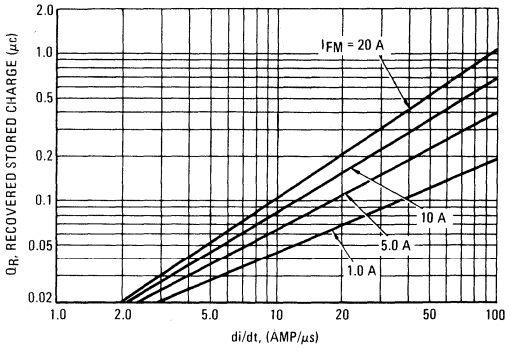


FIGURE 19 – T_J = 100°C

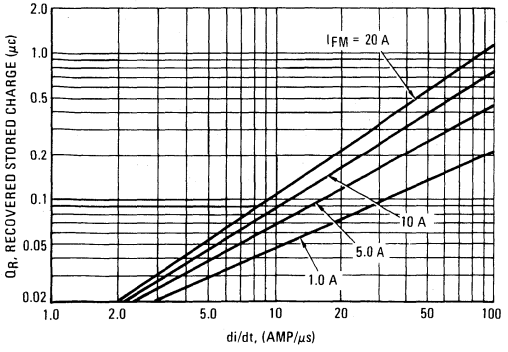
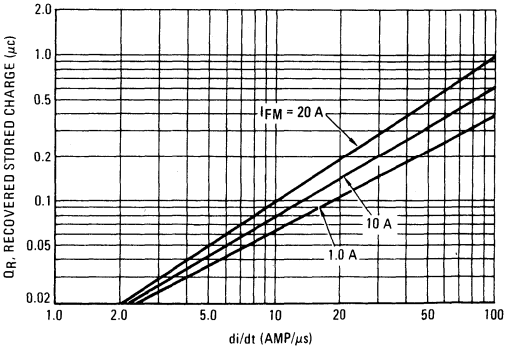


FIGURE 20 – T_J = 150°C



RECOVERY TIME

FIGURE 21 – REVERSE RECOVERY CIRCUIT

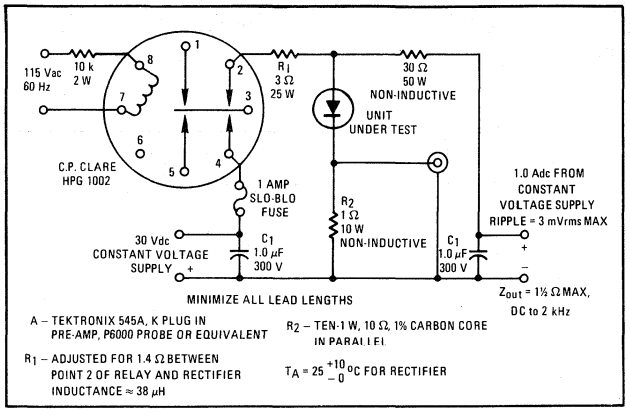
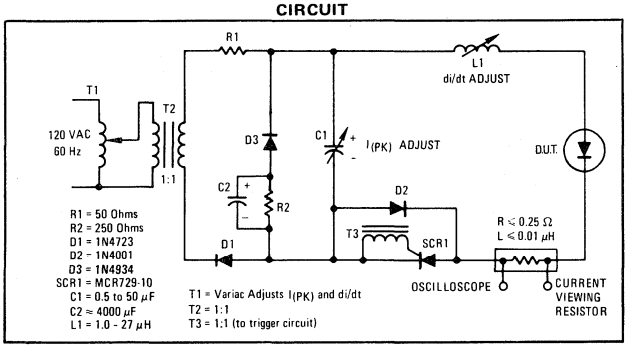


FIGURE 22 – JEDEC REVERSE RECOVERY CIRCUIT



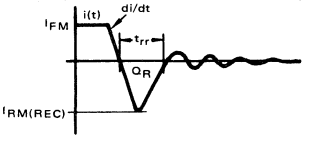
NOTE 3

Reverse recovery time is the period which elapses from the time that the current, thru a previously forward biased rectifier diode, passes thru zero going negatively until the reverse current recovers to a point which is less than 10% peak reverse current.

Reverse recovery time is a direct function of the forward current prior to the application of reverse voltage.

For any given rectifier, recovery time is very circuit dependent. Typical and maximum recovery time of all Motorola fast recovery power rectifiers are rated under a fixed set of conditions using I_F = 1.0 A, V_R = 30 V. In order to cover all circuit conditions, curves are given for typical recovered stored charge versus commutation di/dt for various levels of forward current and for junction temperatures of 25°C, 75°C, 100°C, and 150°C.

To use these curves, it is necessary to know the forward current level just before commutation, the circuit commutation di/dt, and the operating junction temperature. The reverse recovery test current waveform for all Motorola fast recovery rectifiers is shown.



From stored charge curves versus di/dt, recovery time (t_{rr}) and peak reverse recovery current ($I_{RM(REC)}$) can be closely approximated using the following formulas:

$$t_{rr} = 1.41 \times \left[\frac{Q_R}{di/dt}\right]^{1/2}$$

$$I_{RM(REC)} = 1.41 \times \left[Q_R \times di/dt\right]^{1/2}$$

FIGURE 23 – TYPICAL REVERSE LEAKAGE

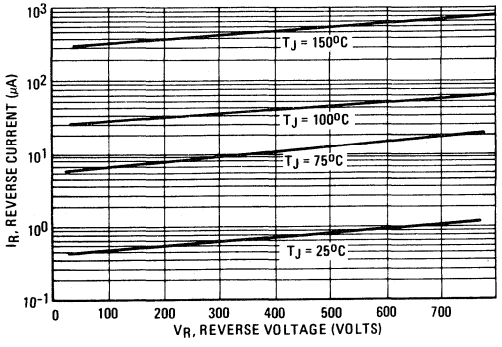
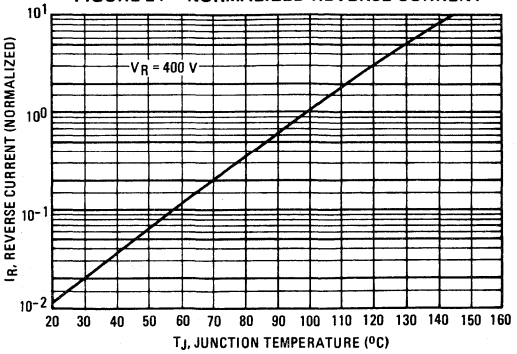


FIGURE 24 – NORMALIZED REVERSE CURRENT



1N5333 • 1N5388

5.0 WATT SURMETIC 40 SILICON ZENER DIODES (SILICON OXIDE PASSIVATED)

. . . a complete new series of 5.0 Watt Zener Diodes with tight limits and better operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Up to 180 Watt Surge Rating @ 8.3 ms
- Maximum Limits Guaranteed on Seven Electrical Parameters

(5M3.3ZS10 thru 5M200ZS10
1N5333A thru 1N5388A
5M3.3ZS5 thru 5M200ZS5
1N5333B thru 1N5388B)

5.0 WATT
ZENER REGULATOR DIODES

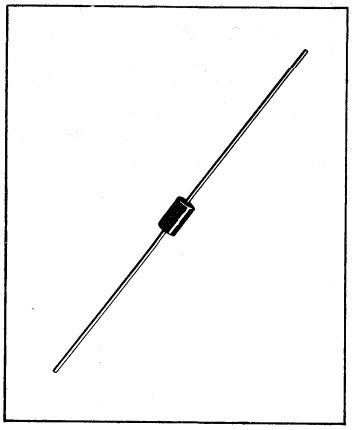
3.3 – 200 VOLTS

MAXIMUM RATINGS

Junction and Storage Temperature: −65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 5.0 W @ T_L = 75°C, Lead Length = 3/8"
(Derate 40 mW/°C above 75°C)



MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

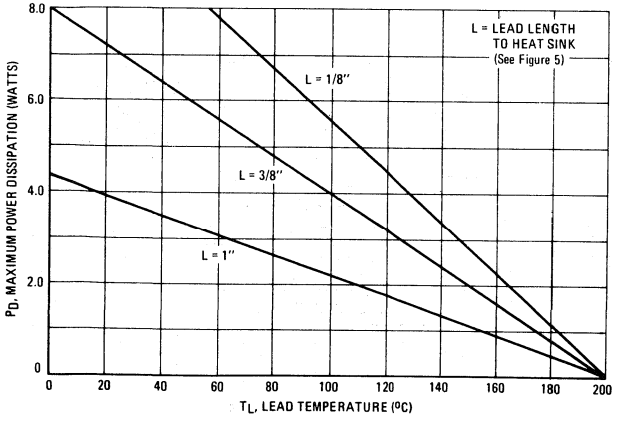
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable

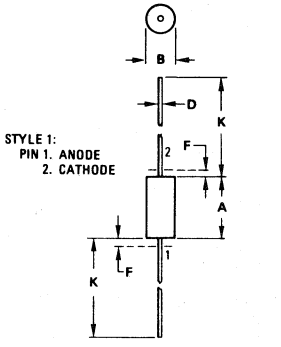
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any

WEIGHT: 0.7 gram (approx)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	3.30	3.68	0.130	0.145
D	0.94	1.09	0.037	0.043
F	–	1.27	–	0.050
K	25.40	31.75	1.000	1.250

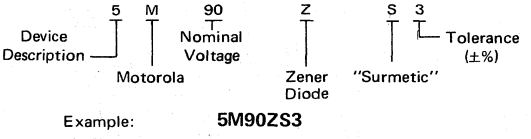
CASE 17

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) V_F = 1.2 Max @ I_F = 1.0 A for all types

JEDEC Type No. (Note 1 & 2)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 3)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current			Applies to all Suffix	A & B Suffix Only	Maximum Regulator Current I_{ZM} mA
			Z_{ZT} @ I_{ZT} Ohms (Note 3)	Z_{ZK} @ I_{ZK} = 1.0 mA Ohms (Note 3)	I_R μA	@ V_R Volts		Max Surge Current i_r, Amps	Max Voltage Regulation $\triangle V_Z$, Volts	
						Non & A Suffix	B-Suffix	(Note 4)	(Note 5)	(Note 6)
1N5333	3.3	380	3.0	400	300	1.0	1.0	20.0	0.85	1440
1N5334	3.6	350	2.5	500	150	1.0	1.0	18.7	0.80	1320
1N5335	3.9	320	2.0	500	50	1.0	1.0	17.6	0.54	1220
1N5336	4.3	290	2.0	500	10	1.0	1.0	16.4	0.49	1100
1N5337	4.7	260	2.0	450	5.0	1.0	1.0	15.3	0.44	1010
1N5338	5.1	240	1.5	400	1.0	1.0	1.0	14.4	0.39	930
1N5339	5.6	220	1.0	400	1.0	2.0	2.0	13.4	0.25	865
1N5340	6.0	200	1.0	300	1.0	3.0	3.0	12.7	0.19	790
1N5341	6.2	200	1.0	200	1.0	3.0	3.0	12.4	0.10	765
1N5342	6.8	175	1.0	200	10	4.9	5.2	11.5	0.15	700
1N5343	7.5	175	1.5	200	10	5.4	5.7	10.7	0.15	630
1N5344	8.2	150	1.5	200	10	5.9	6.2	10.0	0.20	580
1N5345	8.7	150	2.0	200	10	6.3	6.6	9.5	0.20	545
1N5346	9.1	150	2.0	150	7.5	6.6	6.9	9.2	0.22	520
1N5347	10	125	2.0	125	5.0	7.2	7.6	8.6	0.22	475
1N5348	11	125	2.5	125	5.0	8.0	8.4	8.0	0.25	430
1N5349	12	100	2.5	125	2.0	8.6	9.1	7.5	0.25	395
1N5350	13	100	2.5	100	1.0	9.4	9.9	7.0	0.25	365
1N5351	14	100	2.5	75	1.0	10.1	10.6	6.7	0.25	340
1N5352	15	75	2.5	75	1.0	10.8	11.5	6.3	0.25	315
1N5353	16	75	2.5	75	1.0	11.5	12.2	6.0	0.30	295
1N5354	17	70	2.5	75	0.5	12.2	12.9	5.8	0.35	280
1N5355	18	65	2.5	75	0.5	13.0	13.7	5.5	0.40	264
1N5356	19	65	3.0	75	0.5	13.7	14.4	5.3	0.40	250
1N5357	20	65	3.0	75	0.5	14.4	15.2	5.1	0.40	237
1N5358	22	50	3.5	75	0.5	15.8	16.7	4.7	0.45	216
1N5359	24	50	3.5	100	0.5	17.3	18.2	4.4	0.55	198
1N5360	25	50	4.0	110	0.5	18.0	19.0	4.3	0.55	190
1N5361	27	50	5.0	120	0.5	19.4	20.6	4.1	0.60	176
1N5362	28	50	6.0	130	0.5	20.1	21.2	3.9	0.60	170
1N5363	30	40	8.0	140	0.5	21.6	22.8	3.7	0.60	158
1N5364	33	40	10	150	0.5	23.8	25.1	3.5	0.60	144
1N5365	36	30	11	160	0.5	25.9	27.4	3.3	0.65	132
1N5366	39	30	14	170	0.5	28.1	29.7	3.1	0.65	122
1N5367	43	30	20	190	0.5	31.0	32.7	2.8	0.70	110
1N5368	47	25	25	210	0.5	33.8	35.8	2.7	0.80	100
1N5369	51	25	27	230	0.5	36.7	38.8	2.5	0.90	93.0
1N5370	56	20	35	280	0.5	40.3	42.6	2.3	1.00	86.0
1N5371	60	20	40	350	0.5	43.0	45.5	2.2	1.20	79.0
1N5372	62	20	42	400	0.5	44.6	47.1	2.1	1.35	76.0
1N5373	68	20	44	500	0.5	49.0	51.7	2.0	1.50	70.0
1N5374	75	20	45	620	0.5	54.0	56.0	1.9	1.60	63.0
1N5375	82	15	65	720	0.5	59.0	62.2	1.8	1.80	58.0
1N5376	87	15	75	760	0.5	63.0	66.0	1.7	2.00	54.5
1N5377	91	15	75	760	0.5	65.5	69.2	1.6	2.20	52.5
1N5378	100	12	90	800	0.5	72.0	76.0	1.5	2.50	47.5
1N5379	110	12	125	1000	0.5	79.2	83.6	1.4	2.50	43.0
1N5380	120	10	170	1150	0.5	86.4	91.2	1.3	2.50	39.5
1N5381	130	10	190	1250	0.5	93.6	98.8	1.2	2.50	36.6
1N5382	140	8.0	230	1500	0.5	101	106	1.2	2.50	34.0
1N5383	150	8.0	330	1500	0.5	108	114	1.1	3.00	31.6
1N5384	160	8.0	350	1650	0.5	115	122	1.1	3.00	29.4
1N5385	170	8.0	380	1750	0.5	122	129	1.0	3.00	28.0
1N5386	180	5.0	430	1750	0.5	130	137	1.0	4.00	26.4
1N5387	190	5.0	450	1850	0.5	137	144	0.9	5.00	25.0
1N5388	200	5.0	480	1850	0.5	144	152	0.9	5.00	23.6

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

TOLERANCE DESIGNATION – The JEDEC type numbers shown indicate a tolerance of ±20% with guaranteed limits on only V_Z, I_R, i_r, and V_F as shown in the electrical characteristics table. Units with guaranteed limits on all seven parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.



Example: **5M90ZS3**

NOTE 2 – SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES: To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances (±3%, ±2%, ±1%), the Motorola type number should be used.

(B) MATCHED SETS: (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A) for specifying units

with a special voltage and/or tolerance except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and, in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.

5	M	5 1	Z	S	5	B	1
Device Description	Motorola	51 Volts (each device)	Zener Diodes	"Surmetic"	Tolerance per device (±5%) (omit for ±20% units)	Code*	Overall Tolerance of set (±1%)

*Code:
B – Two devices in series
C – Three devices in series
D – Four devices in series
(A-Not used)

Example: **5M51ZS5B1**

(C) ZENER CLIPPERS: (Standard Tolerance ±10% and ±5%).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature:

5	M	20,	Z	Z	10
Device Description	Motorola	Nominal Voltage	Zener Diodes	Clipper	Tolerance for each of the two Zener voltages (not a matching requirement)

Example: **5M20ZZ10**

NOTE 3 – ZENER VOLTAGE (V_Z) AND IMPEDANCE (Z_{ZT} & Z_{ZK})

Test conditions for Zener voltage and impedance are as follows: I_Z is applied 40 ± 10 ms prior to reading. Mounting contacts are located 3/8" to 1/2" from the inside edge of mounting clips to the body of the diode. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$).

NOTE 4 – SURGE CURRENT (i_r)

Surge current is specified as the maximum allowable peak, non-recurrent square-wave current with a pulse width, PW, of 8.3 ms. The data given in Figure 6 may be used to find the maximum surge current for a square wave of any pulse width between 1.0 ms and 1000 ms by plotting the applicable points on logarithmic paper. Examples of this, using the 3.3 V and 200 V zeners, are shown in Figure 7. Mounting contact located as specified in Note 3. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$).

NOTE 5 – VOLTAGE REGULATION (ΔV_Z)

Test conditions for voltage regulation are as follows: V_Z measurements are made at 10% and then at 50% of the I_Z max value listed in the electrical characteristics table. The test currents are the same for the 5% and 10% tolerance devices. The test current time duration for each V_Z measurement is 40 ± 10 ms. ($T_A = 25^oC \, ^{+8}_{-2}{}^oC$). Mounting contact located as specified in Note 3.

NOTE 6 – MAXIMUM REGULATOR CURRENT (I_{ZM})

The maximum current shown is based on the maximum voltage of a 5% type unit, therefore, it applies only to the B-suffix device. The actual I_{ZM} for any device may not exceed the value of 5.0 watts divided by the actual V_Z of the device. $T_L = 75^oC$ at 3/8" maximum from the device body.

TEMPERATURE COEFFICIENTS

FIGURE 2 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 3.0 TO 10 VOLTS

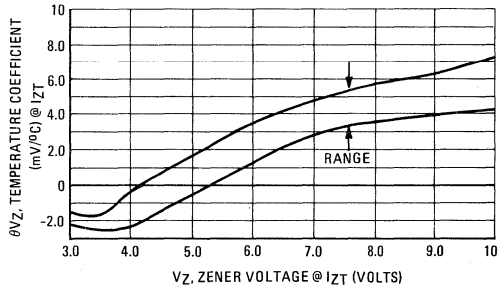


FIGURE 3 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 220 VOLTS

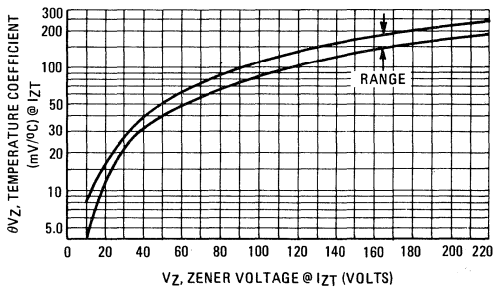


FIGURE 4 – TYPICAL THERMAL RESPONSE

L, LEAD LENGTH = 3/8 INCH

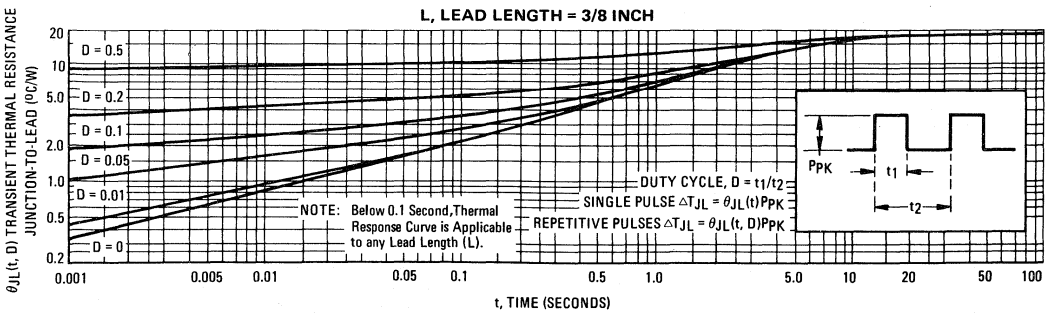


FIGURE 5 – TYPICAL THERMAL RESISTANCE

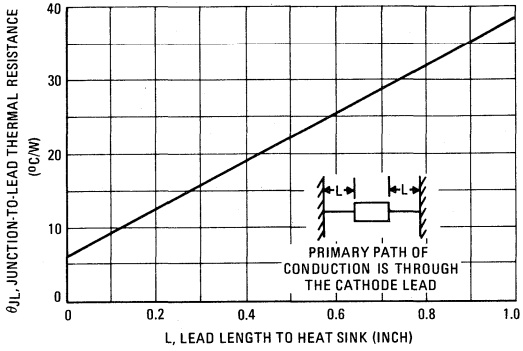


FIGURE 6 – MAXIMUM NON-REPETITIVE SURGE CURRENT versus NOMINAL ZENER VOLTAGE
(See Note 4)

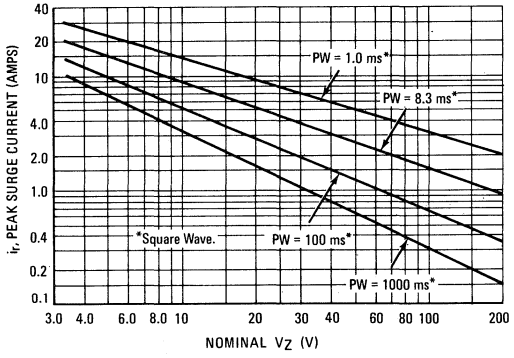
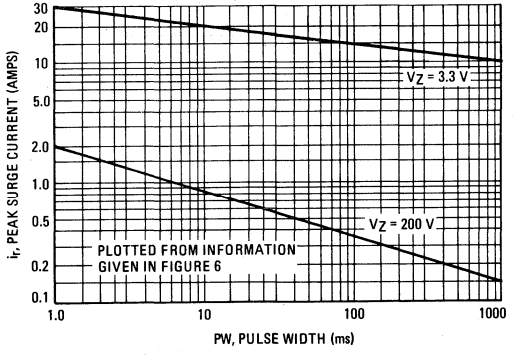


FIGURE 7 – PEAK SURGE CURRENT versus PULSE WIDTH
(See Note 4)



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 4 for a train of power pulses or from Figure 5 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of $T_J(\Delta T_J)$ may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 2 and 3.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 4 should not be used to compute surge capability. Surge limitations are given in Figure 6. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 6 be exceeded.

1N5817
1N5818

Designers Data Sheet

HOT CARRIER POWER RECTIFIERS

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

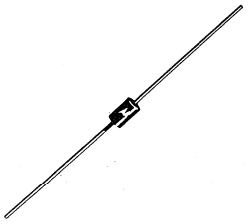
- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

SCHOTTKY BARRIER RECTIFIERS

1 AMPERE
20, 30 VOLTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



*MAXIMUM RATINGS

Rating	Symbol	1N5817	1N5818	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	Volts
Average Rectified Forward Current (2) $V_{R(equiv)} \leq 0.2\,V_{R(dc)}$, $T_L = 90^oC$ ($R_{\theta JA} = 80^oC/W$, P.C. Board Mounting, See Note 2)	I_O	1.0		Amp
Ambient Temperature Rated $V_{R(dc)}$, $P_{F(AV)} = 0$ $R_{\theta JA} = 80^oC/W$	T_A	85	80	^oC
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase 60 Hz, $T_L = 70^oC$	I_{FSM}	100 (for 1 cycle)		Amp
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	-65 to +125		^oC
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150		^oC

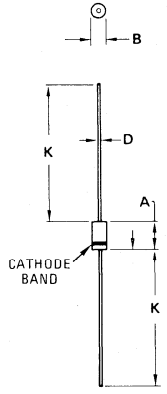
*THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_L = 25^oC$ unless otherwise noted.) (2)

Characteristic	Symbol	1N5817	1N5818	Unit
Maximum Instantaneous Forward Voltage (1)	v_F			Volts
(i_F = 0.1 Amp)		0.320	0.330	
(i_F = 1.0 Amp)		0.450	0.550	
(i_F = 3.1 Amp)		0.750	0.875	
Maximum Instantaneous Reverse Current @ rated dc Voltage (1)	I_R			mA
$T_L = 25^oC$		1.0	1.0	
$T_L = 100^oC$		10	10	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from Case.
*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.20	0.185	0.205
B	2.54	2.71	0.100	0.107
D	0.76	0.86	0.030	0.034
K	27.94	–	1.100	–

CASE 59
DO-41

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded

FINISH: All external surfaces corrosion-resistant and the terminal leads are readily solderable.

POLARITY: Cathode indicated by polarity band

MOUNTING POSITIONS: Any

SOLDERING: 220°C 1/16" from case for 10 s.

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1 and 2 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figure 1 and 2 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1 and 2 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5818 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 1.0 A ($I_{F(AV)}$ = 0.5A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 V(rms), $R_{\theta JA}$ = 80°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I ∴ $V_{R(equiv)}$ = (1.41)(10)(0.65) = 9.2 V

Step 2: Find T_R from Figure 2. Read T_R = 109°C @ V_R = 9.2 V & $R_{\theta JA}$ = 80°C/W.

Step 3: Find $P_{F(AV)}$ from Figure 3. **Read $P_{F(AV)}$ = 0.5 W @ $\frac{I_{(FM)}}{I_{(AV)}}$ = 10 & $I_{F(AV)}$ = 0.5 A

Step 4: Find $T_{A(max)}$ from equation (3). $T_{A(max)}$ = 109 - (80) (0.5) = 69°C

**Values given are for the 1N5818. Power is slightly lower for the 1N5817 because of its lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped *†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5817

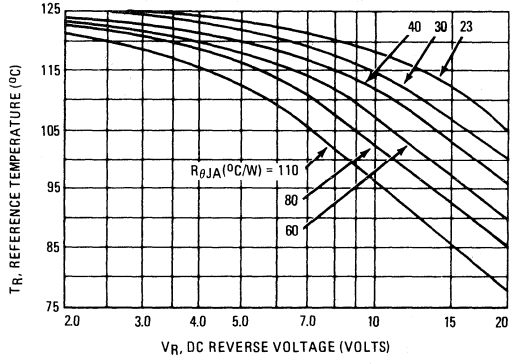


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5818

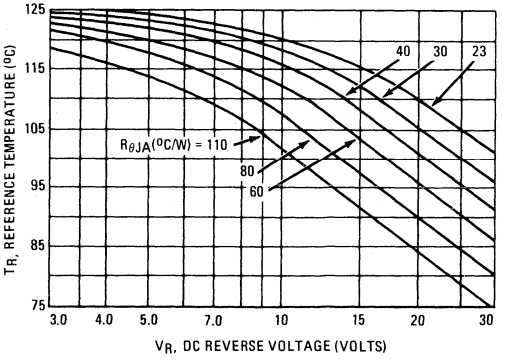
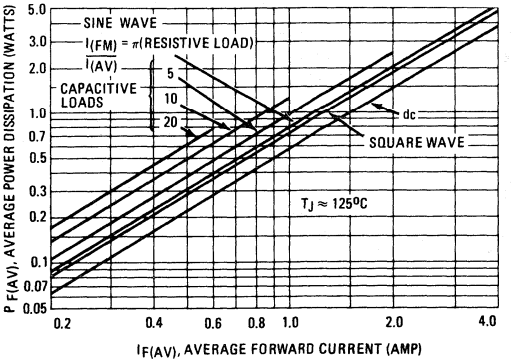


FIGURE 3 – FORWARD POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 4 – THERMAL RESPONSE

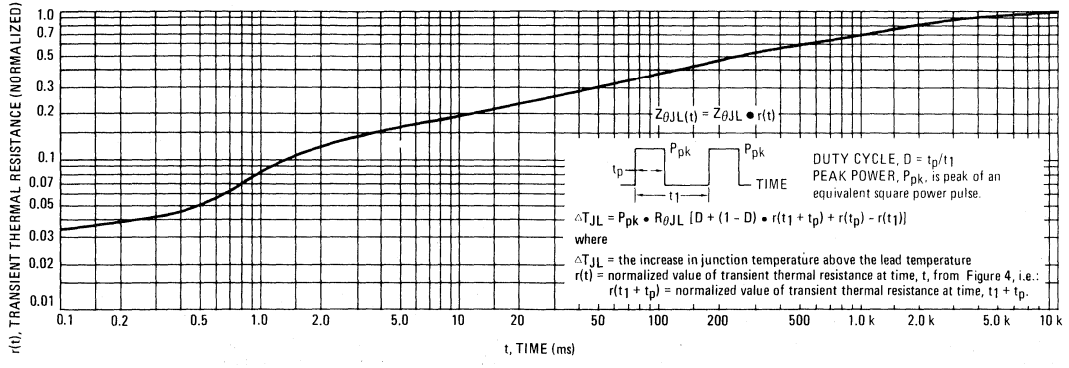
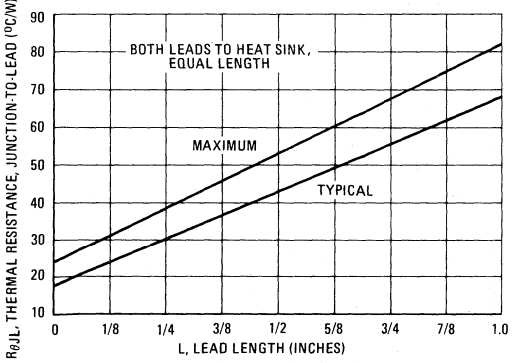


FIGURE 5 – STEADY – STATE THERMAL RESISTANCE



NOTE 2 – MOUNTING DATA

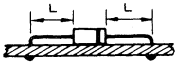
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

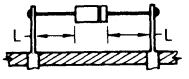
MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	3/8	1/2	3/4	$R_{\theta JA}$
1	52	65	72	85	°C/W
2	67	80	87	100	°C/W
3	50				°C/W

MOUNTING METHOD 1

P.C. Board with 1-1/2" x 1-1/2" copper surface.



MOUNTING METHOD 2



Vector pin mounting

MOUNTING METHOD 2

P.C. Board with 1-1/2" x 1-1/2" copper surface.

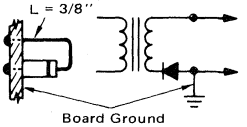
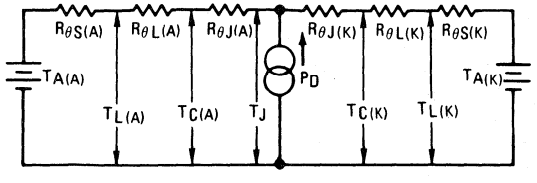


FIGURE 6 – THERMAL CIRCUIT MODEL
(For Heat Conduction Through The Leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides respectively.)

Values for thermal resistance components are:
$R_{\theta L}$ = 100°C/W/IN. Typically and 120°C/W/IN Maximum
$R_{\theta J}$ = 36°C/W Typically and 46°C/W Maximum

FIGURE 7 – TYPICAL FORWARD VOLTAGE

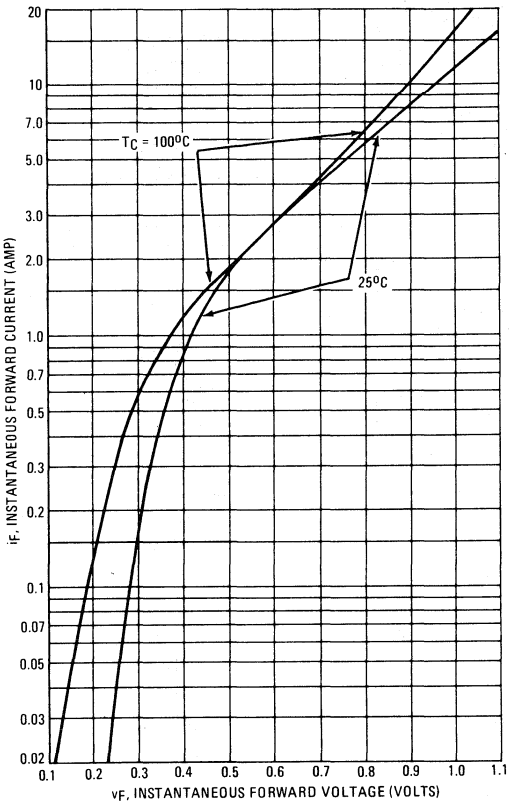


FIGURE 8 – MAXIMUM NON-REPETITIVE SURGE CURRENT

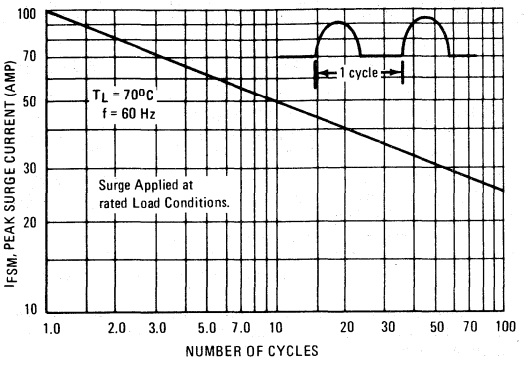


FIGURE 9 – TYPICAL REVERSE CURRENT

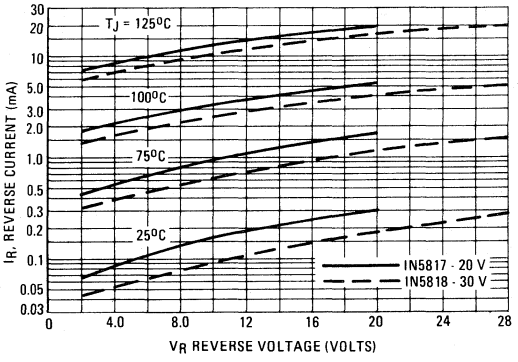
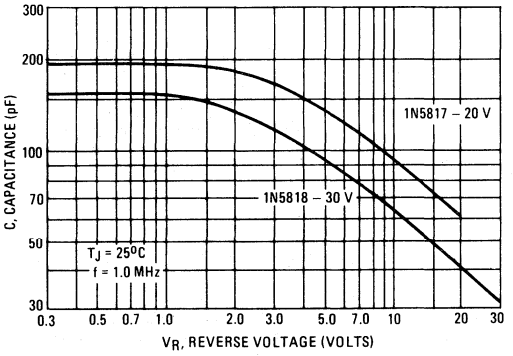


FIGURE 10 – CAPACITANCE



NOTE 3 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 10.)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

1N5820
1N5821

Designers Data Sheet

HOT CARRIER POWER RECTIFIERS

. . . employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high-frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency
- High Surge Capacity

Designer's Data for "Worst Case" Conditions

The Designers▲ Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

SCHOTTKY BARRIER RECTIFIERS

3.0 AMPERE
20, 30 VOLTS

*MAXIMUM RATINGS

Rating	Symbol	1N5820	1N5821	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	Volts
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	Volts
Average Rectified Forward Current (2) $V_{R(equiv)} \leq 0.2\, V_R$ (dc), $T_L = 95^oC$ ($R_{\theta JA} = 28^oC/W$, P.C. Board Mounting, See Note 2)	I_O	3.0		Amp
Ambient Temperature Rated V_R (dc), $P_{F(AV)} = 0$ $R_{\theta JA} = 28^oC/W$	T_A	90	85	°C
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, halfwave, single phase 60 Hz, $T_L = 75^oC$)	I_{FSM}	250 (for 1 cycle)		Amp
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	–65 to +125		°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150		°C

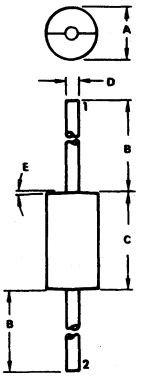
*THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C/W

*ELECTRICAL CHARACTERISTICS ($T_L = 25^oC$ unless otherwise noted.) (2)

Characteristic	Symbol	1N5820	1N5821	Unit
Maximum Instantaneous Forward Voltage (1) (i_F = 1.0 Amp) (i_F = 3.0 Amp) (i_F = 9.4 Amp)	v_F	 0.370 0.475 0.850	 0.380 0.500 0.900	Volts
Maximum Instantaneous Reverse Current @ rated dc Voltage (1) $T_L = 25^oC$ $T_L = 100^oC$	I_R	 2.0 20	 2.0 20	mA

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from Case.
*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



	INCHES		MILLIMETERS	
A	0.190	0.210	4.83	5.33
B	1.062	1.072	26.97	27.23
C	0.370	0.380	9.40	9.65
D	0.048	0.052	1.22	1.32
E	2°		2°	

CASE 267

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded

FINISH: All external surfaces corrosion-resistant and the terminal leads are readily solderable.

POLARITY: Cathode indicated by polarity band

MOUNTING POSITIONS: Any

SOLDERING: 220°C 1/16" from case for 10 s.

NOTE 1: DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature

$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation

$P_{R(AV)}$ = Average reverse power dissipation

$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1 and 2 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1 and 2 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1 and 2 is based upon dc conditions. For use in common rectifier circuits, Table I indicates suggested factors for an equivalent dc voltage to use for conservative design; i.e.:

$$V_{R(equiv)} = V_{(FM)} \times F \quad (4)$$

The Factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

Example: Find $T_{A(max)}$ for 1N5821 operated in a 12-Volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 2.0 A ($I_{F(AV)}$ = 1.0 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 40°C/W.

Step 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table I
$V_{R(equiv)} = (1.41)(10)(0.65) = 9.2$ V

Step 2: Find T_R from Figure 2. Read T_R = 108°C @ V_R = 9.2 V & $R_{\theta JA}$ = 40°C/W.

Step 3: Find $P_{F(AV)}$ from Figure 3.**Read $P_{F(AV)}$ = 0.85 W @ $\frac{I_{(FM)}}{I_{(AV)}}$ = 10 & $I_{F(AV)}$ = 1.0 A

Step 4: Find $T_{A(max)}$ from equation (3).
$T_{A(max)}$ = 108 - (0.85) (40) = 74°C

**Values given are for the 1N5821. Power is slightly lower for the 1N5820 because of its lower forward voltage.

TABLE I – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped *†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2\ V_{in(PK)}$ †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE – 1N5820

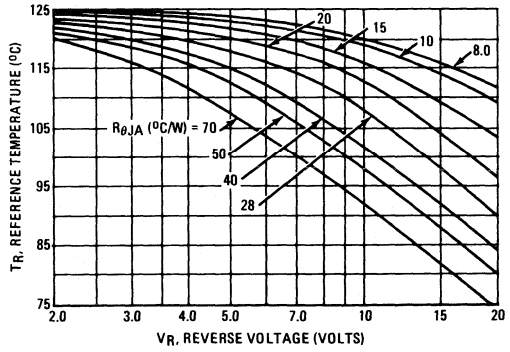


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE – 1N5821

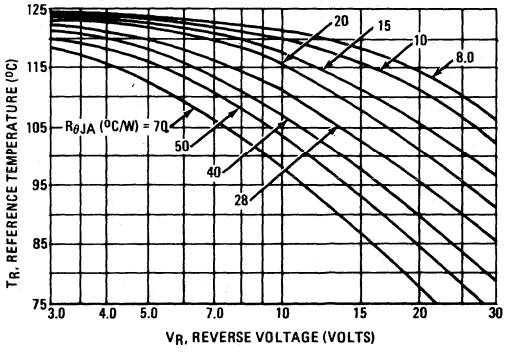
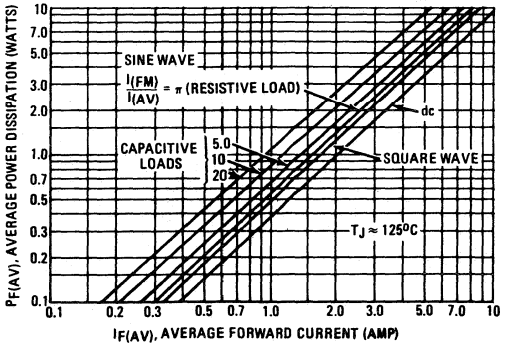


FIGURE 3 – FORWARD POWER DISSIPATION



THERMAL CHARACTERISTICS

FIGURE 4 – THERMAL RESPONSE

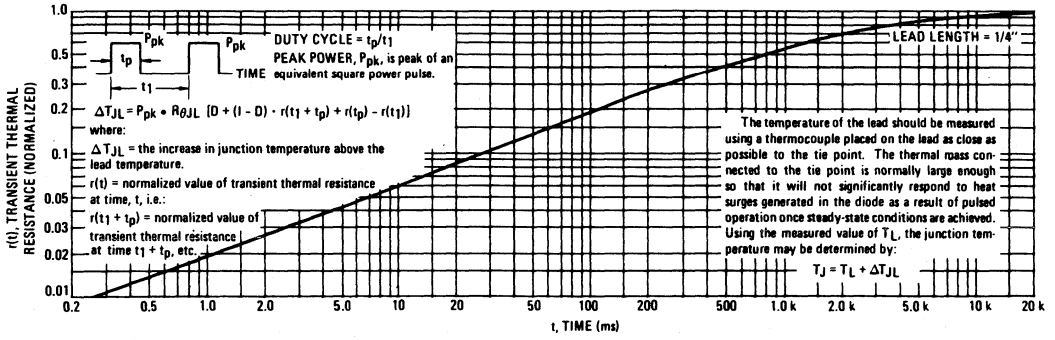
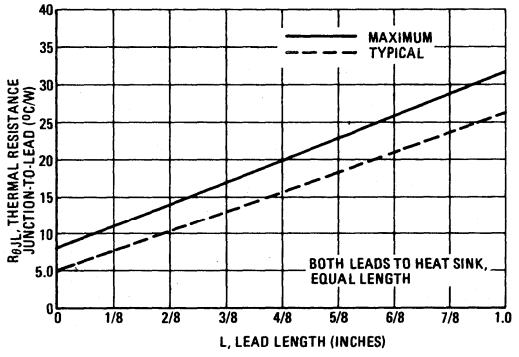


FIGURE 5 – STEADY – STATE THERMAL RESISTANCE



NOTE 2 – MOUNTING DATA

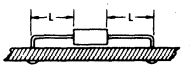
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

MOUNTING METHOD	LEAD LENGTH, L (IN) 1/8	1/4	1/2	3/4	$R_{\theta JA}$
1	50	51	53	55	°C/W
2	58	59	61	63	°C/W
3	28				°C/W

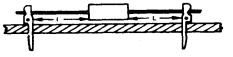
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with 2-1/2" x 2-1/2" Copper Surface

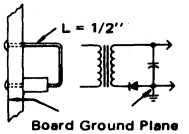
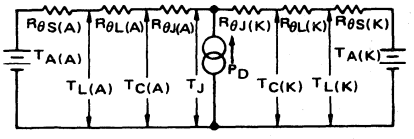


FIGURE 6 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_L = Lead Temperature
T_C = Case Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation

(Subscripts (A) and (K) refer to anode and cathode sides respectively.) Values for thermal resistance components are:

$R_{\theta L}$ = 42°C/W/IN. Typically and 48°C/W/IN. Maximum.
$R_{\theta J}$ = 10°C/W Typically and 16°C/W Maximum.

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

Where: $\Delta T_{JL} \approx R_{\theta JL} \bullet P_D$

FIGURE 7 – TYPICAL FORWARD VOLTAGE

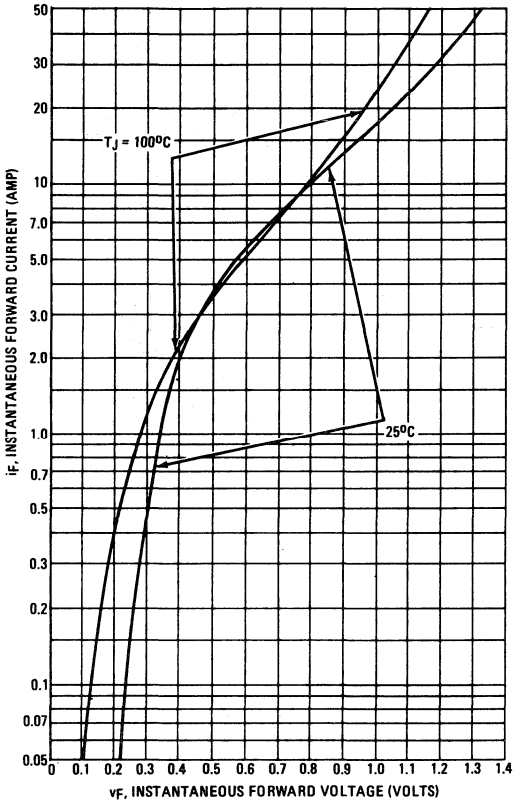


FIGURE 8 – MAXIMUM NON-REPETITIVE SURGE CURRENT

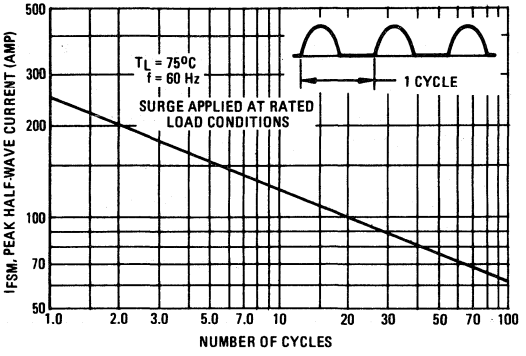


FIGURE 9 – TYPICAL REVERSE CURRENT

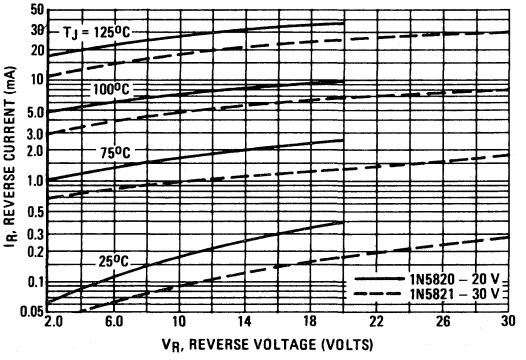
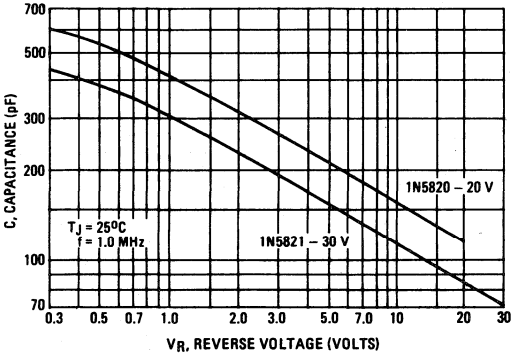


FIGURE 10 – CAPACITANCE



NOTE 3 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 10.)

3N246 thru 3N252
(MDA100A Series)

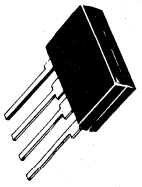
MINIATURE INTEGRAL DIODE ASSEMBLIES

. . . with silicon rectifier chips interconnected and encapsulated into voidless rectifier bridge circuits.

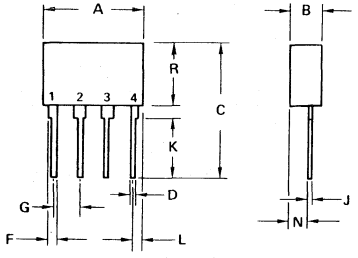
- High Resistance to Shock and Vibration
- High Dielectric Strength
- Built-In Printed Circuit Board Stand-Offs

SINGLE-PHASE
FULL-WAVE BRIDGE

1.0 AMPERE
50-1000 VOLTS



MAXIMUM RATINGS Rating (Per Diode)	Symbol	3N246 MDA100A	3N247 MDA101A	3N248 MDA102A	3N249 MDA104A	3N250 MDA106A	3N251 MDA108A	3N252 MDA110A	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	 Vdc Vdc	 32 50	 64 100	 127 200	 255 400	 382 600	 510 800	 640 1000	 Volts Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase bridge operation, resistive load, 60 Hz, T_A = 75°C)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (Preceded and followed by rated current and voltage, T_A = 75°C)	I_{FSM}	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150							°C



STYLE 1:
TERM 1. POS
2. AC
3. AC
4. NEG

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	4.57	5.08	0.180	0.200
C	–	20.57	–	0.810
D	0.76	1.02	0.030	0.040
F	1.02	1.27	0.040	0.050
G	3.68	3.94	0.145	0.155
J	0.56	0.71	0.022	0.028
K	–	9.02	–	0.355
L	1.78	2.03	0.070	0.080
N	2.54	2.79	0.100	0.110
R	9.40	10.03	0.370	0.395

CASE 312-02

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) (i_F = 1.57 Amp, T_J = 25°C)	v_F	1.15	1.3	Volts
Reverse Current (Per Diode) (Rated V_R, T_A = 25°C) (Rated V_R, T_A = 100°C)	I_R	– –	10 100	μA

MECHANICAL CHARACTERISTICS

CASE: Transfer Molded Plastic
POLARITY: Terminal-designation on case
(+) for DC output
(–) for DC output
(AC) for AC input

MOUNTING POSITION: Any
WEIGHT: 1.8 grams (approx)
TERMINALS: Readily solderable connections, corrosion resistant.

MAXIMUM RATINGS, BRIDGE OPERATION

FIGURE 1 – CURRENT DERATING

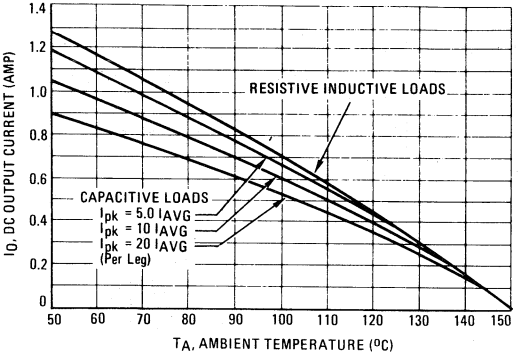


FIGURE 2 – POWER DISSIPATION

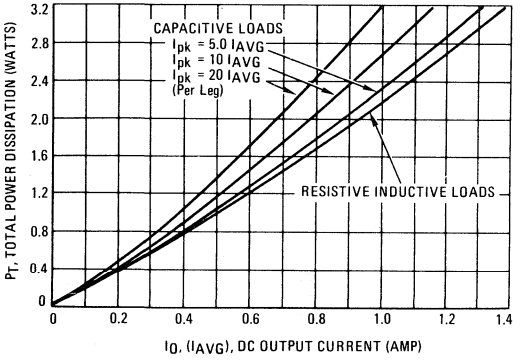
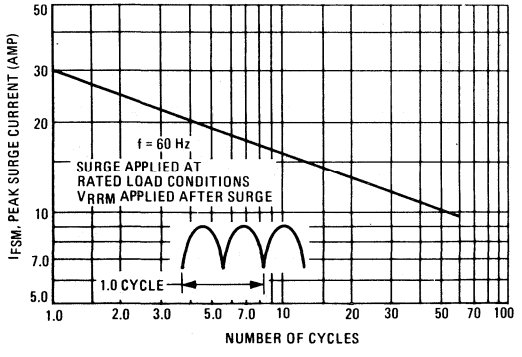


FIGURE 3 – SURGE CURRENT



SINGLE DIODE CHARACTERISTICS

FIGURE 4 – MAXIMUM FORWARD VOLTAGE

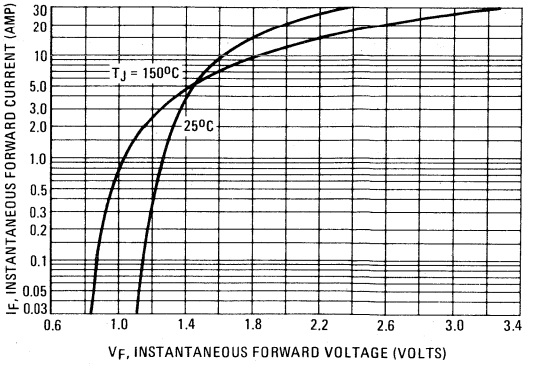


FIGURE 5 – FORWARD RECOVERY TIME

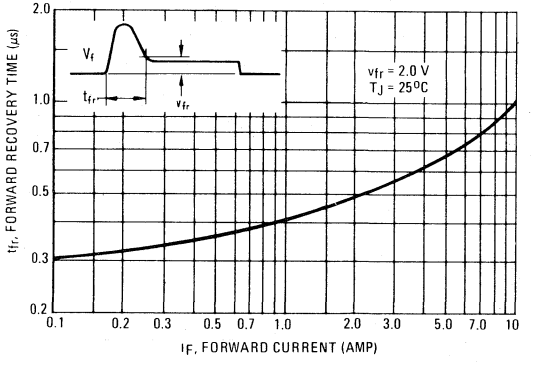
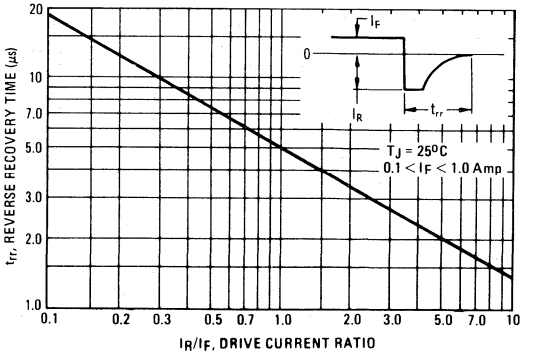


FIGURE 6 – REVERSE RECOVERY TIME



3N253 thru 3N259
(MDA200 Series)

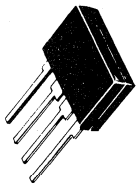
MINIATURE INTEGRAL DIODE ASSEMBLIES

. . . with silicon rectifier chips interconnected and encapsulated into voidless rectifier bridge circuits.

- High Resistance to Shock and Vibration
- High Dielectric Strength
- Built-In Printed Circuit Board Stand-Offs

SINGLE-PHASE
FULL-WAVE BRIDGE

2.0 AMPERES
50-1000 VOLTS



MAXIMUM RATINGS Rating (Per Diode)	Symbol	3N253 MDA200	3N254 MDA201	3N255 MDA202	3N256 MDA204	3N257 MDA206	3N258 MDA208	3N259 MDA210	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
DC Output Voltage Resistive Load Capacitive Load	 Vdc Vdc	 32 50	 64 100	 127 200	 255 400	 382 600	 510 800	 640 1000	 Volts Volts
Sine Wave RMS Input Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase bridge operation, resistive load, 60 Hz, $T_A = 55^oC$)	I_O	2.0							Amp
Non-Repetitive Peak Surge Current (Preceded and followed by rated current and voltage, $T_A = 55^oC$)	I_{FSM}	60 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +165							^oC

ELECTRICAL CHARACTERISTICS

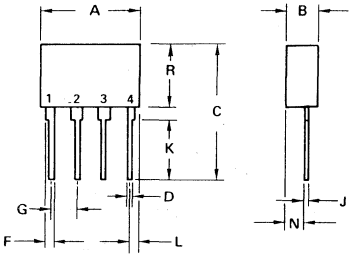
Characteristic	Symbol	Typ	Max	Unit
Instantaneous Forward Voltage (Per Diode) ($i_F = 3.14$ Amp, $T_J = 25^oC$)	v_F	1.0	1.1	Volts
Reverse Current (Per Diode) (Rated V_R, $T_A = 25^oC$) (Rated V_R, $T_A = 100^oC$)	I_R	 – –	 10 100	μA

MECHANICAL CHARACTERISTICS

CASE: Transfer Molded Plastic
POLARITY: Terminal designation on case

(+) for DC output
(-) for DC output
(AC) for AC input

MOUNTING POSITION: Any
WEIGHT: 1.8 grams (approx)
TERMINALS: Readily solderable connections, corrosion resistant.



STYLE 1:
TERM 1. POS
2. AC
3. AC
4. NEG

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	4.57	5.08	0.180	0.200
C	–	20.57	–	0.810
D	0.76	1.02	0.030	0.040
F	1.02	1.27	0.040	0.050
G	3.68	3.94	0.145	0.155
J	0.56	0.71	0.022	0.028
K	–	9.02	–	0.355
L	1.78	2.03	0.070	0.080
N	2.54	2.79	0.100	0.110
R	9.40	10.03	0.370	0.395

CASE 312-02

MAXIMUM RATINGS, BRIDGE OPERATION

FIGURE 1 – CURRENT DERATING

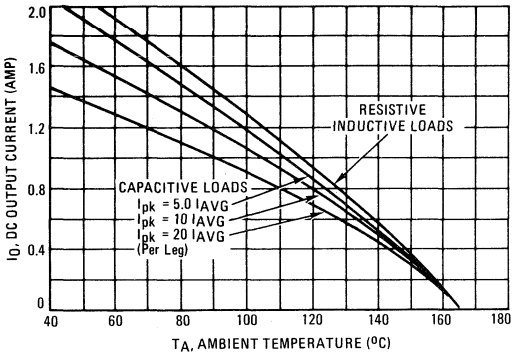


FIGURE 2 – POWER DISSIPATION

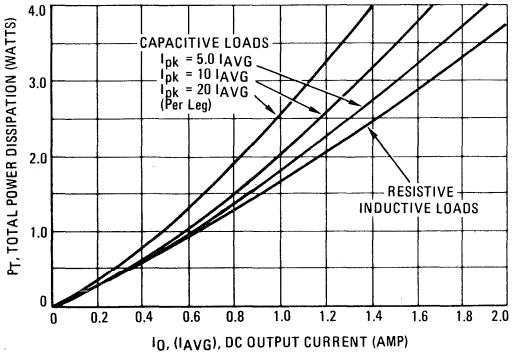
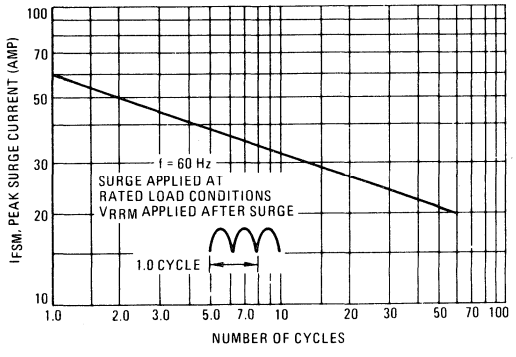


FIGURE 3 – SURGE CURRENT



SINGLE DIODE CHARACTERISTICS

FIGURE 4 – MAXIMUM FORWARD VOLTAGE

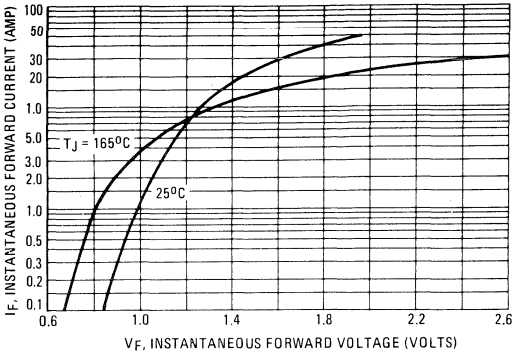


FIGURE 5 – FORWARD RECOVERY TIME

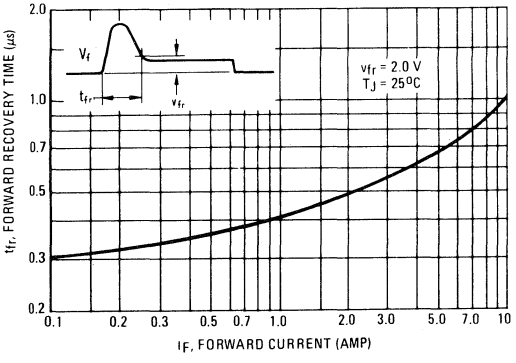
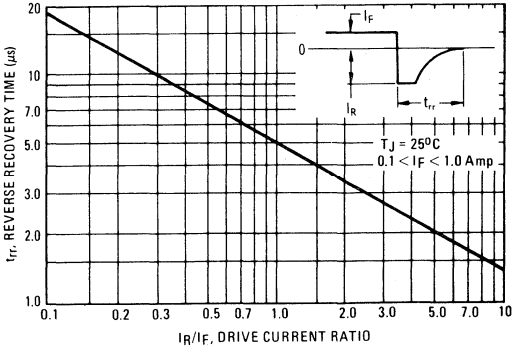


FIGURE 6 – REVERSE RECOVERY TIME



OPTO COUPLED ISOLATORS

Opto Couplers	V_{ISO} Min. V	V_R Max. V	BV_{CEO} Min. V	I_C @ I_F = 10 mA Min. mA	I_C @ I_F = 10 mA Typ. mA	Package	Page
MOC1005	5000	3	30	2	5	673-04	8-1
MOC1006	5000	3	30	1	3	673-04	8-1
4N25, 4N25A	2500	3	30	2	3.5	673-04	8-5
4N26	1500	3	30	2	3.5	673-04	8-5
4N27	1500	3	30	1	2.0	673-04	8-5
4N28	500	3	30	1	2.0	673-04	8-5
4N29	2500	3	30	10	–	673-03	8-9
4N30 (MOC1200)	1500	3	30	10	–	673-03	8-9
4N31	1500	3	30	5	–	673-03	8-9
4N32	2500	3	30	50	–	673-03	8-9
4N33	1500	3	30	50	–	673-03	8-9
4N38	1500	3	80	–	3.5	673-04	8-13
4N38A	2500	3	80	–	3.5	673-04	8-13

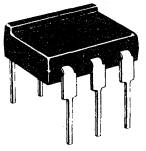
MOC1005
MOC1006

5000 VOLTS – HIGH ISOLATION COUPLER

. . . Gallium Arsenide LED optically coupled to a Silicon Phototransistor designed for applications requiring high electrical isolation, high transistor breakdown-voltage and low-leakage, small package size and low cost; such as interfacing and coupling systems, logic to power circuit interface, and solid-state relays.

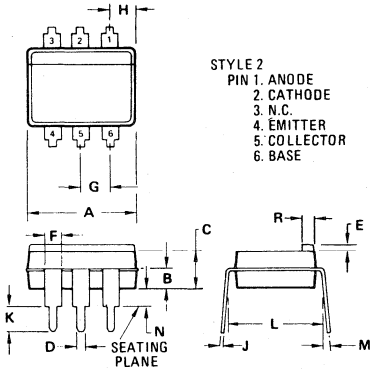
- High Isolation Voltage – V_{ISO} = 5000 V (Min)
- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 80 V (Typ) @ I_C = 1.0 mA
- High Collector Output Current @ I_F = 10 mA – I_C = 5.0 mA (Typ) – MOC1005
  = 3.0 mA (Typ) – MOC1006
- Economical, Compact, Dual-In-Line Plastic Package

INFRARED LIGHT EMITTING DIODE
PHOTOTRANSISTOR
COUPLED PAIR



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted).

Rating	Symbol	Value	Unit
INFRARED-EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	80	mA
Forward Current – Peak Pulse Width = 300 μs, 2.0% Duty Cycle	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	150 2.0	mW mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Total Power Dissipation @ T_A = 25°C Negligible Power in Diode Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE RATINGS			
Total Power Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element Derate above 25°C	P_D	250 3.3	mW mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C



STYLE 2
PIN 1. ANODE
2. CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DOT OR INDEX FOR PIN NO. 1 ORIENT.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.38	0.53	0.015	0.021
E	–	1.02	–	0.040
F	1.02	1.27	0.040	0.050
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.92	3.30	0.115	0.130
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.27	0.020	0.050
R	–	1.90	–	0.075

CASE 673-04

FIGURE 1 – MAXIMUM POWER DISSIPATION

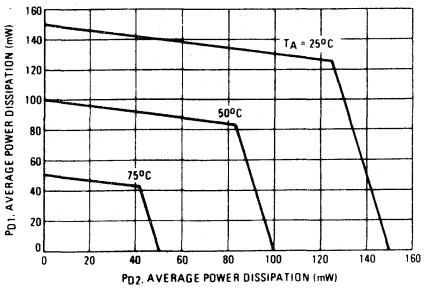


Figure 1 is based upon using limit values in the equation:

$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)

T_A Ambient Temperature

$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)

P_{D1} Power Dissipation in One Chip

P_{D2} Power Dissipation in Other Chip

K_θ Thermal Coupling Coefficient (20%)

Example.

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.

8

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Leakage Current (V_R = 3.0 V)	I_R	–	0.05	100	μA
Forward Voltage (I_F = 10 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	30	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	I_{CEO}	–	3.5	50	nA
Collector-Base Dark Current (V_{CB} = 10 V, Emitter Open)	I_{CBO}	–	–	20	nA
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	BV_{CBO}	70	–	–	Volts
Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	BV_{CEO}	30	80	–	Volts
Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)	BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)	h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	MOC1005	I_C	2.0	5.0	–	mA
	MOC1006		1.0	3.0	–	
Isolation Surge Voltage,(1) DC (2),		V_{ISO}	5000	10000	–	Vdc
AC (3)			5000	10000	–	
Isolation Resistance (4) (V = 500 V)		–	–	10^{11}	–	Ohms
Collector-Emitter Saturation (I_C = 2.0 mA, I_F = 50 mA)		$V_{CE(sat)}$	–	0.2	0.5	Volts
Isolation Capacitance (4) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF
Bandwidth (5) (I_C = 2.0 mA, R_L = 100 Ohms, Figure 11)		–	–	300	–	kHz

SWITCHING CHARACTERISTICS

Delay Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 6 and 8	MOC1005	t_d	–	0.07	–	μs
		MOC1006		–	0.10	–	
Rise Time		MOC1005	t_r	–	0.8	–	μs
		MOC1006		–	2.0	–	
Storage Time	(I_C = 10 mA, V_{CC} = 10 V) Figures 7 and 8	MOC1005	t_s	–	4.0	–	μs
		MOC1006		–	2.0	–	
Fall Time		MOC1005	t_f	–	7.0	–	μs
		MOC1006		–	3.0	–	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%
(2) Peak DC Voltage – 1.0 Minute
(3) Non-Repetitive Peak AC Voltage – 1 Full Cycle, Sine Wave, 60 Hz
(4) For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common.
(5) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA p-p at 10 kHz.

8

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 2 – MOC1005

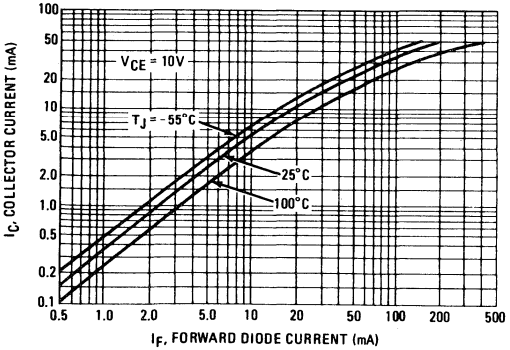
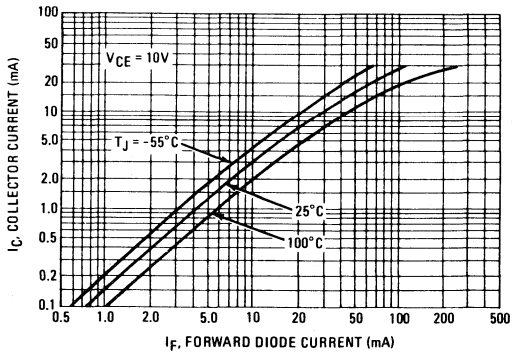


FIGURE 3 – MOC1006



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 4 – DIODE FORWARD CHARACTERISTICS

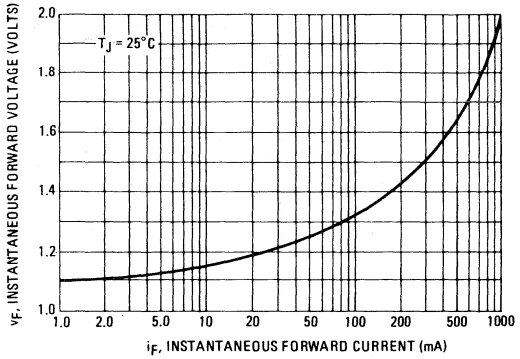


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

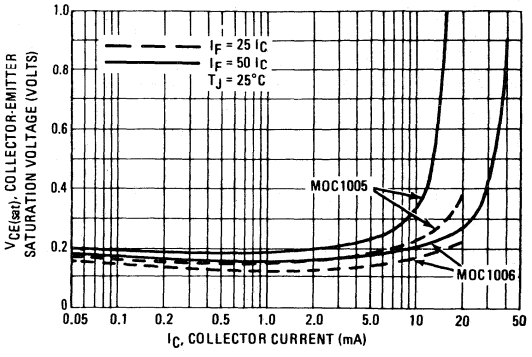


FIGURE 6 – TURN-ON TIME

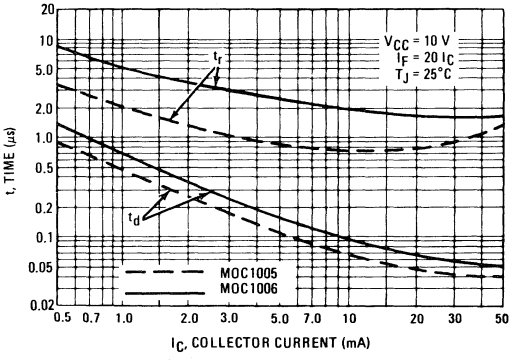


FIGURE 7 – TURN-OFF TIME

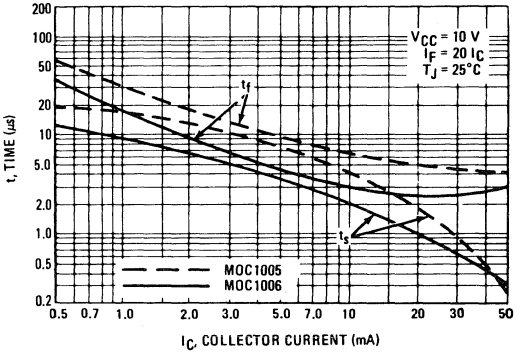


FIGURE 8 – SATURATED SWITCHING TEST CIRCUIT

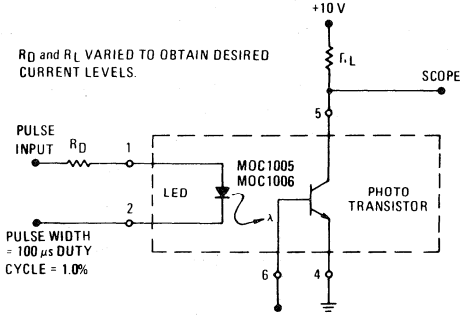


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE

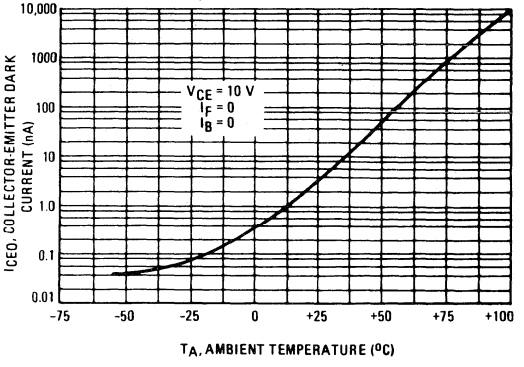


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FIGURE 10 – FREQUENCY RESPONSE

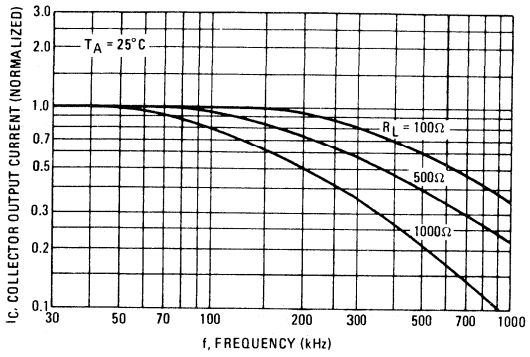


FIGURE 11 – FREQUENCY RESPONSE TEST CIRCUIT

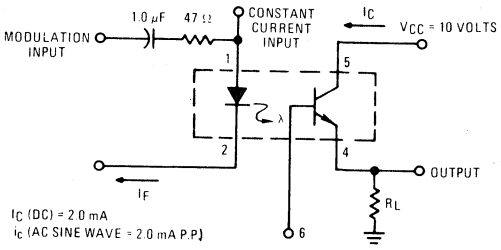


FIGURE 12 – POWER AMPLIFIER

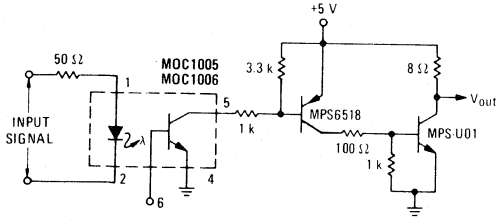


FIGURE 13 – INTERFACE BETWEEN LOGIC AND LOAD

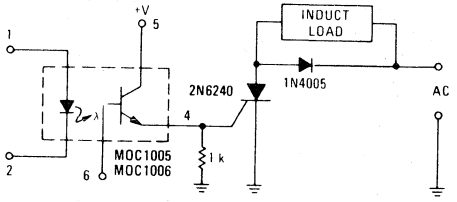


FIGURE 14 – UNIVERSAL CMOS LOGIC TRANSLATOR
(Programmable Constant Current Drive)

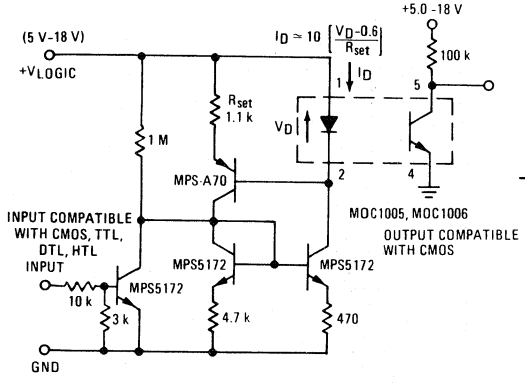
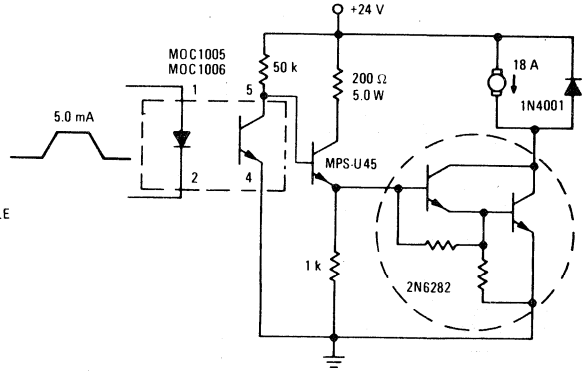


FIGURE 15 – ISOLATED DC MOTOR CONTROLLER



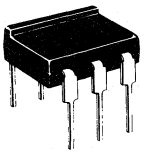
4N25 • 4N25A
4N26 • 4N27 • 4N28

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

...Gallium Arsenide LED optically coupled to a Silicon Photo Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage —
  V_{ISO} = 2500 V (Min) — 4N25,A
  1500 V (Min) — 4N26,4N27
  500 V (Min) — 4N28
- High Collector Output Current @ I_F = 10 mA —
  I_C = 3.5 mA (Typ) — 4N25,A,4N26
  2.0 mA (Typ) — 4N27,4N28
- Economical, Compact, Dual-In-Line Package
- Excellent Frequency Response — 300 kHz (Typ)
- Fast Switching Times @ I_C = 10 mA
  t_{on} = 0.87 μs (Typ) — 4N25,A,4N26
  2.1 μs (Typ) — 4N27,4N28
  t_{off} = 11 μs (Typ) — 4N25,A,4N26
  5.0 μs (Typ) — 4N27,4N28
- 4N25A is UL Recognized

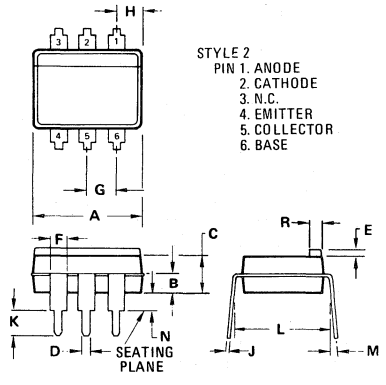
INFRARED LIGHT EMITTING DIODE PHOTOTRANSISTOR COUPLED PAIR



*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted).

Rating	Symbol	Value	Unit
INFRARED-EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	80	mA
Forward Current — Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C (Negligible Power in Transistor)	P_D	150	mW
Derate above 25°C		2.0	mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Total Device Dissipation @ T_A = 25°C	P_D	150	mW
Negligible Power in Diode (Derate above 25°C)		2.0	mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C	P_D	250	mW
Equal Power Dissipation in Each Element (Derate above 25°C)		3.3	mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

*Indicates JEDEC Registered Data.



STYLE 2
PIN 1. ANODE
2. CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.38	0.53	0.015	0.021
E	—	1.02	—	0.040
F	1.02	1.27	0.040	0.050
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H	1.57	1.83	0.062	0.072
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K	2.92	3.30	0.115	0.130
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.27	0.020	0.050
R	—	1.90	—	0.075

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. INDEX FOR PIN NO. 1 ORIENT.

CASE 673-04

FIGURE 1 — MAXIMUM POWER DISSIPATION

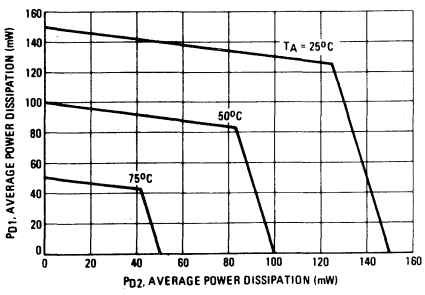


Figure 1 is based upon using limit values in the equation:

$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:
With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.

8

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 10 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	4N25,A 4N26, 4N27 4N28	I_{CEO}	– –	3.5 –	50 100	nA
*Collector-Base Dark Current (V_{CB} = 10 V, Emitter Open)		I_{CBO}	–	–	20	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)		BV_{CBO}	70	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)		BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)		BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V I_C = 500 μA)		h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N25,A, 4N26 4N27,4N28	I_C	2.0 1.0	3.5 2.0	– –	mA
*Isolation Voltage (2) (60 Hz Peak) (60 Hz RMS For 1 Second) (3)	4N25,A 4N26,4N27 4N28 4N25A	V_{ISO}	2500 1500 500 1775	– – – –	– – – –	Volts
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation (I_C = 2.0 mA, I_F = 50 mA)		$V_{CE(sat)}$	–	0.2	0.5	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF
Bandwidth (4) (I_C = 2.0 mA, R_L = 100 ohms, Figure 11) Note 2		–	–	300	–	kHz

SWITCHING CHARACTERISTICS

Delay Time	(I_C = 10 mA, V_{CC} = 10 V)	4N25,A,4N26 4N27,4N28	t_d	– –	0.07 0.10	– –	μs
Rise Time	Figures 6 and 8	4N25,A,4N26 4N27,4N28	t_r	– –	0.8 2.0	– –	μs
Storage Time	(I_C = 10 mA, V_{CC} = 10 V)	4N25,A,4N26 4N27,4N28	t_s	– –	4.0 2.0	– –	μs
Fall Time	Figures 7 and 8	4N25,A,4N26 4N27,4N28	t_f	– –	7.0 3.0	– –	μs

*Indicates JEDEC Registered Data. (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common.

(3) RMS Volts, 60 Hz, For this test, pins 1, 2, and 3 are common and pins 4, 5, and 6 are common.

(4) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA p-p at 10 kHz.

8

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N25,A,4N26

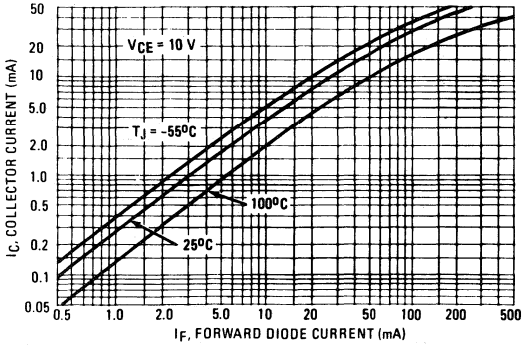
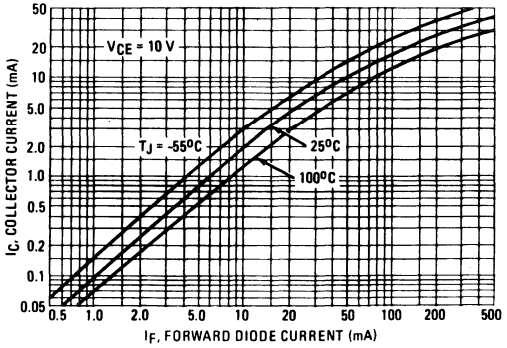


FIGURE 3 – 4N27, 4N28



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 4 – DIODE FORWARD CHARACTERISTICS

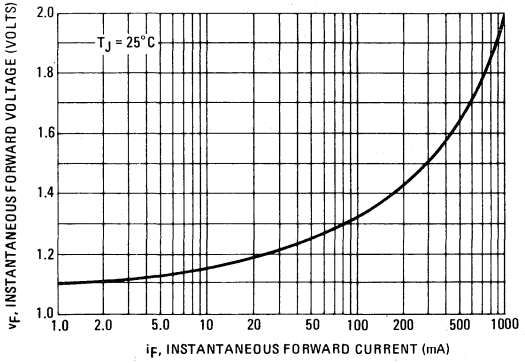


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

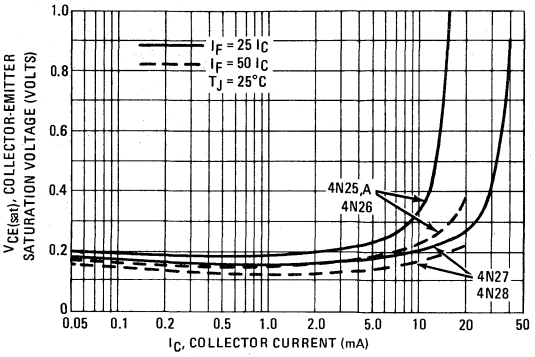


FIGURE 6 – TURN-ON TIME

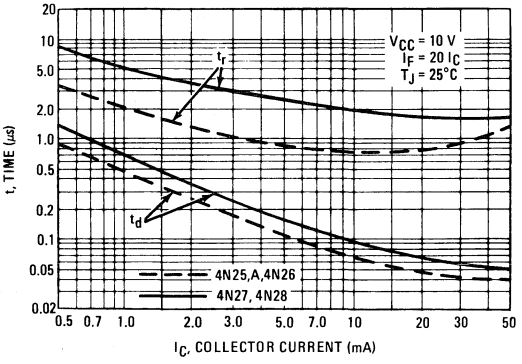


FIGURE 7 – TURN-OFF TIME

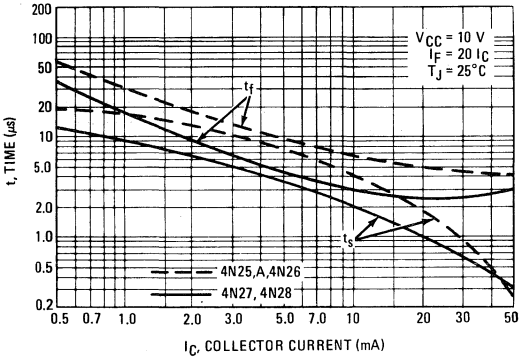


FIGURE 8 – SATURATED SWITCHING TIME TEST CIRCUIT

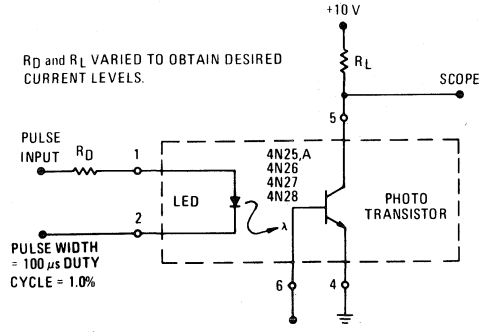


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE

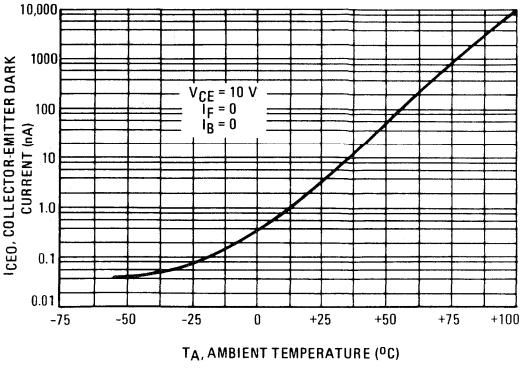


FIGURE 10 – FREQUENCY RESPONSE

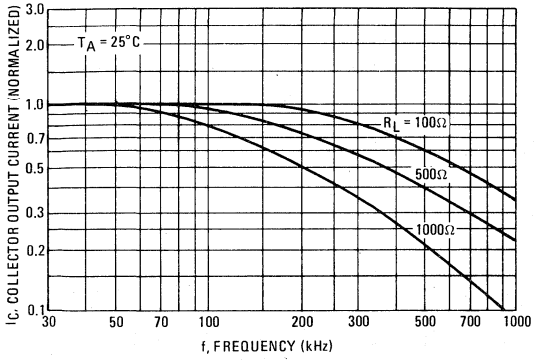
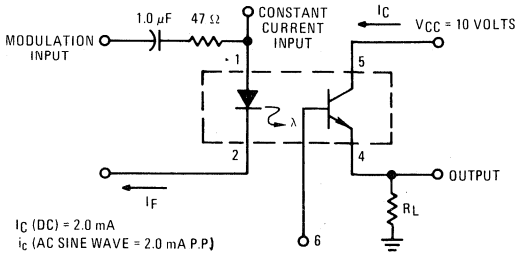


FIGURE 11 – FREQUENCY RESPONSE TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 12 – ISOLATED MTTL TO MOS (P-CHANNEL) LEVEL TRANSLATOR

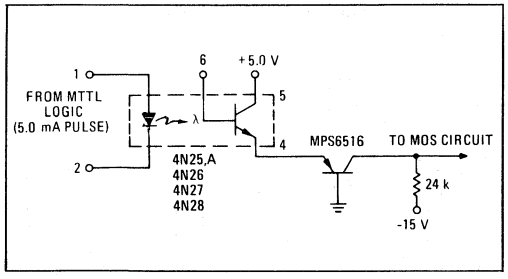


FIGURE 13 – COMPUTER/PERIPHERAL INTERCONNECT

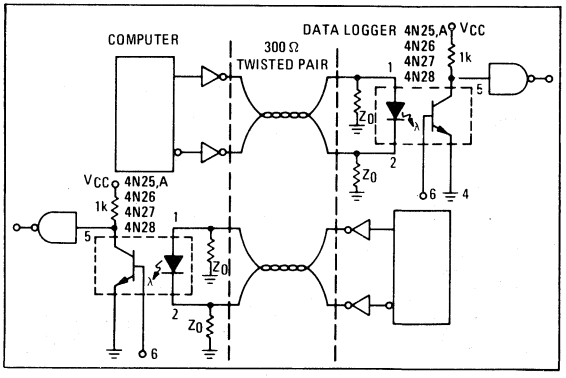


FIGURE 14 – POWER AMPLIFIER

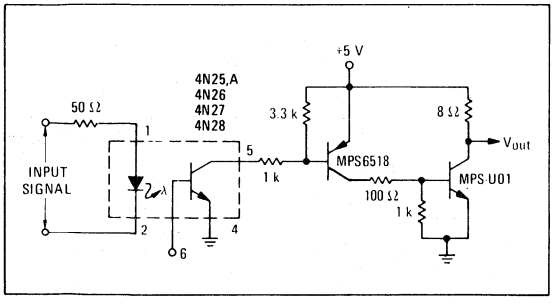
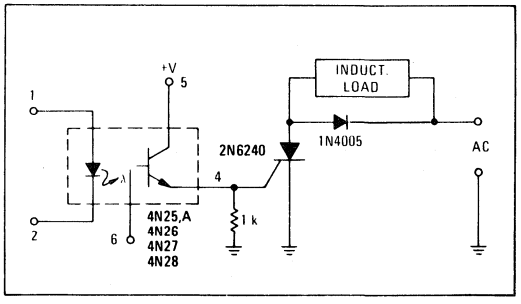


FIGURE 15 – INTERFACE BETWEEN LOGIC AND LOAD



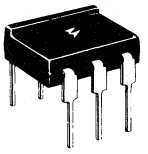
4N29 • 4N30 (MOC1200)
4N31 • 4N32 • 4N33

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Darlington Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage — V_{ISO} = 2500 V (Min) — 4N29,32; 1500 V (Min) — 4N30,31,33
- Excellent Frequency Response — 30 kHz (Typ)
- High Collector Output Current @ I_F = 10 mA — I_C = 50 mA (Min) — 4N32,33; 10 mA (Min) — 4N29,30; 5.0 mA (Min) — 4N31
- Fast Switching Times @ I_C = 50 mA t_{on} = 0.6 μs (Typ); t_{off} = 17 μs (Typ) — 4N29,30,31; 45 μs (Typ) — 4N32,33
- Economical, Compact, Dual-In-Line Package

INFRARED LIGHT EMITTING DIODE PHOTO DARLINGTON TRANSISTOR COUPLED PAIR



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED-EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	80	mA
Forward Current — Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	150 2.0	mW mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	5.0	Volts
Collector-Base Voltage	V_{CBO}	30	Volts
Total Power Dissipation @ T_A = 25°C Negligible Power in Diode Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element Derate above 25°C	P_D	250 3.3	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)	—	260	°C

FIGURE 1 — MAXIMUM POWER DISSIPATION

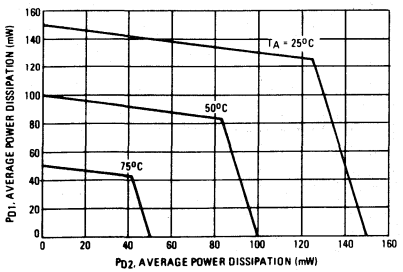


Figure 1 is based upon using limit values in the equation:

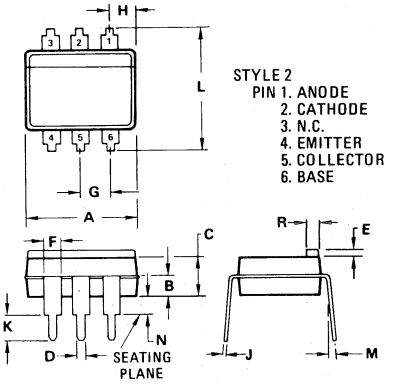
$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the Darlington P_D (P_{D2}) must be less than 50 mW.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.64	0.89	0.025	0.035
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.54	3.30	0.100	0.130
L	7.37	7.87	0.290	0.310
M	—	5°	—	5°
N	—	1.27	—	0.050
R	1.52	1.78	0.060	0.070

CASE 673-03

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V, R_L = 1.0 M ohms)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 50 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 10 V, Base Open)	I_{CEO}	–	–	100	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	BV_{CBO}	30	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 100 μA, I_B = 0)	BV_{CEO}	30	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)	BV_{ECO}	5.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)	h_{FE}	–	5000	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Collector Output Current (1) (V_{CE} = 10 V, I_F = 10 mA, I_B = 0)	4N32, 4N33	I_C	50	–	–	mA
	4N29, 4N30		10	–	–	
	4N31		5.0	–	–	
*Isolation Voltage (2)	4N29, 4N32	V_{ISO}	2500	–	–	Volts
	4N30, 4N31, 4N33		1500	–	–	
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation Voltage (1) (I_C = 2.0 mA, I_F = 8.0 mA)	4N31	$V_{CE(sat)}$	–	–	1.2	Volts
	4N29, 4N30, 4N32, 4N33		–	–	1.0	
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	0.8	–	pF
Bandwidth (3) (I_C = 2.0 mA, R_L = 100 ohms, Figures 6 and 8)		–	–	30	–	kHz

SWITCHING CHARACTERISTICS (Figures 7 and 9), (4)

Turn-On Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)		t_{on}	–	0.6	5.0	μs
Turn-Off Time (I_C = 50 mA, I_F = 200 mA, V_{CC} = 10 V)	4N29,30,31	t_{off}	–	17	40	μs
	4N32,33		–	45	100	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4,5 and 6 are common.

(3) I_F adjusted to yield I_C = 2.0 mA and i_c = 2.0 mA P-P at 10 kHz.

(4) t_d and t_r are inversely proportional to the amplitude of I_F; t_s and t_f are not significantly affected by I_F.

DC CURRENT TRANSFER CHARACTERISTICS

FIGURE 2 – 4N29, 4N30, 4N31

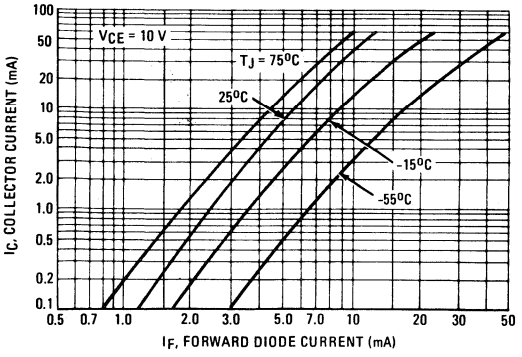
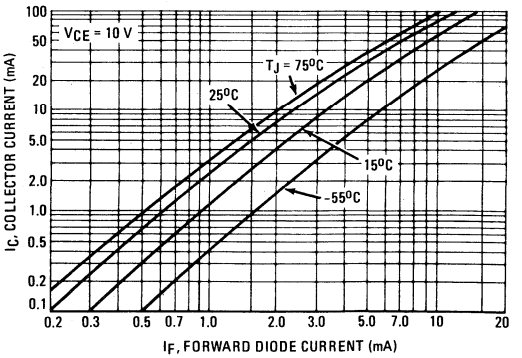


FIGURE 3 – 4N32, 4N33



TYPICAL ELECTRICAL CHARACTERISTICS
(Printed Circuit Board Mounting)

FIGURE 4 – DIODE FORWARD CHARACTERISTIC

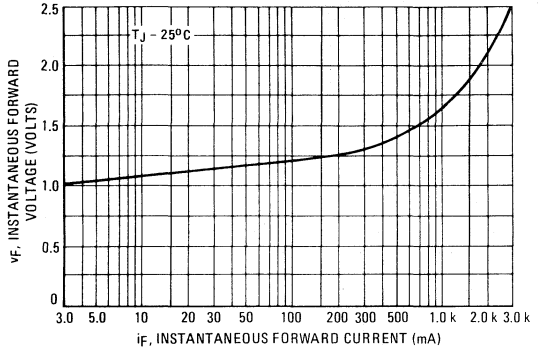


FIGURE 5 – COLLECTOR-EMITTER CUTOFF CURRENT

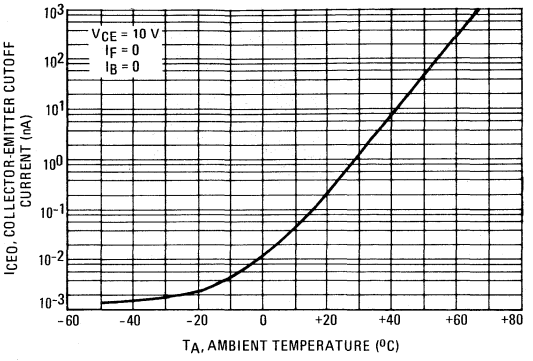


FIGURE 6 – FREQUENCY RESPONSE

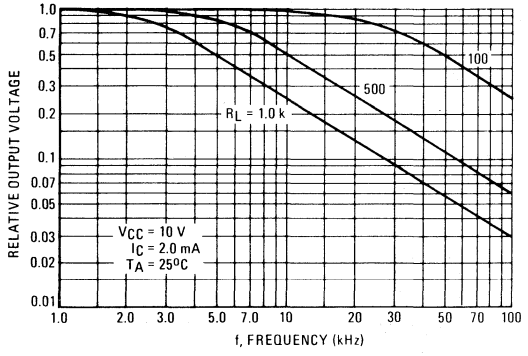


FIGURE 7 – SWITCHING TIMES

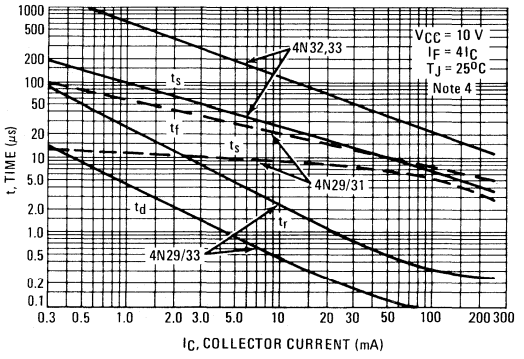


FIGURE 8 – FREQUENCY RESPONSE TEST CIRCUIT

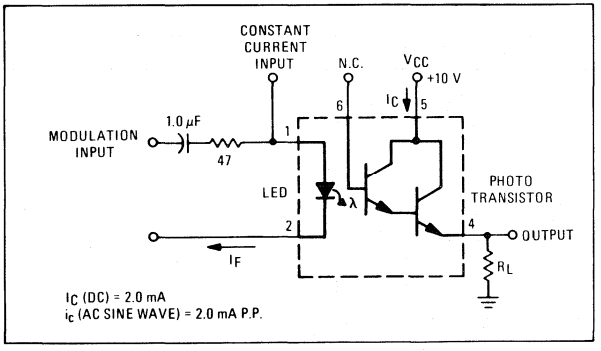
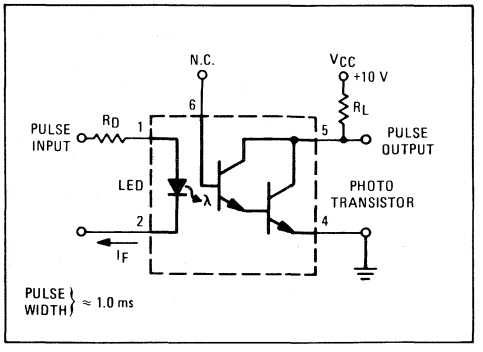


FIGURE 9 – SWITCHING TIME TEST CIRCUIT



TYPICAL APPLICATIONS

FIGURE 10 – VOLTAGE CONTROLLED TRIAC

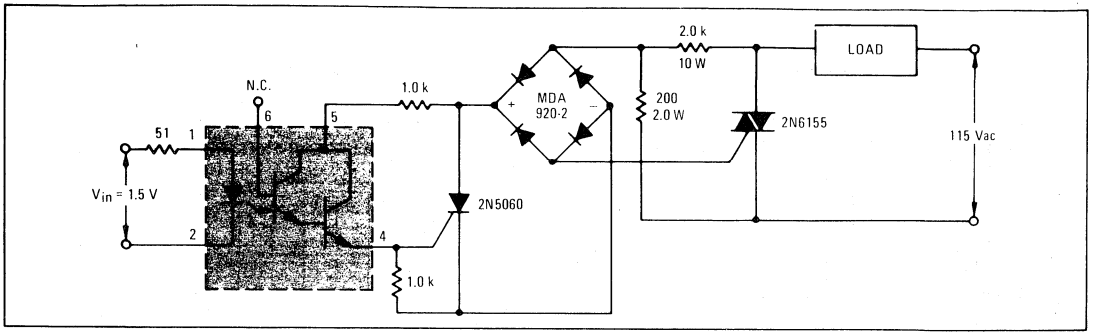


FIGURE 11 – AC SOLID STATE RELAY

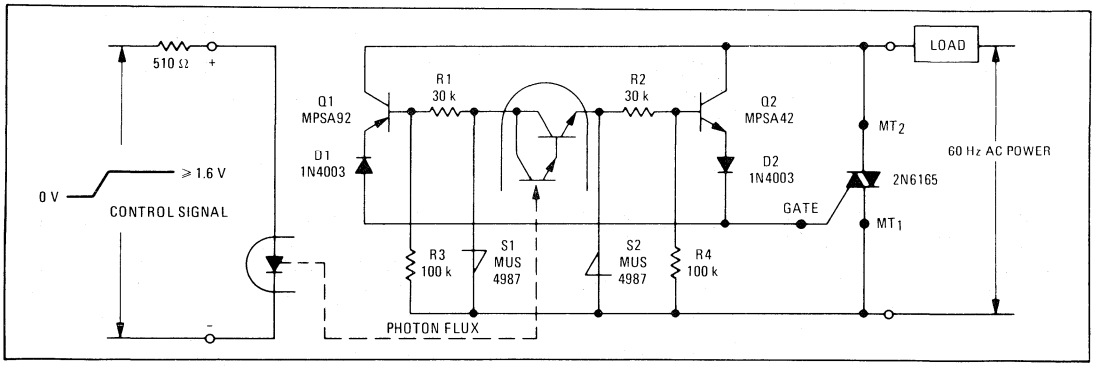


FIGURE 12 – OPTICALLY COUPLED ONE SHOT

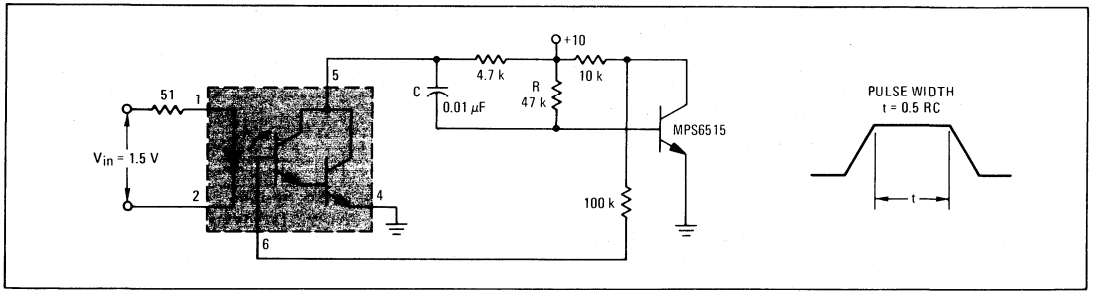
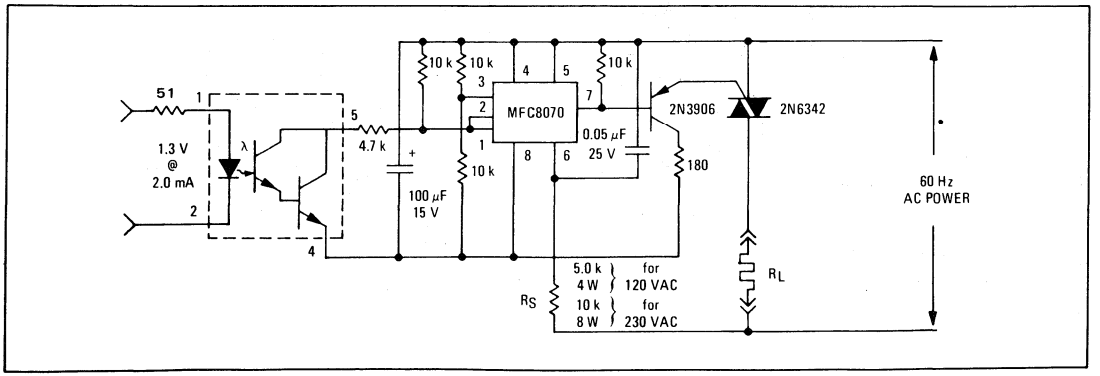


FIGURE 13 – ZERO VOLTAGE SWITCH



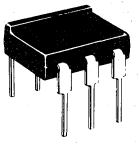
4N38
4N38A

OPTICAL COUPLER WITH NPN TRANSISTOR OUTPUT

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Transistor. Designed for applications requiring electrical isolation, high breakdown voltage and low leakage, such as Teletype Interfacing, Telephone Line pulsing and driving high voltage relays.

- High Isolation Voltage –
  V_{ISO} = 1500 V (Min) – 4N38
  = 2500 V (Min) – 4N38A
- High Collector Emitter Breakdown Voltage –
  BV_{CEO} = 80 V (Min)
- Economical Dual-In-Line Package
- 4N38A UL Recognized

INFRARED LIGHT EMITTING DIODE
PHOTOTRANSISTOR
COUPLED PAIR



***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current – Continuous	I_F	80	mA
Forward Current – Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Device Dissipation @ T_A = 25°C (Negligible Power in Transistor)	P_D	150	mW
Derate above 25°C		2.0	mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	80	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	80	Volts
Total Device Dissipation @ T_A = 25°C (Negligible Power in Diode)	P_D	150	mW
Derate above 25°C		2.0	mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C (Equal Power Dissipation in Each Element)	P_D	250	mW
Derate above 25°C		3.3	mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

* Indicates JEDEC Registered Data.

FIGURE 1 – MAXIMUM POWER DISSIPATION

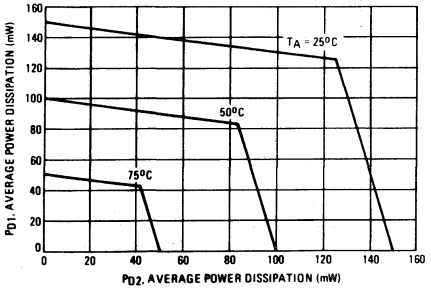


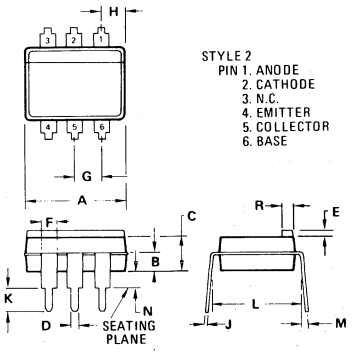
Figure 1 is based upon using limit values in the equation:

$T_{J1} - T_A = R_{\theta JA} (P_{D1} + K_\theta P_{D2})$

where:

T_{J1} Junction Temperature (100°C)
T_A Ambient Temperature
$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)
P_{D1} Power Dissipation in One Chip
P_{D2} Power Dissipation in Other Chip
K_θ Thermal Coupling Coefficient (20%)

Example:
With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW.



STYLE 2
PIN 1. ANODE
2. CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.38	0.53	0.015	0.021
E	–	1.02	–	0.040
F	1.02	1.27	0.040	0.050
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.92	3.30	0.115	0.130
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.27	0.020	0.050
R	–	1.90	–	0.075

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DOT OR INDEX FOR PIN NO. 1 ORIENT.

CASE 673-04

LED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Reverse Leakage Current (V_R = 3.0 V)	I_R	–	0.05	100	μA
*Forward Voltage (I_F = 10 mA)	V_F	–	1.2	1.5	Volts
Capacitance (V_R = 0 V, f = 1.0 MHz)	C	–	150	–	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Collector-Emitter Dark Current (V_{CE} = 60 V, Base Open)	I_{CEO}	–	3.5	50	nA
*Collector-Base Dark Current (V_{CB} = 60 V, Emitter Open)	I_{CBO}	–	–	–	nA
*Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	BV_{CBO}	80	–	–	Volts
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	BV_{CEO}	80	–	–	Volts
*Emitter-Collector Breakdown Voltage (I_E = 100 μA, I_B = 0)	BV_{ECO}	7.0	–	–	Volts
DC Current Gain (V_{CE} = 5.0 V, I_C = 500 μA)	h_{FE}	–	250	–	–

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Isolation Voltage (2)		V_{ISO}				Volts
(60 Hz Peak ac)	4N38		1500	–	–	
	4N38A		2500	–	–	
(60 Hz RMS for 1 second)	4N38A		1775	–	–	
Isolation Resistance (2) (V = 500 V)		–	–	10^{11}	–	Ohms
*Collector-Emitter Saturation (I_C = 4.0 mA, I_F = 20 mA)		$V_{CE(sat)}$	–	–	1.0	Volts
Isolation Capacitance (2) (V = 0, f = 1.0 MHz)		–	–	1.3	–	pF

SWITCHING CHARACTERISTICS

Delay Time	(I_C = 10 mA, V_{CC} = 10 V)	t_d	–	0.07	–	μs
Rise Time	Figures 6 and 8	t_r	–	0.8	–	μs
Storage Time	(I_C = 10 mA, V_{CC} = 10 V)	t_s	–	4.0	–	μs
Fall Time	Figures 7 and 8	t_f	–	7.0	–	μs

*Indicates JEDEC Registered Data. (1) Pulse Test; Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
(2) For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common.

TYPICAL TRANSFER CHARACTERISTICS

FIGURE 2 – COLLECTOR-CURRENT versus DIODE FORWARD CURRENT

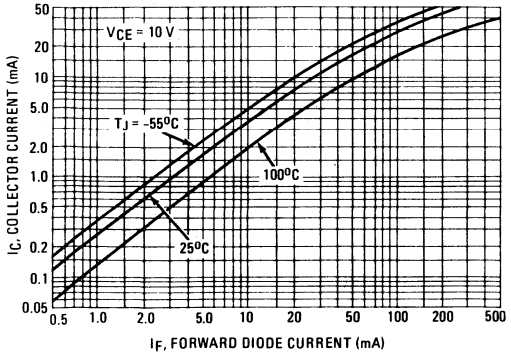
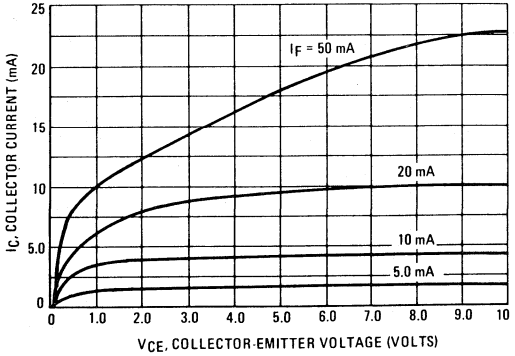


FIGURE 3 – COLLECTOR-CURRENT versus COLLECTOR-EMITTER VOLTAGE



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 4 – DIODE FORWARD CHARACTERISTICS

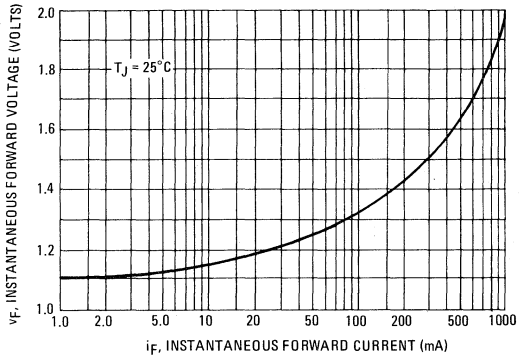


FIGURE 5 – COLLECTOR SATURATION VOLTAGE

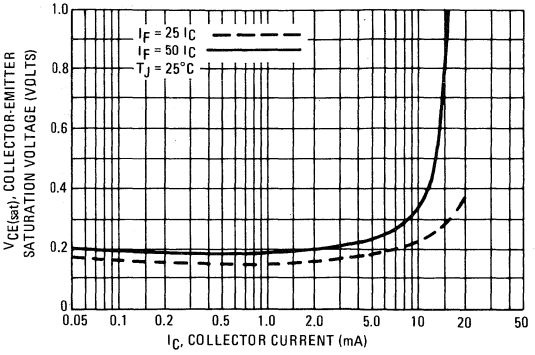


FIGURE 6 – TURN-ON TIME

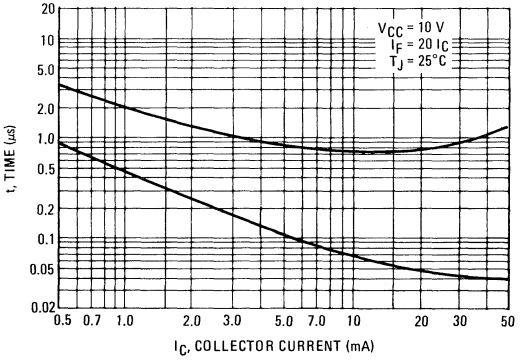


FIGURE 7 – TURN-OFF TIME

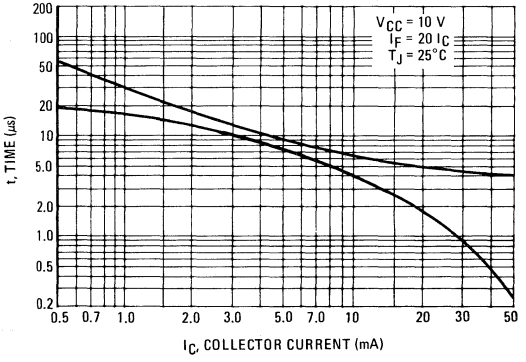


FIGURE 8 – SATURATED SWITCHING TIME TEST CIRCUIT

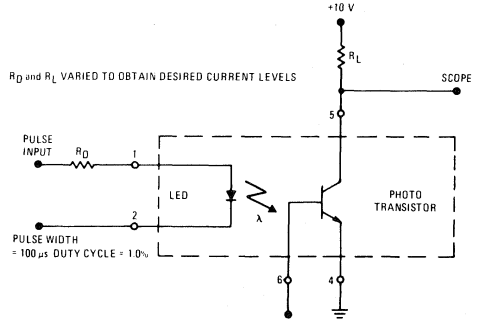
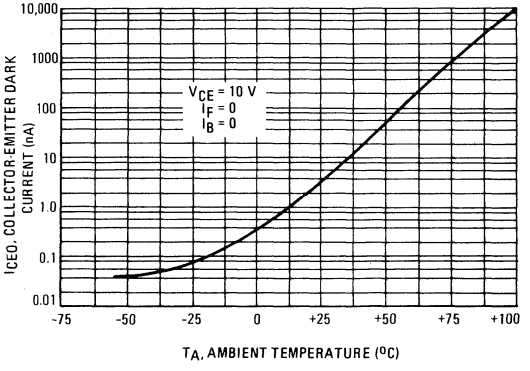


FIGURE 9 – DARK CURRENT versus AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

The applications below utilize the 80 volt breakdown capability of the 4N38 and 4N38A eliminating the need for divider networks, zener diodes and the associated assembly costs.

FIGURE 10 – TYPICAL TELETYPE INTERFACE

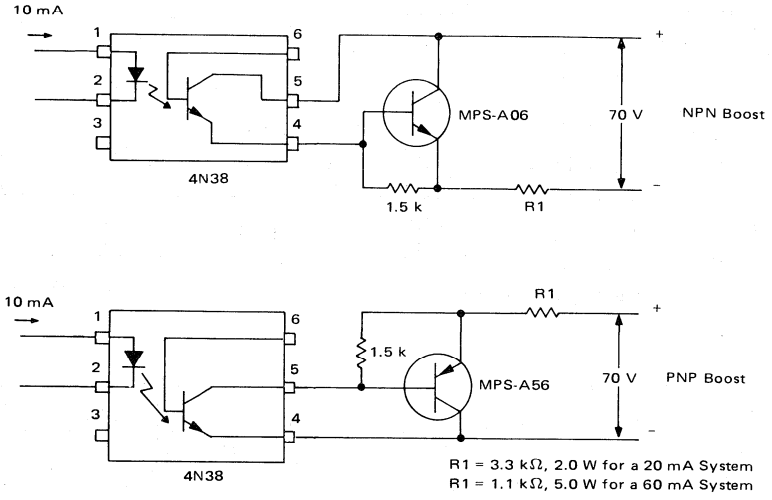


FIGURE 11 – TELEPHONE LINE PULSE CIRCUIT

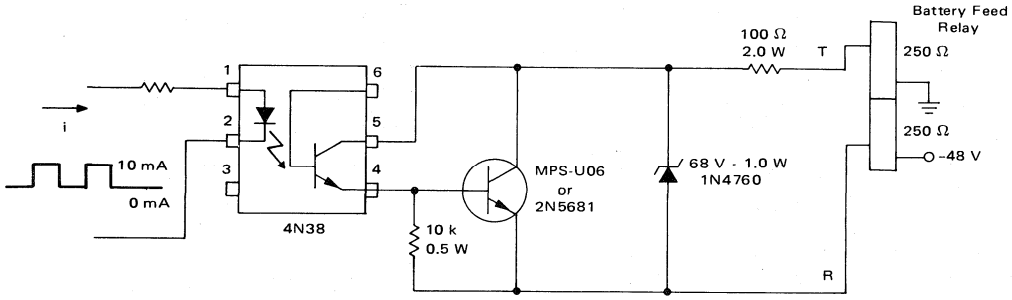
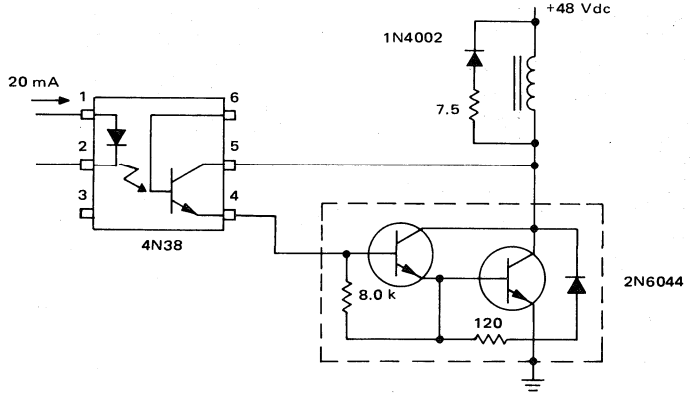


FIGURE 12 – 4-AMPERE SOLENOID DRIVER



INTEGRATED CIRCUITS

Integrated Circuits For General Applications		Package	Page
MC3301	Quad, Single Supply Operational Amplifiers	646	9-71
MC3302	Quad, Single Supply Comparators	646, 632	9-79
MC3340	Electronic Attenuator	626	9-92
MC3344	Programmable Frequency Switch	646, 632	9-95
MC3346	Transistor Arrays	646	9-100
MC3386			9-100
MC3401	Quad, Single Supply Operational Amplifiers	646	9-103
MC3403	Quad Low Power Operational Amplifiers	646, 632	9-111
MC3420	Switchmode Regulator Control Circuit	648, 620	9-117
MC3456	Dual Timing circuits	646	9-137
MC3556		646, 632	9-137
MC14066	Quad Analog Switch	646, 632	9-208
MC14433	Dual Ramp A-D Converter, 3½ Digit	709, 716	9-239

Fixed Voltage Regulators	Polarity	V_O Nom V	V_{IN} V Max.	I_O Max. mA	Package	Page
MC7805C-MC7824C	Positive	5-24	35-40	1500	TO-220, 11	9-169
MC78L05C, AC-MC78L24C, AC	Positive	5-24	30-40	100	TO-92, TO-39	9-180
MC78M05C-MC78M24C	Positive	5-24	35-40	750	TO-39, 199	9-184
MC7902C-MC7924C	Negative	2-24	35-40	1500	TO-220, 11	9-192
MC79L03C, AC-MC79L24C, AC	Negative	3-24	35-40	100	TO-92, TO-39	9-201

Integrated Circuits for Automotive Applications		Package	Page
MC3301	Quad Single Supply Operational Amplifier	646	9-71
MC3302	Quad Single Supply Comparator	646, 632	9-79
MC3325	Voltage Regulator	646	9-83
MC3333	Vari-Dwell Ignition Circuit	646	9-88
MC14460	Automotive Speed Control Processor	648	9-251

Integrated Circuits for Appliance Applications		Package	Page
MC14433	Dual Ramp A-D Converter, 3½ Digit	709, 716	9-239
UAA1004	Zero Voltage Switch	626, TO-99	9-295

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	Integrated Circuits for Television, Radio and HI-FI Applications	Package	Page
MC1310	FM Stereo Demodulator	646	9-1
MC1312	SQ Decoder	646	9-9
MC1314	Voltage Controlled Attenuator } CBS SQ Logic Decoder System	648	9-9
MC1315	Logic Circuit	648	9-9
MC1327	Dual Doubly Balanced Chroma Demodulator	646, 647	9-21
MC1327A	Chrominance Demodulator	646	9-25
MC1330A	Low Level Video Detector	626	9-30
MC1349	IF Amplifier with 80dB AGC Range up to 45 MHz	626	9-37
MC1350	IF Amplifier with Wide AGC Range	626	9-43
MC1355	Balanced Four Stage High Gain FM/IF Amplifier	646, 647	9-47
MC1356	FM Detector and Limiter	646	9-51
MC1358	TV-IF Amplifier, Limiter, FM Detector, Audio Driver and Electronic Attenuator	646	9-55
MC1496 }	Balanced Modulator, Demodulator	646, 632, 603	9-61
MC1596 }		632, 603	9-61
MC3340	Electronic Attenuator	626	9-92
MC3420	Switchmode Regulator Control Circuit	648, 620	9-117
MC6525	Remote Control Receiver – 12 Programmes	710-01	9-145
MC6526	Remote Control Receiver – 8/16/32 Programmes	710-01	9-153
MC6529	Remote Control Receiver – 8/12/16 Programmes	710-01	9-161
MC14422	Remote Control Transmitter – 22ch	648	9-214
MC14424	Remote Control Transmitter – 31ch	648	9-221
MC14425	Tuning Memory System Control Circuit (in conjunction with UAA1008A, MC14426)	701	9-226
MC14426	Tuning Memory System Memory Circuit – 8ch (in conjunction with MC14425 or MC14429)	648	9-230
MC14429	Tuning Memory System Control Circuit (in conjunction with UAA1008A, MC14426)	701	9-234
MC14430	TV, Radio Programme, Address Encoder – 8 Programmes	648	9-238
SAA1006	Diode Matrix Encoder – 16 Lines to 4 Bits	648	9-257
TBA120C, D	FM/IF Amplifier, Limiter and Detector	646	9-259
TBA120U	FM/IF Amplifier, Limiter and Detector	646	9-264
TBA395	TV Chrominance Combination (used in conjunction with TBA396 and TBA327 or MC1327)	646	9-267
TBA396	TV Luminance, Chrominance (used in conjunction with TBA395 and TDA3950 or MC1327)	646	9-271
TBA920, 920S	TV Horizontal Combination with Line Oscillator	648	9-275
TCA4500A	FM Stereo Demodulator for use in HI-FI and Car Radios	648	9-278
TDA1190Z	TV Audio System	722A	9-286
TDA2002	8 Watt Audio Power Amplifier	314A, B	9-290
TDA3950	TV Chrominance combination (used in conjunction with TBA396, MC1327)	646	9-292
UAA1008A	Tuning Memory System, Linear Processor (in conjunction with MC14426 and MC14425 or MC14429)	724	9-300

Specifications and Applications Information

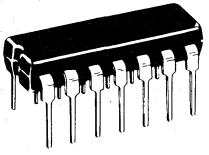
FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FM STEREO
DEMODULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



CASE 646

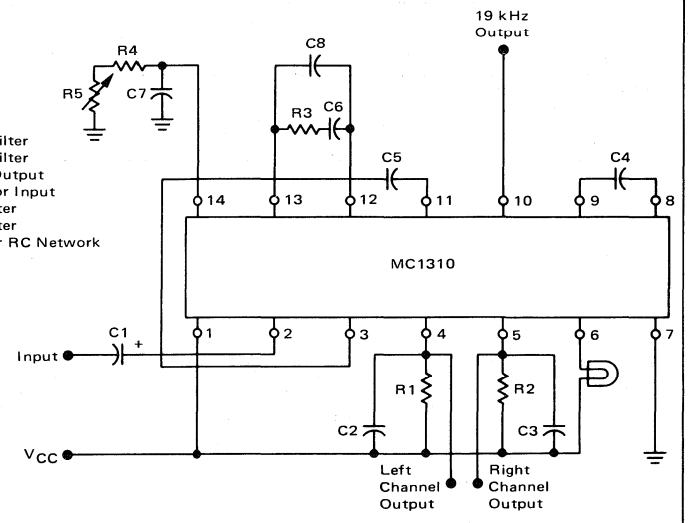
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}	Pin 8 = Switch Filter
Pin 2 = Input	Pin 9 = Switch Filter
Pin 3 = Amplifier Output	Pin 10 = 19 kHz Output
Pin 4 = Left Channel Output	Pin 11 = Modulator Input
Pin 5 = Right Channel Output	Pin 12 = Loop Filter
Pin 6 = Lamp Indicator	Pin 13 = Loop Filter
Pin 7 = Ground	Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 μF	C8 = 0.25 μF
C2 = 0.02 μF	R1 = 3.9 kΩ
C3 = 0.02 μF	R2 = 3.9 kΩ
C4 = 0.25 μF	R3 = 1.0 kΩ
C5 = 0.05 μF	R4 = 16 kΩ
C6 = 0.5 μF	R5 = 5.0 kΩ
C7 = 470 pF	



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MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{(p-p)}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	–	–	$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8	–	–	$V_{(p-p)}$
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Audio Output Voltage (desired channel)	–	485	–	mV(RMS)
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.3	–	%
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	34.4 45	– –	dB
Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level 19 kHz input level for lamp "on" 19 kHz input level for lamp "off"	 – 5.0	 – –	 20 –	mV(RMS)
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	13	–	mAdc

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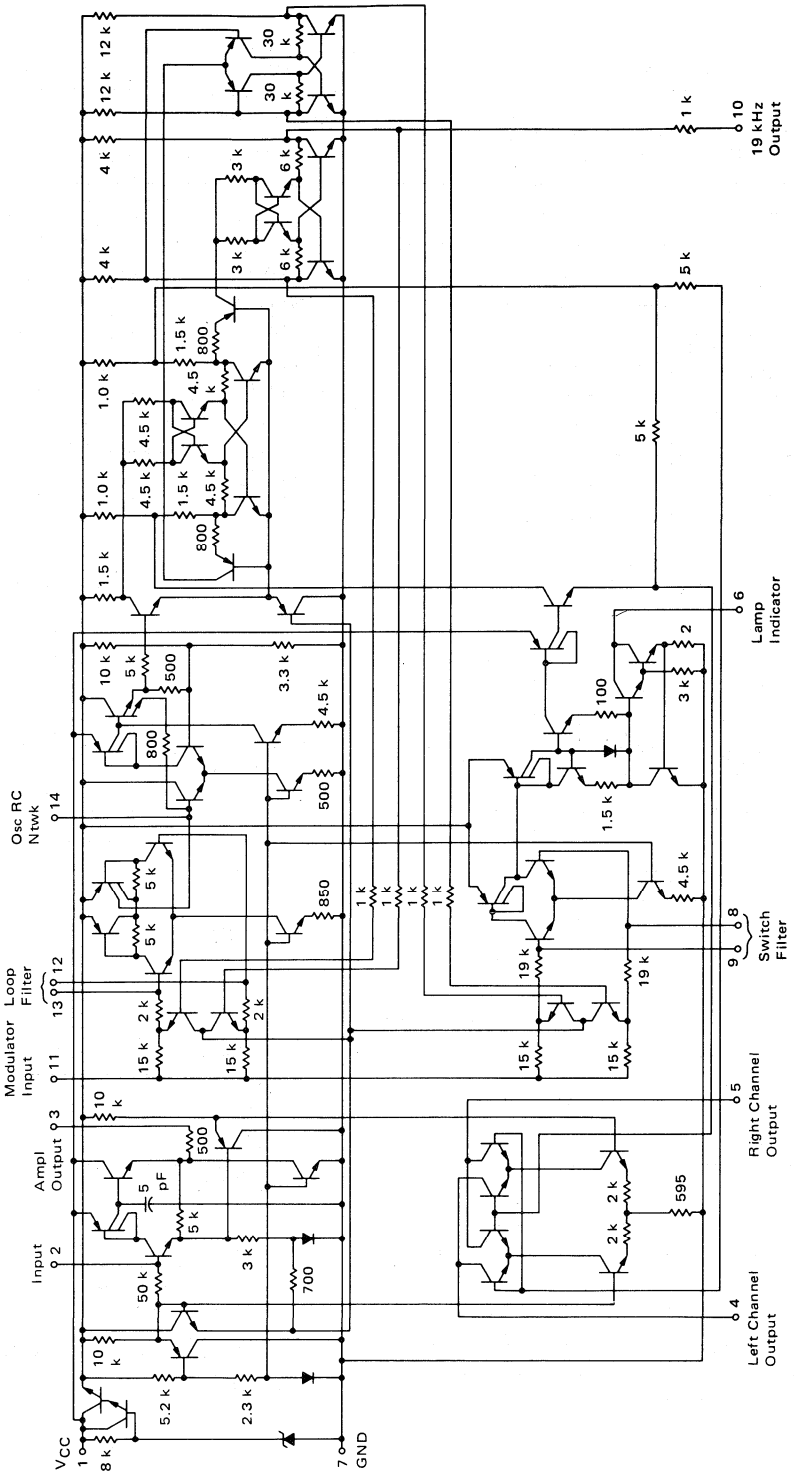


FIGURE 2 – CIRCUIT SCHEMATIC

TYPICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C; 560 mV(RMS) (2.8 $V_{[p-p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

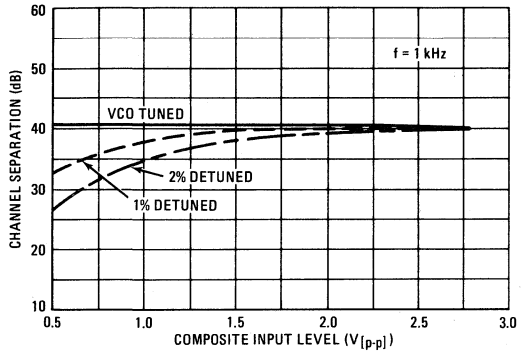


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

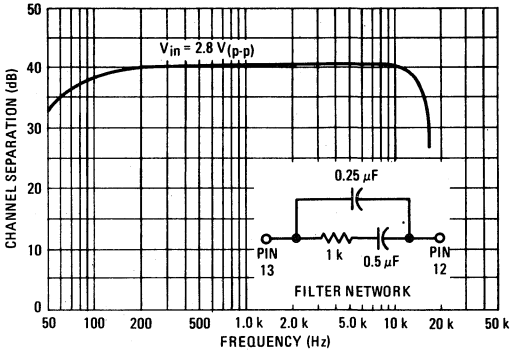


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE-RUNNING FREQUENCY

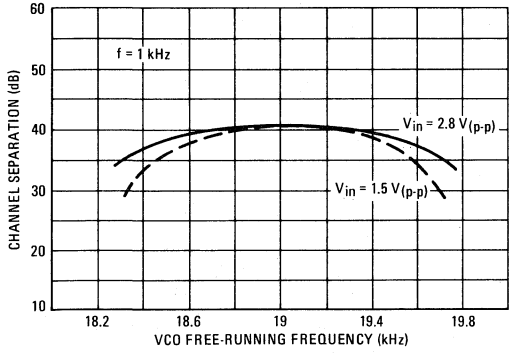


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

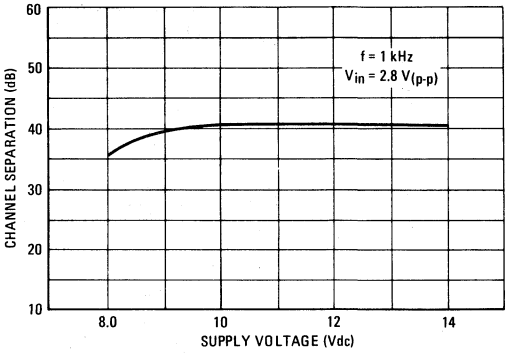


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL*

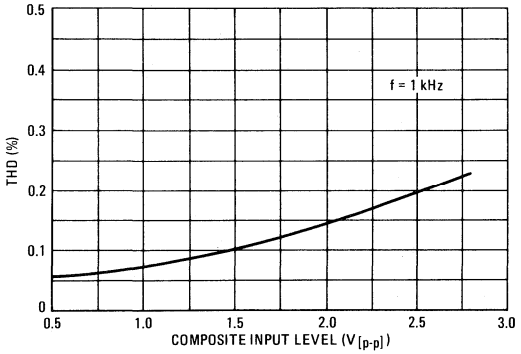
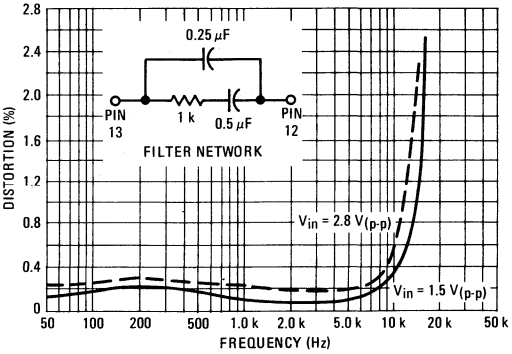


FIGURE 8 – DISTORTION versus FREQUENCY*



*Measured with Low Pass Filter (BW = 15 kHz).

9

FIGURE 9 – DISTORTION versus FREQUENCY*

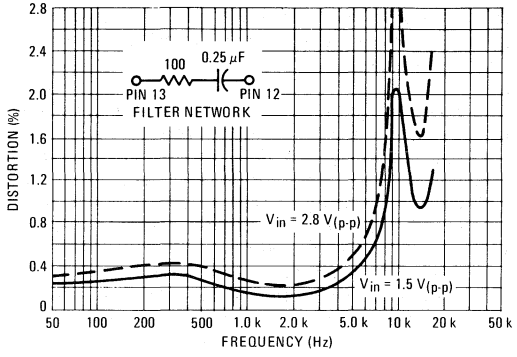


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

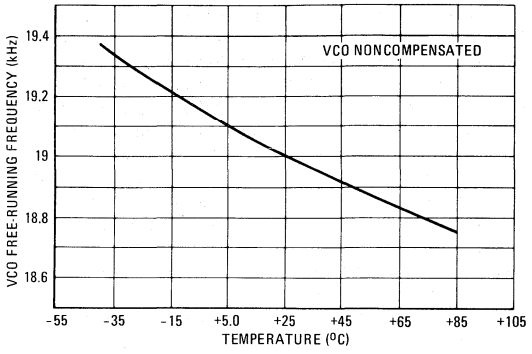
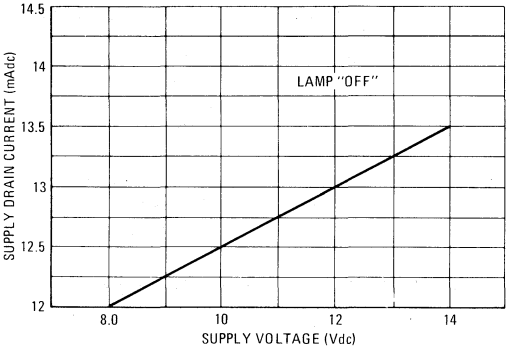


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY

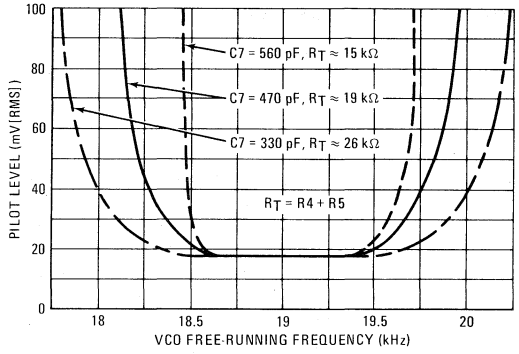
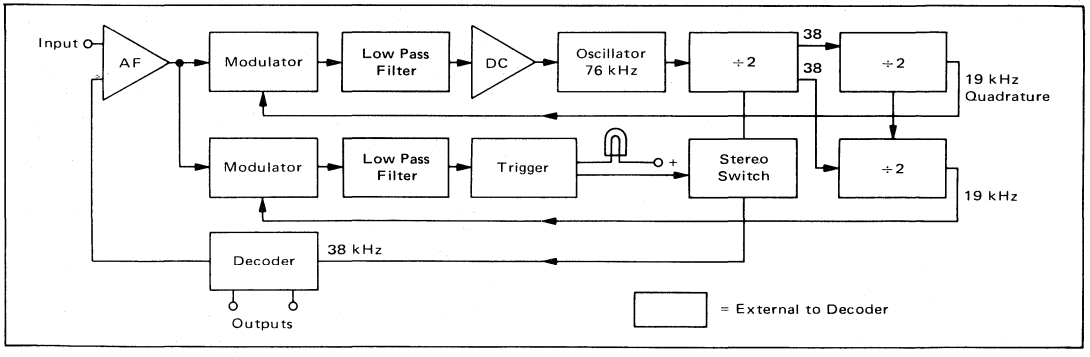


FIGURE 13 – SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

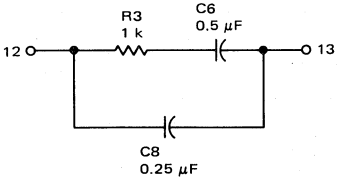
C1 — Input coupling capacitor; 2.0 μF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.

R1, R2, C2, C3 — See Maximum Load Resistance section.

C4 — Filter capacitor for stereo switch level detector; time constant is C4 x 53 kilohms ±30%, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.

C5 — See Phase Compensation section.

R3, C6, C8 — Phase-locked loop filter components; the following network is recommended:



When less performance is required a simpler network consisting of R3 = 100 ohms and C6 = 0.25 μF may be used (omit C8). See Figure 9.

R4, R5, C7 — Oscillator timing network; recommended values:

C7 = 470 pF	1%
R4 = 16 kΩ	1%
R5 = 5 kΩ	Preset

These values give ±3.5% typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.

Stereo Lamp — Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.

19-kHz Output — A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired. Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2^{o}. The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

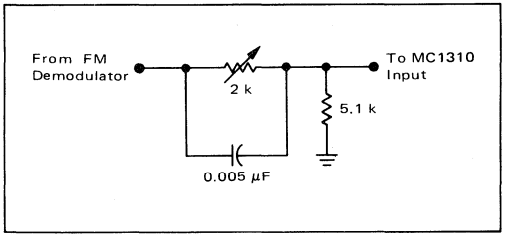
additional lead of 3.5° (for C5 = 0.05 μF) giving a total lead of 5.5°.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated subcarrier to lag the original. However, a 5.5° phase error if left noncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 – IF COMPENSATION NETWORK



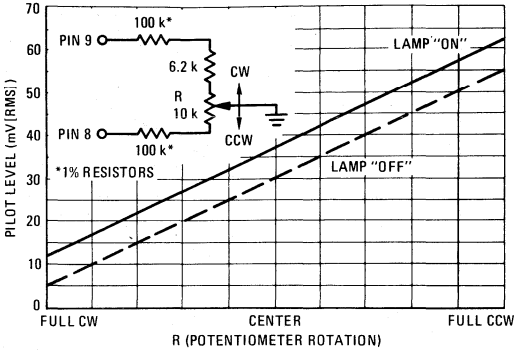
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM. This will hold the oscillator drift to approximately ±1% over a temperature range of -40 to +85°C. Allowing ±2% for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 – PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

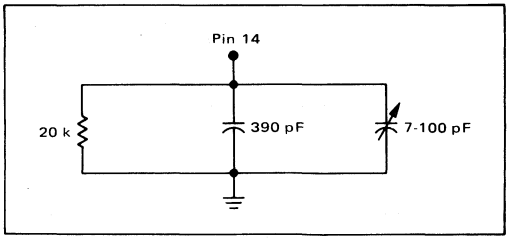
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM.

FIGURE 16

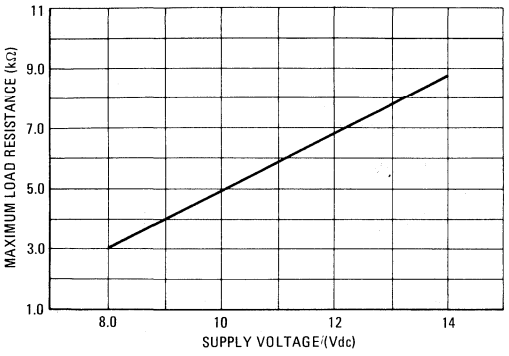


Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard 75 μs de-emphasis.

APPLICATIONS INFORMATION (continued)

FIGURE 17 – MAXIMUM LOAD RESISTANCE versus SUPPLY VOLTAGE



Audio Output

The ratio $G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}}$ for different types of input is as follows:

	INPUT	
	Single-Channel Composite Signal	Monaural Signal
	0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

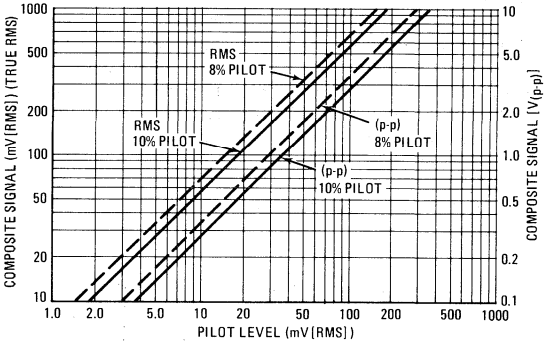
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

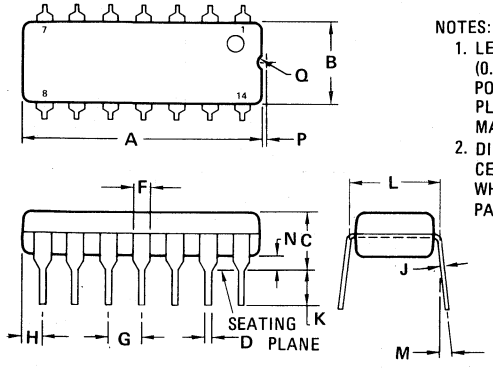
Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 – COMPOSITE LEVEL versus PILOT (L or R Modulation Only)



OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 646



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC1312P
MC1314P • MC1315P

FOUR CHANNEL SQ LOGIC DECODER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

CBS SQ* LOGIC DECODER SYSTEM

. . . a matrix system designed to decode SQ encoded program material into four separate channels. This system conforms to specifications for decoding quadraphonic records produced by the largest record companies in the world.

MC1312P - DECODER

. . . consists of two high input impedance preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-phase networks which generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left front, left back, right front, and right back signals (L_F', L_B', R_F', R_B').

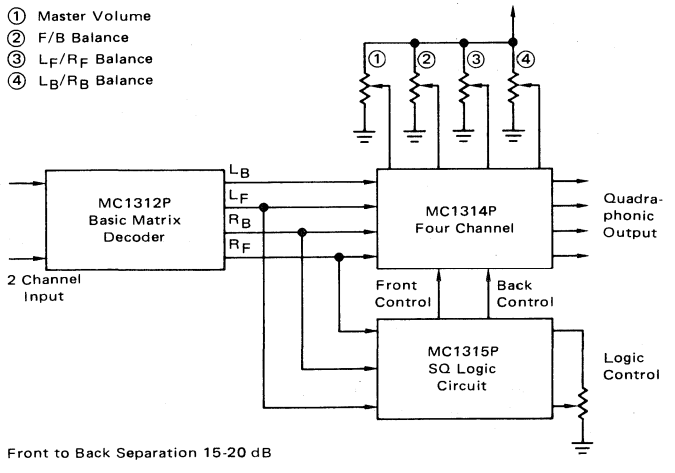
MC1314P - VOLTAGE CONTROLLED ATTENUATOR

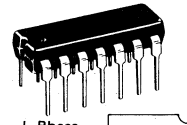
. . . a gain control and balance adjustment unit for use with any quadraphonic system. It has four channels whose gain can be varied by an external dc voltage. In addition, the relative gain between channels can be set by 3 external dc voltages. Thus with four variable resistors the master volume L_F/R_F, L_B/R_B and F/B balance may be controlled.

MC1315P - LOGIC CIRCUIT

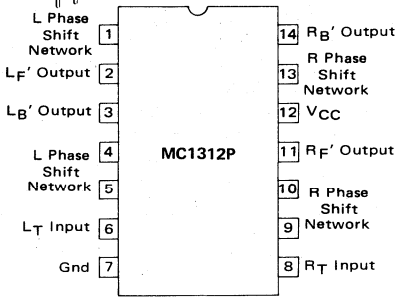
. . . provides the basic logic function to enhance the front to back separation in the CBS SQ four channel decoding system. This device is designed to interface with the MC1312 decoder and MC1314. The MC1315 provides dc logic enhancement control signals which extends the performance of the basic SQ system to the levels desired for top-of-the-line systems.

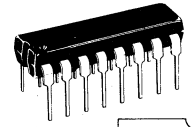
FIGURE 1 – SQ LOGIC DECODER SYSTEM



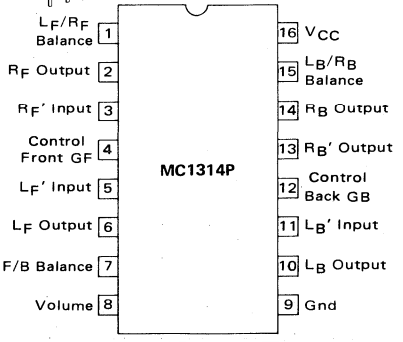


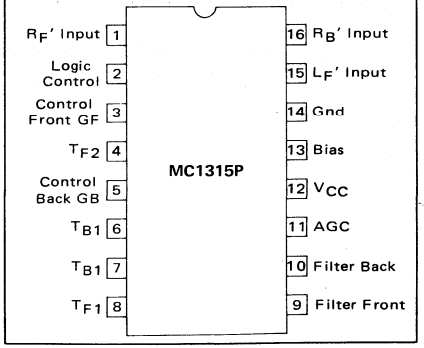
P SUFFIX
PLASTIC PACKAGE
CASE 646





P SUFFIX
PLASTIC PACKAGE
CASE 648





*Trademark of Columbia Broadcasting Systems, Inc.

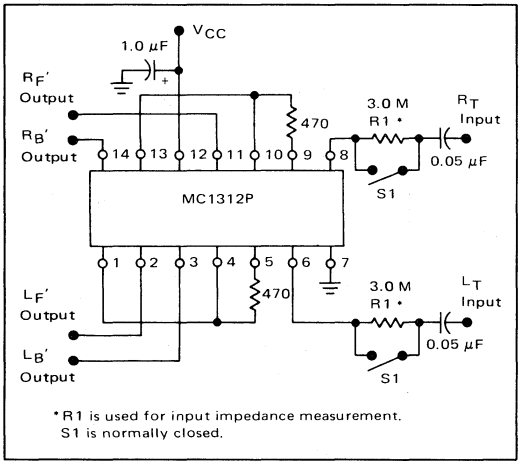
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	25	Vdc
Power Dissipation @ T_A = 25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, V_{in} = 0.5 V(RMS) @ 1 kHz, T_A = +25°C unless otherwise noted.)

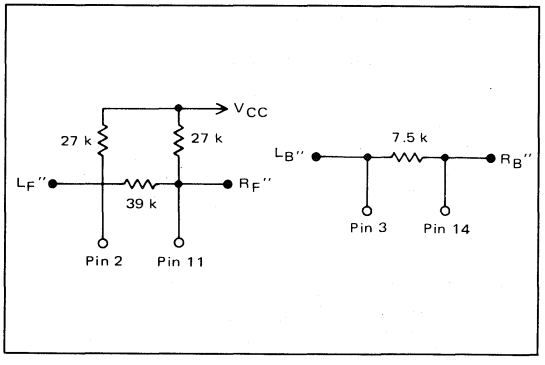
Characteristic	Min	Typ	Max	Unit
Supply Current Drain	11	16	21	mA
Input Impedance	1.8	3.0	–	MΩ
Output Impedance	–	5.0	–	kΩ
Channel Balance (L_F/R_F)	-1.0	0	+1.0	dB
Voltage Gain L_F/L_T or R_F/R_T	-1.0	0	+1.0	dB
Relative Voltage Gain L_B'/L_F', R_B'/L_F', L_B'/R_F', R_B'/R_F' L_F' measurements made with L_T input, R_F' measurements made with R_T input.	-2.0	-3.0	-4.0	dB
Maximum Input Voltage for 1%THD at Output R_T or L_T	2.0	–	–	V(RMS)
Total Harmonic Distortion R_T or L_T	–	0.1	–	%
Signal to Noise Ratio (Short-Circuit Input V_O = 0.5 V(RMS) with Output Noise Referenced to Output Voltage, V_O) (BW = 20 Hz to 20 kHz)	–	80	–	dB

FIGURE 2 – MC1312P TEST CIRCUIT



*R1 is used for input impedance measurement.
S1 is normally closed.

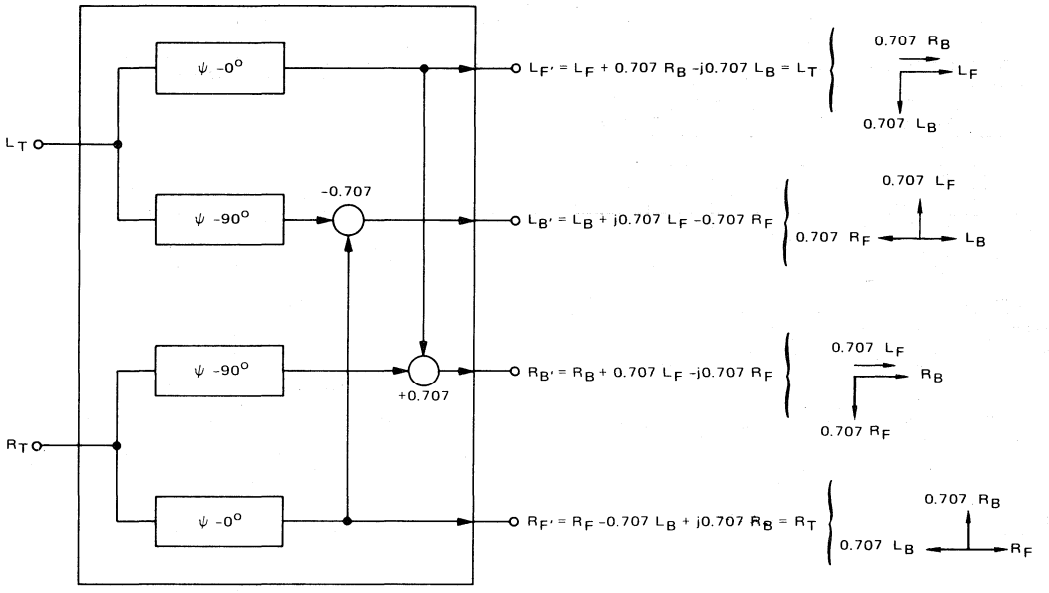
FIGURE 3 – EIA STANDARD BLEND



Note: In applications where tone arm pick-up is connected directly to the MC1312P inputs, a 300 k resistor should be inserted in series with R_T (Pin 8), and L_T (Pin 6) inputs.

APPLICATIONS INFORMATION

FIGURE 4 – DECODING PROCESS DIAGRAM



$L_T = L_F + 0.707\ R_B - j\ 0.707\ L_B$

$R_T = R_F - 0.707\ L_B + j\ 0.707\ R_B$

L_T and R_T are composite signals from SQ encoded records or SQ broadcast.

The decoding process is shown schematically in Figure 4. The MC1312P circuits that perform this function consists of two preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-pass* networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left-front, left-back, right-front, and right-back signals (L_F', L_B', R_F', R_B').

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100-Hz to 10-kHz bandwidth and a phase ripple of $\pm 8.5^o$ on a 90^o phase difference.

It is generally desirable to enhance center-front to center-back separation. This is accomplished by connecting a resistor between pins 2 and 11 (front outputs) and a resistor between pins 3 and 14 (back outputs). For a 10% front channel blending† and a 40% back channel blending†, 47 kilohms between pins 2 and 11 and 7.5 kilohms between pins 3 and 14 is required and results in the following equations:

†$R_F'' = 0.912\ L_T + 0.088\ R_T$

$L_F'' = 0.912\ R_T + 0.088\ L_T$

$R_B'' = \frac{\sqrt{2}}{2}\ [0.714\ (JR_T - L_T) + 0.286\ (R_T - JL_T)]$

$L_B'' = \frac{\sqrt{2}}{2}\ [0.714\ (JL_T - R_T) + 0.286\ (L_T - JR_T)]$

To meet the EIA matrix standards with 10/40 blend use the circuit of Figure 5, which results in the following equations:

$R_F'' = 0.772\ (0.995\ R_T + 0.0972\ L_T)$

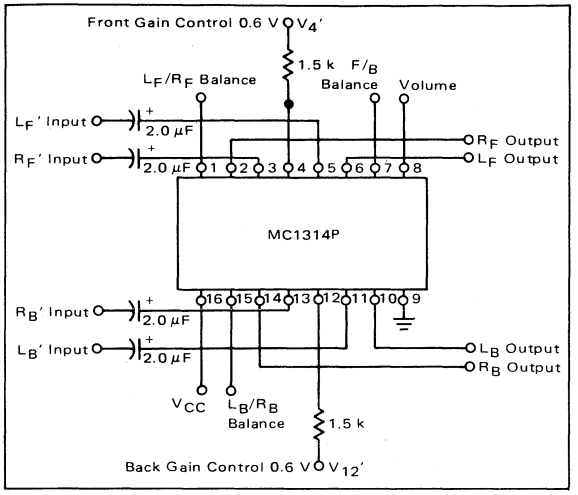
$L_F'' = 0.772\ (0.995\ L_T + 0.0972\ R_T)$

$R_B'' = \frac{\sqrt{2}}{2}\ (0.769)\ [0.928\ (JR_T - L_T) + 0.372\ (R_T - JL_T)]$

$L_B'' = \frac{\sqrt{2}}{2}\ (0.769)\ [0.928\ (JL_T - R_T) + 0.372\ (L_T - JR_T)]$

*An all-pass network produces phase shift without amplitude variations.

FIGURE 5 – MC1314P TEST CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	28	Vdc
Input Voltage Swing	±6.0	V_{pp}
Volume Control Range	-0.3 to +8.0	V
Balance Control Voltage	-4.0 to +10	V
Output Current Sinking (dc)	0	mA
Output Current Sourcing (dc)	1.0	mA
Power Dissipation @ T_A = +25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_4' = V_{12}' = 0.60 Vdc, T_A = +25°C, V_{IN} = 1.0 V(rms) @ 1.0 kHz, balance control pins open, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Maximum Gain (V_8 = 6 V)	-1.0	1.0	+3.0	dB
Minimum Gain (V_8 = 0 V)	-60	–	–	dB
Gain Spread @ Gain = Max @ Gain = -20 dB @ Gain = -40 dB	– – –	1.0 – –	3.0 3.0 3.0	dB dB dB
Signal Handling (THD < 1%)	1.3	–	–	Vrms
Signal Handling (V_4' = V_{12}' = 0.42 Vdc balance controls set for max gain in channel undertest) THD < 1%)	0.4	–	–	Vrms
Total Harmonic Distortion (V_{in} = 0.4 Vrms, max gain)	–	0.2	–	%
Signal/Noise Ratio (20 Hz - 15 kHz Bandwidth) Note 1. V_{IN} = 0.4 Vrms (ref)	–	80	–	dB
Channel Separation Note 2	–	60	–	dB
Balance Control Range – 20 dB gain V_8 = 6.0 V (≈Max Gain) V_8 = 3.0 V (≈ 6.0 dB Gain) V_8 = 1.0 V (≈ 20 dB Gain)	– 18 –	20 26 32	– – –	dB
Gain Enhancement (V_4' = V_{12}' = 0.42 Vdc compared to V_4' = V_8' = 0.60 Vdc)	2.0	–	4.0	dB
Gain Reduction (V_4' = V_{12}' = 1.86 Vdc compared to V_4' = V_{12}' = 0.60 Vdc)	7.0	–	11	dB
Gain Reduction (V_4' = V_{12}' = 3.12 Vdc compared to V_4' = V_{12}' = 0.60 Vdc, V_{CC} = 25 Vdc)	–	14	–	dB
Supply Current (max gain) (V_{IN} = 0 V) (min gain) (V_{IN} > 0 V)	– –	19 9.0	25 15	mA mA
Input Impedance	–	13	–	kΩ
Output Impedance	–	2.0	–	kΩ
Control Current I_4 or I_{12}	–	-20	–	μA
Balance Control Reference Voltage (relative to V_{CC}) L_F/R_F & L_B/R_B Controls (V_{1q}/V_{CC} & V_{15q}/V_{CC}) F/B Control (V_{7q}/V_{CC})	– –	15 13	– –	% %
Intermodulation Distortion (f_1 = 7 kHz, f_2 = 60 Hz)	–	0.6	–	%

Note 1: All Inputs ac shorted
Note 2: Input to 3-Channels driven, 4th Channel open.

FIGURE 6 – ATTENUATION versus CONTROL VOLTAGE

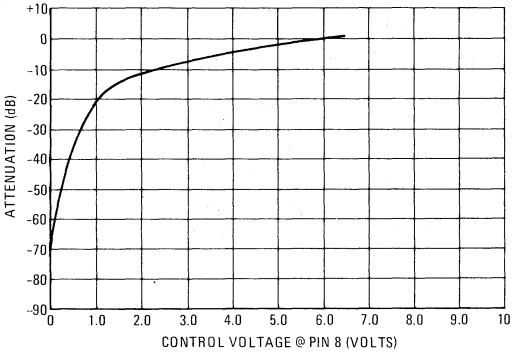
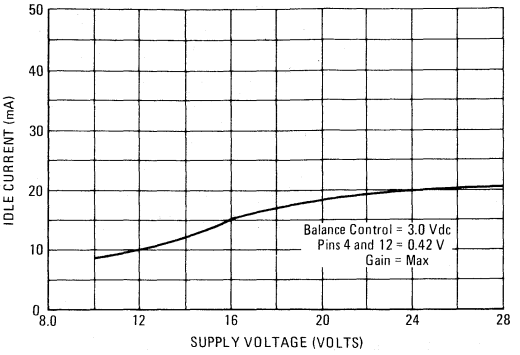


FIGURE 7 – IDLE CURRENT versus SUPPLY VOLTAGE



DISTORTION CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus ATTENUATION

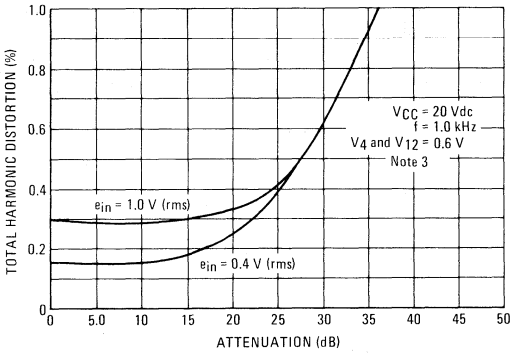


FIGURE 9 – INTERMODULATION DISTORTION versus INPUT VOLTAGE

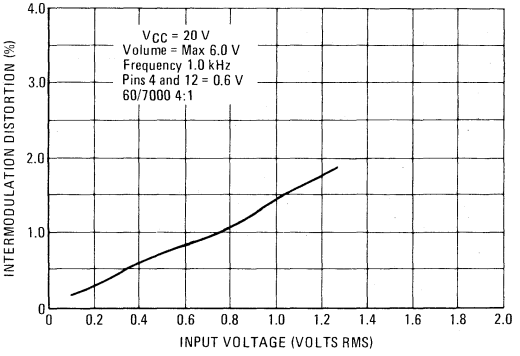


FIGURE 10 – TOTAL HARMONIC DISTORTION versus INPUT VOLTAGE

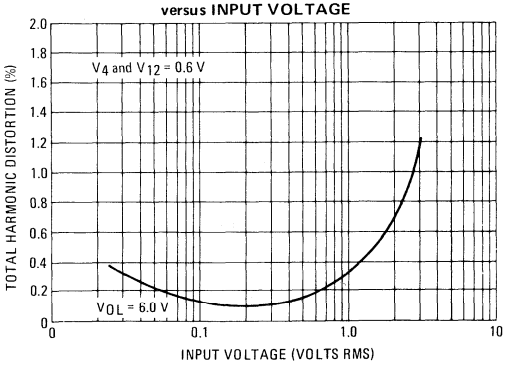
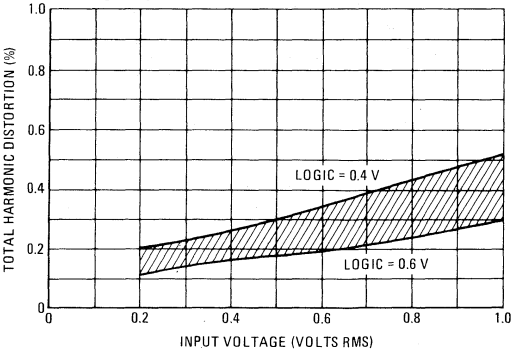


FIGURE 11 – LOGIC VOLTAGE EFFECTS ON TOTAL HARMONIC DISTORTION



Note 3: Major component of THD beyond 20 dB attenuation is noise.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Voltage (Note 1)	25	V
Input Signal Voltage	±4.0	Vpk
Bias Terminal Current	±2.0	mA
Output Current	±2.0	mA
Power Dissipation @ T_A = 25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 20 Vdc, Logic Control = 50%, V_{IN} = 0.5 Vrms, f = 2.0 kHz, unless otherwise noted, Note 1, Figure 12.)

Characteristic	Min	Typ	Max	Unit
Supply Current (Pin 12) @ V_{IN} = 0 @ V_{IN} = 1.4 Vrms	– –	7.0 15	13 –	mA mA
Input Resistance @ Pin 1, 15, 16	–	20	–	kΩ
Output Resistance @ Pin 3, 5	–	1.5	–	kΩ
Paraphase Filter Resistance @ Pin 9, 10	–	4.0	–	kΩ
Front-Back Logic Discharge Resistance @ Pin 7, 8	–	5.0	–	kΩ
Bias Voltage (10 k to ground) @ Pin 13	–	1.4	–	Vdc
Logic Control Input Current @ Pin 2 (V_2 = V_{13} or V_2 = 0)	–	±0.5	–	mA
Quiescent Input Voltage (V_{IN} = 0) @ Pin 1, 15, 16	–	7.0	–	Vdc
Quiescent Output Voltage (V_{IN} = 0)	0.48	–	0.72	Vdc
Quiescent Output Offset (V_{IN} = 0)	–	±0.02	±0.1	Vdc
Relative Output Change Front output with L_B or R_B inputs or back output with L_F or R_F inputs Back output with C_F input Front output with L_F, C_F or R_F inputs or back output with L_B, or R_B input	 2.1 7.5 1.9 5.5 0.8 2.2	 2.8 9.0 2.5 8.0 0.67 3.5	 5.0 14 3.5 11 0.56 5.0	 V/V dB V/V dB V/V dB
AGC Leveling - V_{IN} = 1.4 Vrms to V_{IN} = 50 mVrms (Note 2) Figure 8 (AGC1, AGC2)	–	1.0	3.0	dB
Quiescent Output Voltage at Max Logic (S_1 in Position 1, Figure 12) (V_{IN} = 0, V_2 = V_{13})	0.45	–	0.83	Vdc
Max Logic Relative Output Change (V_2 = V_{13}) Front output with L_B or R_B inputs or back outputs with L_F, C_F or R_F inputs Front output with L_F, C_F or R_F inputs or back outputs with L_B or R_B inputs	 – – – –	 5.0 14 0.67 3.5	 – – – –	 V/V dB V/V dB

Note 1: When testing with well regulated supplies, current should be limited to 25 mA.

Note 2: For example, this is the decrease in the back control voltage, V_5 with a right front input signal as this signal is varied from 1.4 Vrms to 50 mVrms.

FIGURE 12 – MC1315P TEST CIRCUIT

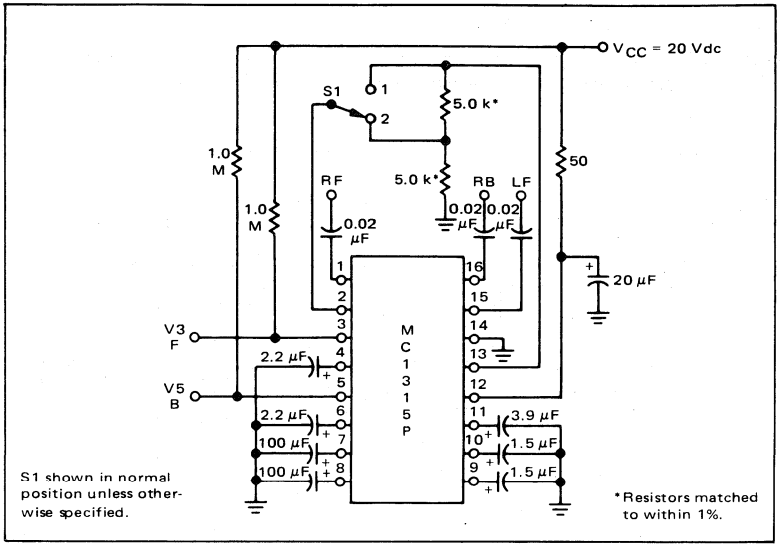


TABLE 1 – DEFINITION OF INPUT SIGNALS: (f = 2.0 kHz)

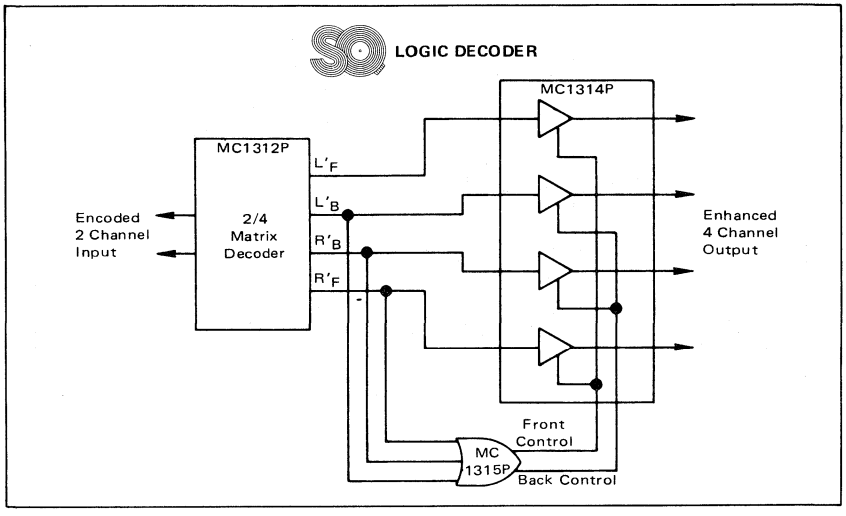
V_I Name	Signal Description	Apply To Pin	V_I Name	Signal Description	Apply To Pin
RF	0.5 V rms /0°	1	CF	0.35 V rms /0°	1
	0.35 V rms /-90°	16		0.35 V rms /-45°	16
	(1)	15		0.35 V rms /0°	15
LF	(1)	1			
	0.35 V rms /0°	16			
	0.5 V rms /0°	15			
LB	0.35 V rms /180°	1	AGC1	(1)	15
	(1)	16		1.0 V rms /-90°	16
	0.35 V rms /-90°	15		1.4 V rms /0°	1
RB	0.35 V rms /90°	1	AGC2	(1)	15
	0.5 V rms /0°	16		35 mV rms /-90°	16
	0.35 V rms /0°	15		50 mV rms /0°	1

(1) All unused inputs shall be ac grounded.
(2) This signal not used at present.

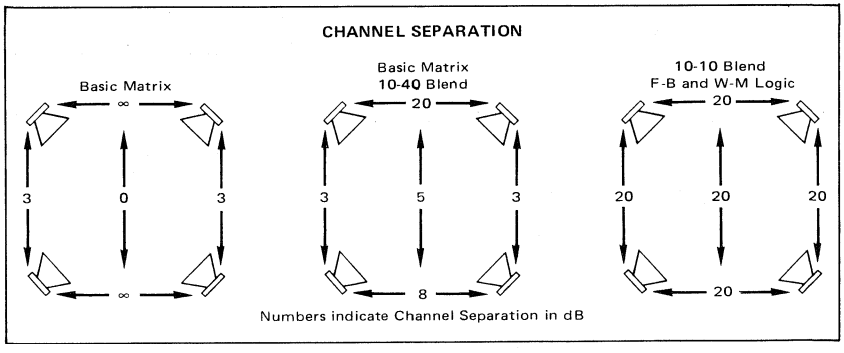
WHY LOGIC?

Enhances front to back separation from 6 dB to 20 dB.

Front-to-back separation of SQ material can be enhanced by the MC1315 logic circuit which detects the presence of dominant front or back signals and adjusts the front-back gain relationship of the MC1314P to enhance the relative gain of the dominant channels.



Front and back control voltages (from the MC1315P) are connected to the MC1314P. Although the relative gains of the front and back channels are altered with these control signals, they vary in a complementary manner to maintain constant power output from the MC1314P.



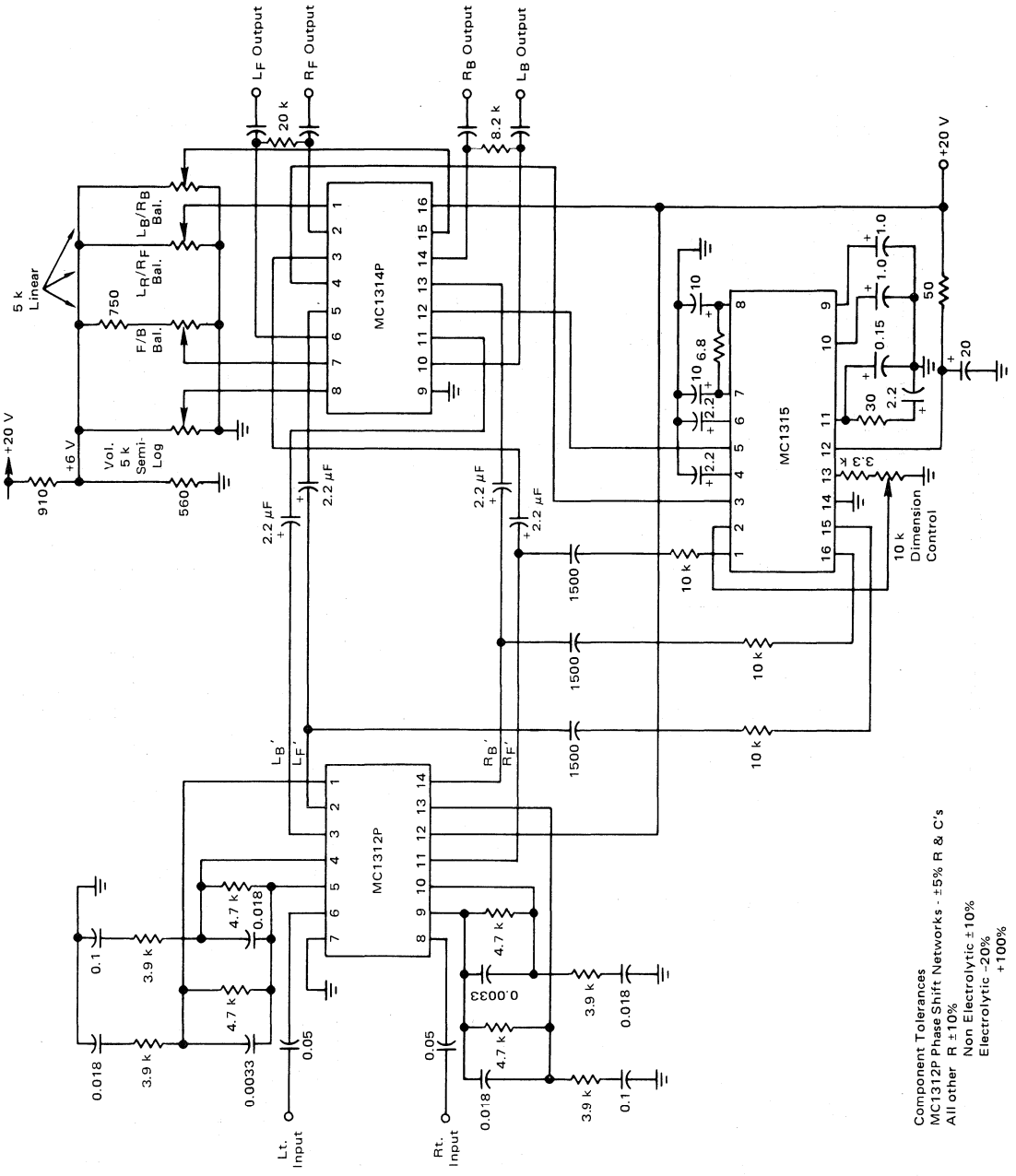
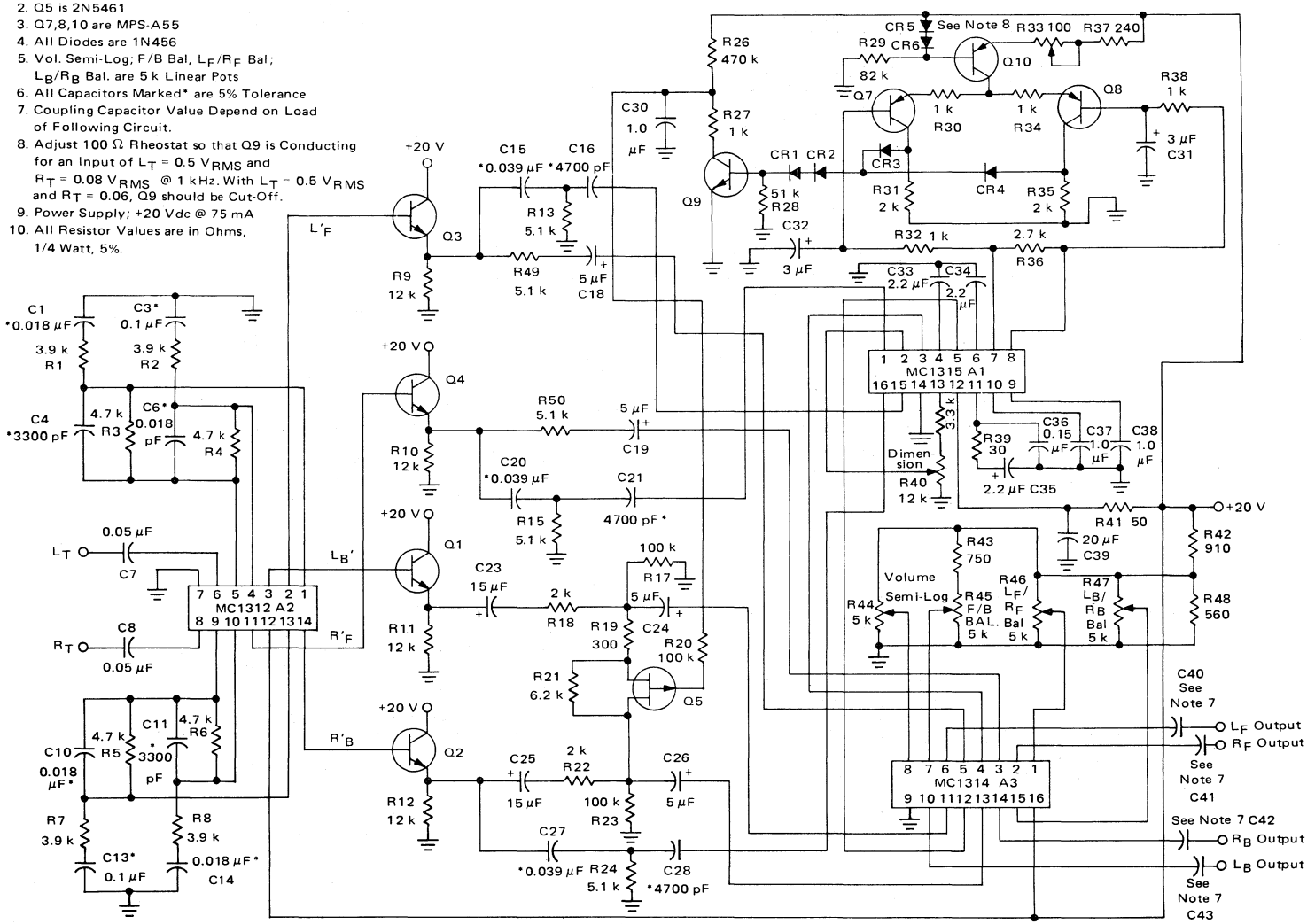


FIGURE 13 – CBS SQ LOGIC SYSTEM (L1a)

NOTES: (Unless otherwise specified)

1. Q1,2,3,4,9 are MPS-A18
2. Q5 is 2N5461
3. Q7,8,10 are MPS-A55
4. All Diodes are 1N456
5. Vol. Semi-Log; F/B Bal, L_F/R_F Bal; L_B/R_B Bal. are 5 k Linear Pots
6. All Capacitors Marked* are 5% Tolerance
7. Coupling Capacitor Value Depend on Load of Following Circuit.
8. Adjust 100 Ω Rheostat so that Q9 is Conducting for an Input of L_T = 0.5 V_{RMS} and R_T = 0.08 V_{RMS} @ 1 kHz. With L_T = 0.5 V_{RMS} and R_T = 0.06, Q9 should be Cut-Off.
9. Power Supply; +20 Vdc @ 75 mA
10. All Resistor Values are in Ohms, 1/4 Watt, 5%.

FIGURE 14 – CBS LOGIC SYSTEM WITH VARIABLE BLEND (L2a)



TYPICAL SYSTEM PERFORMANCE CHARACTERISTICS (MC1312P, MC1314P, MC1315P)

Power Supply Requirements:	60 mA at 20 V
Nominal Signal Level:	0.5 V
Maximum Input Voltage:	1.9 V
Input Impedance:	2 MΩ
Output Impedance:	2 kΩ
Total Harmonic Distortion:	0.2% at nominal input
at 1 Hz	1.0% at maximum input
Voltage Gain (at quiescent):	1.0
4 Channel Volume Control	Range - 70 dB
	Tracking - within 3 dB
4 Channel Balance Control:	-35 dB at -20 dB gain

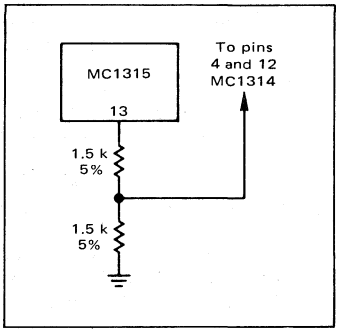
NOTES

MC1314P

1. If volume control is not used, connect Pin 8 to +6.0 V.
2. If balance controls are not used, open Pins 1, 7 and 15.
3. L_F/R_F and L_B/R_B balance controls can be ganged by connecting Pins 1 and 15.
4. Signal handling capability is reduced at maximum logic (20 dB front to back separation) unless V_{CC} = 25 V on MC1314.

MC1315P

1. The logic control will provide enhancement of front to back separation from 6 dB typical to 20 dB max (15 dB typical at the recommended operating level of 50% control).
2. To defeat the logic use the circuit connections as shown on right.



SYSTEM CHARACTERISTICS

FIGURE 15 – GAIN versus F/B BALANCE

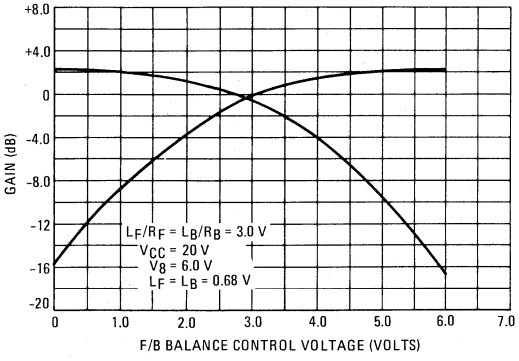
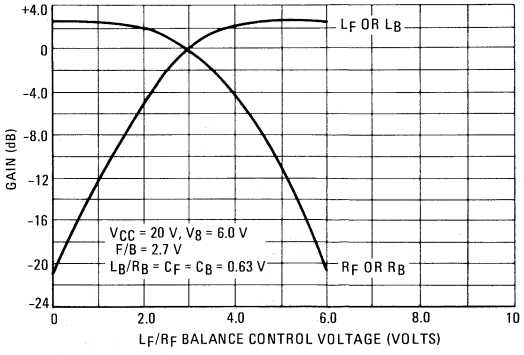


FIGURE 16 – GAIN versus L_F/R_F BALANCE CONTROL



Signal Definitions for Total System

Test signals shall have the following relative phase and amplitude characteristics.

Source Location	Input Signals	
	L_T	R_T
L_F	1	0
C_F	.71	.71
R_F	0	1
L_B	$.71/-90^o$	$.71/180^o$
R_B	.71	$.71/90^o$

Where L_F is left front, R_B is right back, C_F is center front, etc.

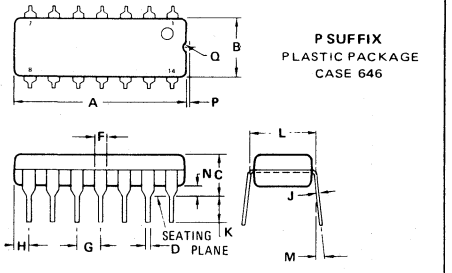
1. System Tests: MC1312P, MC1314P, MC1315P
   a) L_F source - connect signal to L_T input, ac ground R_T input of MC1312P.
   b) R_F source - apply signal to R_T, ac ground L_T.
   c) C_F source - apply equal signals to L_T and R_T inputs.

   NOTES: Balance control inputs of MC1314 may be opened for convenience or set for perfect balance with C_F and C_B inputs; set logic control to 50%: Max signal should be limited to 1.6 Vrms L_T or R_T: MC1314P outputs give system performance, typically 15 dB front back separation for corners, 12 dB for center front, center back.

2. Logic Circuit Tests: MC1315P
   a) L_F source - apply $L_F' = \sqrt{2}\ R_B'$, $R_F' = 0$; dc voltage at Pin 3 should decrease by 3 dB, at Pin 5 should increase by 9 dB.
   b) R_B source - apply $R_F' = \sqrt{2}\ R_B'$, $R_F' = 0$; dc voltage at Pin 3 should increase by 9 dB, at Pin 5 should decrease by 3 dB.

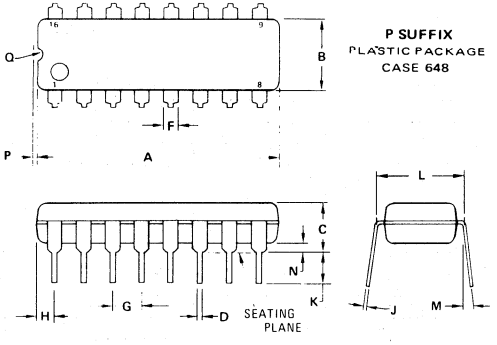
3. Voltage Controlled Amplifier Tests: MC1314P
   a) Volume control - with balance controls open or balanced, gain should be +0.5 dB at 6 V on Pin 8 and less than -60 dB at 0 V.
   b) Balance controls - with balance controls at Pins 1 and 15 at 15% of supply and Pin 7 at 13% of supply, system is nominally balanced. Taking Pin 1 to ground should increase L_F gain by 3 dB and decrease R_F gain by greater than 12 dB at maximum volume and 30 dB at lower volume levels.

OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

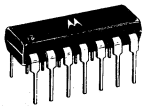
. . . a monolithic device designed for use in solid-state color television receivers.

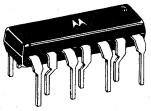
- Good Chroma Sensitivity — 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage — 0.6 V Maximum
- Differential DC Temperature Stability — 0.7 mV/°C
- High Blue Output Voltage Swing — 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

DUAL DOUBLY BALANCED CHROMA DEMODULATOR with RGB OUTPUT MATRIX AND PAL SWITCH

MONOLITHIC SILICON INTEGRATED CIRCUIT

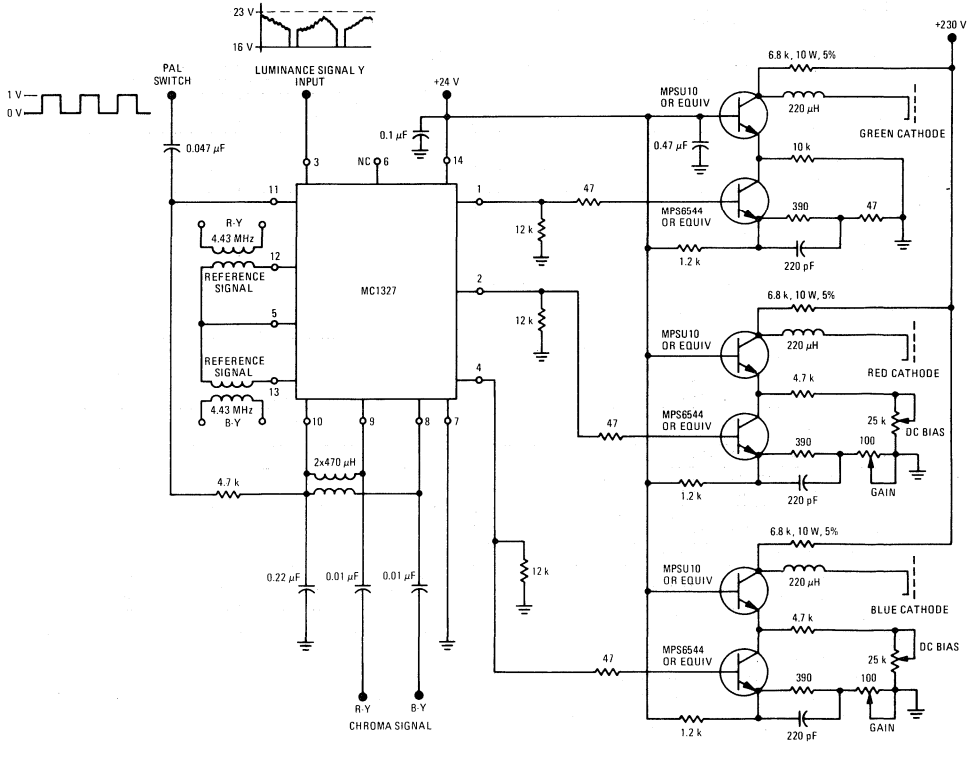
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116





PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}* = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

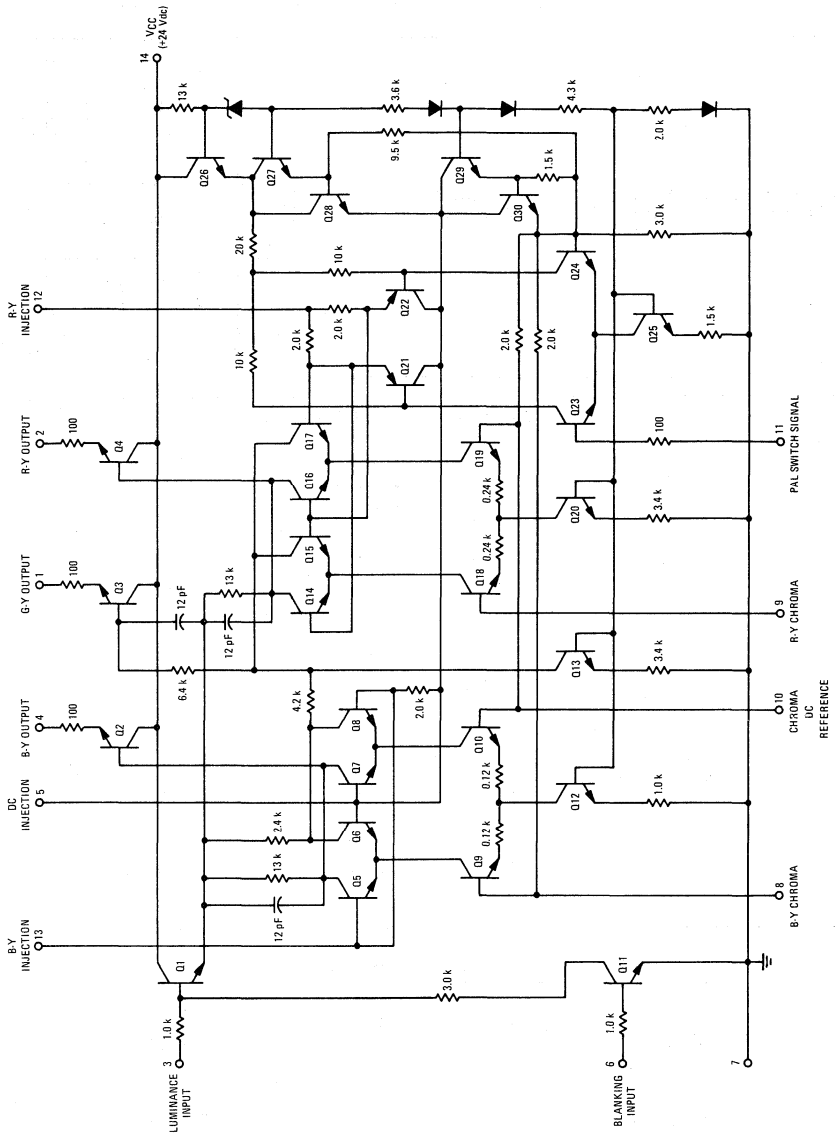
Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage (See Figure 2)	1,2,4	13.2	14.5	15.8	Vdc
Quiescent Input Current from Supply (Figure 2) (R_L = ∞) (R_L = 3.3 k ohms)		 – 16	 7.5 19	 – 26	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (See Note 1 and Figure 2)	1,2,4	–	0.3	0.6	Vdc
Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	0.7	–	mV/°C
Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	+0.5	±5.0	mV/°C
DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)					
Blue Output Voltage Swing (See Note 2 and Figure 3)	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) (See Note 3 and Figure 3)	8	–	280	550	mVp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz, reference at 100 kHz)	1,2,4	 – –	 0.95 -1.8	 – –	– dB
Differential Luminance Gain, RGB Outputs (@ 5.0 MHz)		–	0.3	–	dB
Blanking Input Resistance (1.0 Vdc) (0 Vdc)	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) (See Note 4) G Output R Output	4 1 2	 1.4 2.5	 1.8 2.9	 2.2 3.3	Vp-p
PAL Switch Operating Voltage Range (7.8 kHz Square Wave)	11	0.3	–	3.0	Vp-p
R-Y Output dc Offset with PAL Switch Operation		–	–	100	mVdc
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	200	300	mVp-p
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1,2,4	–	0.6	1.0	Vp-p
Reference Input Resistance (Chroma Input = 0)	12,13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12,13	–	6.0	–	pF
Chroma Input Resistance	8,9,10	–	2.0	–	kΩ
Chroma Input Capacitance	8,9,10	–	2.0	–	pF

NOTES:

1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p.
4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC1327 CHROMA DEMODULATOR (PAL)



TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 kilohms, T_A = +25°C unless otherwise noted)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

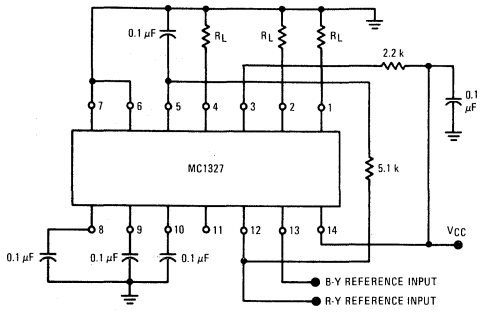
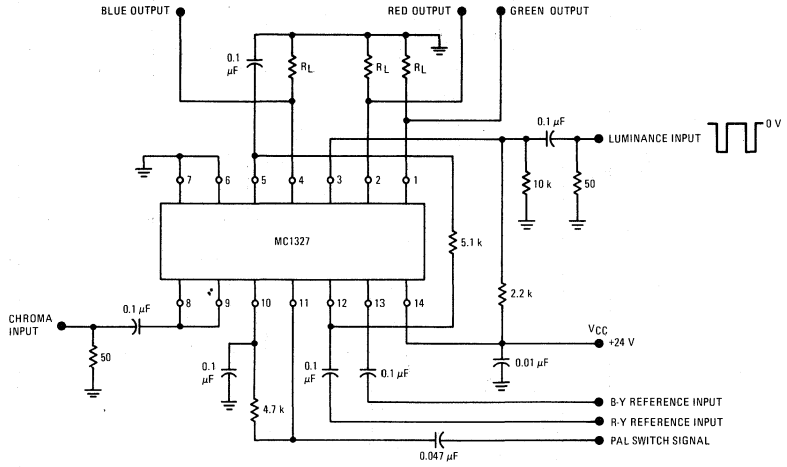
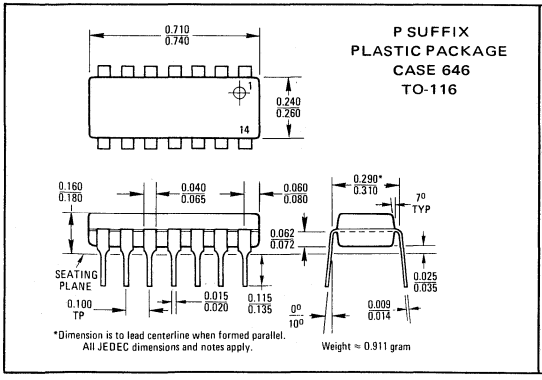
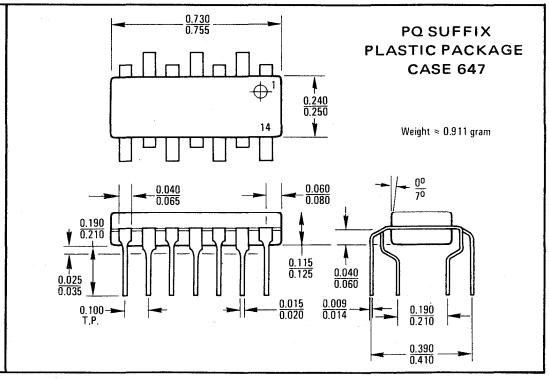


FIGURE 3 – DYNAMIC TEST CIRCUIT



OUTLINE DIMENSIONS





ADVANCE INFORMATION

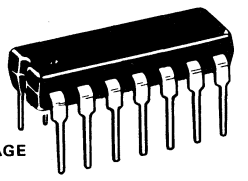
DUAL DOUBLE BALANCED CHROMINANCE DEMODULATOR WITH RBG MATRIX AND PAL SWITCH

. . . a monolithic device designed for use in PAL colour television decoders.

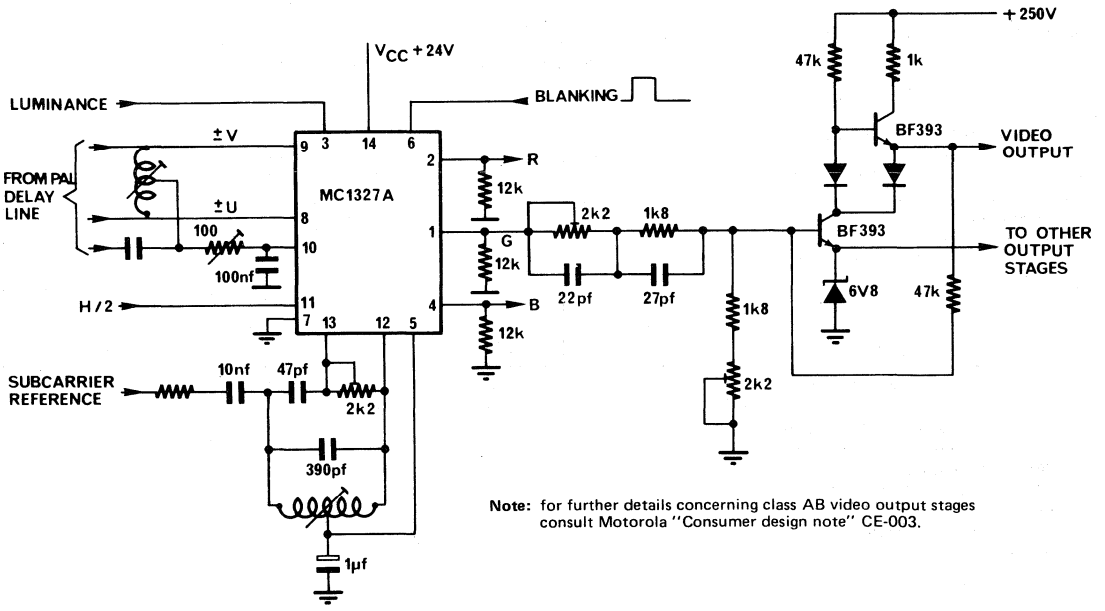
- Good chrominance sensitivity 0.22 V p-p Input typical for 5 V p-p Output
- Differential DC Temperature Stability 0.5 mV/°C typ.
- High B-Y Output Voltage Swing 10 V p-p
- Blanking Input Provided
- Luminance Bandwidth greater than 5 MHz.

CHROMINANCE DEMODULATOR WITH RBG OUTPUT MATRIX AND PAL SWITCH

MONOLITHIC SILICON
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



Note: for further details concerning class AB video output stages consult Motorola "Consumer design note" CE-003.

FIGURE 1 – TYPICAL APPLICATION CIRCUIT

MAXIMUM RATINGS (T_A = +25 °C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chrominance Signal Input Voltage	5.0	VpK
Reference Signal Input Voltage	5.0	VpK
Minimum load resistance	3.0	K
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation Derate above 25 °C	1000 8	mW mW/°C
Operating Temperature Range (Ambient)	−20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, RL = 3K3, T_A = 25 °C, 4.43 MHz reference input 1 Vp-p (unless otherwise stated)

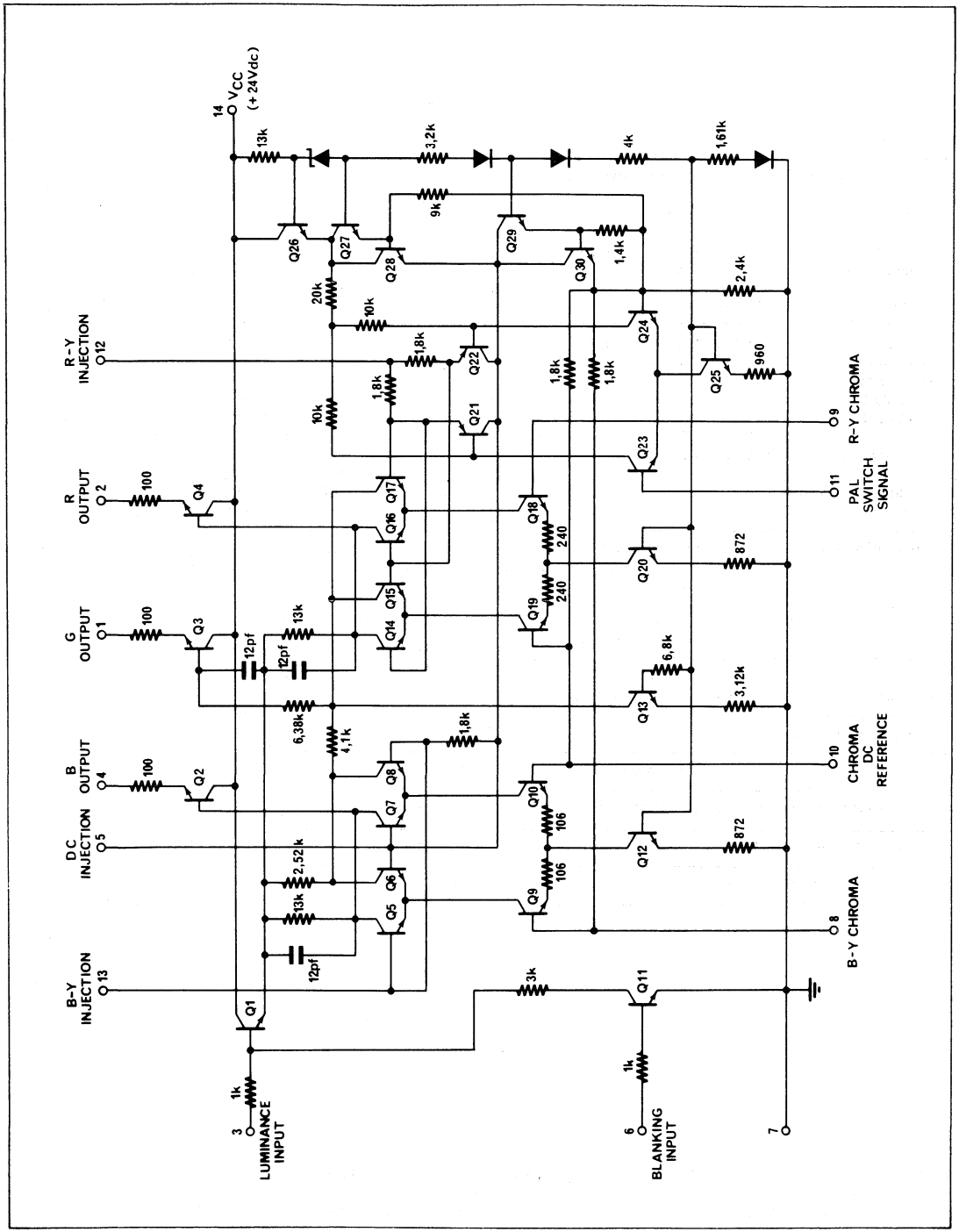
STATIC CHARACTERISTICS

Characteristic	Pin No.	Min.	Typ.	Max.	Unit
Quiescent Output Voltage	1, 2, 4	13.2	14.7	15.8	Vdc
Quiescent Input Current from Supply (Fig. 2) $R_L = \infty$ R_L = 3K3	14	 16	 7.5 19	 26	 mAdc mAdc
Reference Input dc Voltage (Fig. 2)	5, 12, 13		6.2		Vdc
Chrominance Input dc Voltage (Fig. 2)	8, 9, 10		3.4		Vdc
Differential Output Voltage (Fig. 2) (see note 1)	1, 2, 4		0	0.6	Vdc
Differential Output Voltage Temperature Coefficient +25 °C to +65 °C. (See note 1) (Fig. 2)	1, 2, 4		0.5	1.5	mV/°C
Output Voltage Temperature Coefficient (see note 1) (Fig. 2)	1, 2, 4		−4		mV/°C

DYNAMIC CHARACTERISTICS

Characteristic	Pin No.	Min.	Typ.	Max.	Unit
Blue Output Voltage Swing (see note 2) (Fig. 3)	4	8	10		Vp-p
Chrominance Input Voltage at Blue Output = Vp-p (see note 3) (Fig. 3)	8	150	220	350	mVp-p
Luminance Input Resistance	3	100			KΩ
Luminance Gain from pin 3 to Outputs @ dc @ 5.0 MHz referred to 100 KHz	1, 2, 4	0.95	 −1.8		 db
Differential Luminance Gain RGB Outputs at 5 MHz	1, 2, 4		0.3		db
Blanking Input Resistance (1 Vdc) (0 Vdc)	6		 1.1 75		 KΩ KΩ
Ratio of colour matrices (see note 3) (Fig. 3) B:R (no-b-y input) R:G (no r-y input) B:G	 4.2 2.1 4.1	 1.50 1.76 4.64	 1.78 1.96 5.15	 1.96 2.16 5.67	
PAL Switch Operating Voltage 7.8 KHz square wave	11	0.3			Vp-p
Red Output Offset with PAL switch Operation 7.8 KHz square wave	2			100	mVp-p
Demodulator Unbalance 4.43 MHz residual carrier (normal 4.43 MHz reference signal with no chrominance input)	1, 2, 4		100	200	mVp-p
Residual 4.43 MHz plus harmonics ourput voltage (with 4.43 MHz reference and chrominance input such that B out = 5 Vp-p	1, 2, 4		0.6	1.0	Vp-p
Reference input resistance chrominance input = 0	12, 13		2		KΩ
Reference input capacitance chrominance input = 0	12, 13		6		pF
Chrominance input resistance	8, 9, 10		2		KΩ
Chrominance input capacitance	8, 9, 10		2		pF

Note:
1. Chrominance input signal voltage = 0 and normal reference input voltage = 1 Vp-p 4.43 MHz.
2. With normal reference input signal voltage adjust chrominance input signal voltage to 1.2 Vp-p.
3. With normal reference signal voltage adjust chrominance input signal voltage until the blue output voltage = 5 Vp-p.


14 VCC (+24Vdc)
13k
3,2k
4k
1,61k
9k
Q26
Q27
Q28
Q29
Q30
1,4k
2,4k
20k
10k
R-Y INJECTION 12
1,8k
Q22
Q24
Q25
960
1,8k
1,8k
1,8k
10k
Q21
Q23
9 R-Y CHROMA
R OUTPUT 2
100
Q4
Q17
Q16
Q18
240
11 PAL SWITCH SIGNAL
872
Q20
G OUTPUT 1
100
Q3
12pf
13k
Q15
Q14
Q19
240
12pf
6,8k
3,12k
Q13
6,38k
4,1k
1,8k
B OUTPUT 4
100
Q2
Q8
Q7
Q10
106
10 CHROMA DC REFERENCE
DC INJECTION 5
872
Q12
2,52k
Q6
Q9
106
13k
Q5
8 B-Y CHROMA
12pf
B-Y INJECTION 13
3k
Q1
Q11
1k
3 LUMINANCE INPUT
1k
6 BLANKING INPUT
7

TEST CIRCUITS

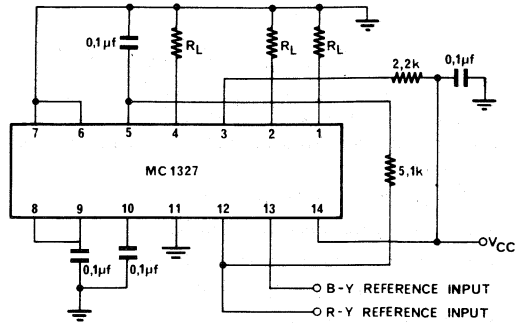


FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

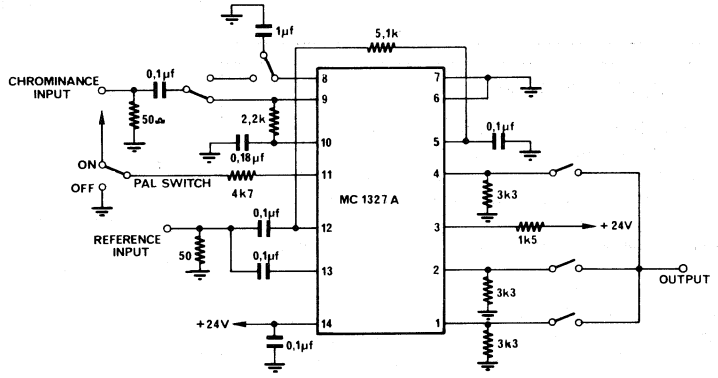
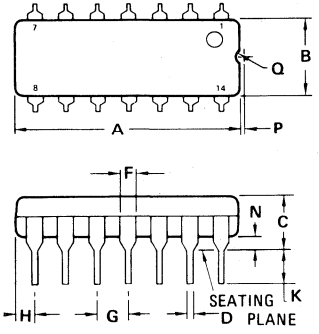


FIGURE 3 – DYNAMIC TEST CIRCUIT

OUTLINE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 646

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC1330A1P
MC1330A2P

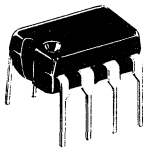
LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

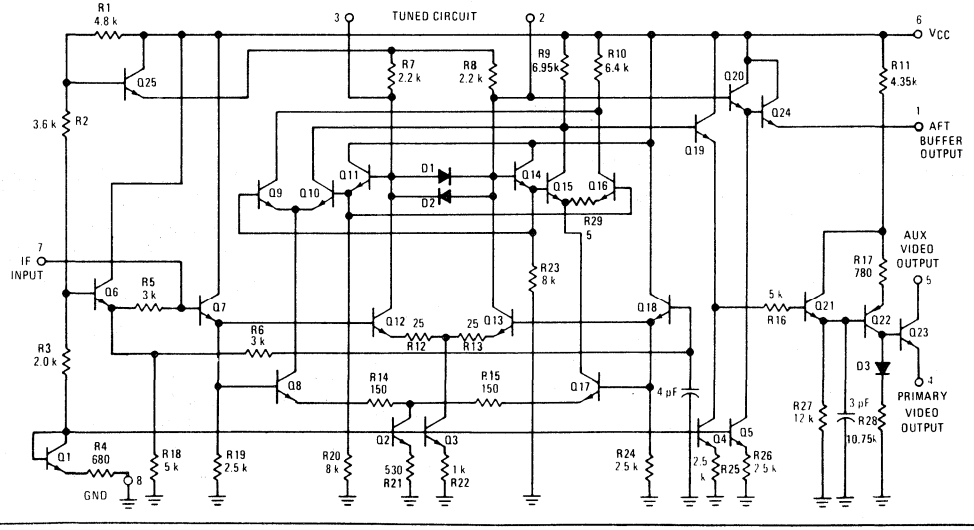
The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

OUTPUT VOLTAGE SELECTION

The MC1330A1P is identical to the MC1330A2P with the following exception:

	ZERO SIGNAL DC OUTPUT VOLTAGE
MC1330A1P	7.0 to 8.2 Vdc
MC1330A2P	7.8 to 9.0 Vdc

FIGURE 1 – CIRCUIT SCHEMATIC



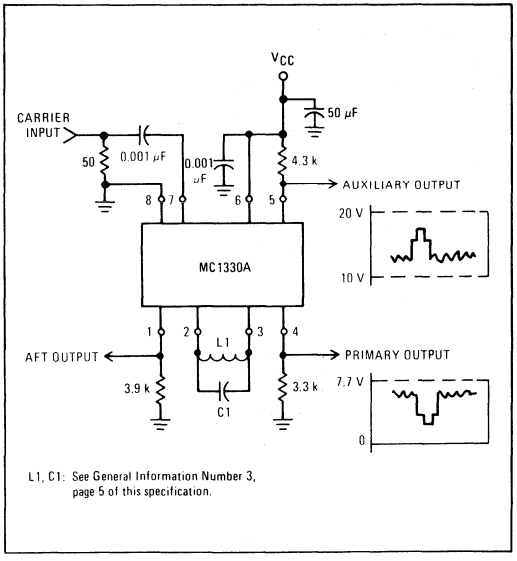
MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, fc = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	MC1330A1P	4	7.0	–	8.2	Vdc
	MC1330A2P	4	7.8	–	9.0	Vdc
Supply Current		5, 6	11	17.5	20	mA
Maximum Signal dc Output Voltage		4	–	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)		7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency		1	300	475	650	mVp-p

FIGURE 2 – TEST FIXTURE CIRCUIT



L1, C1: See General Information Number 3, page 5 of this specification.

FIGURE 3 – INPUT ADMITTANCE

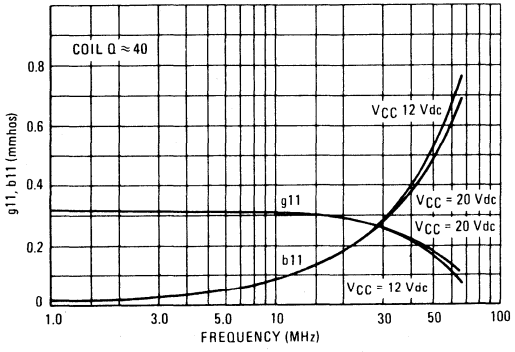
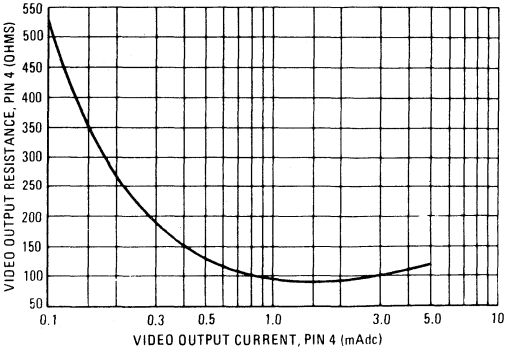


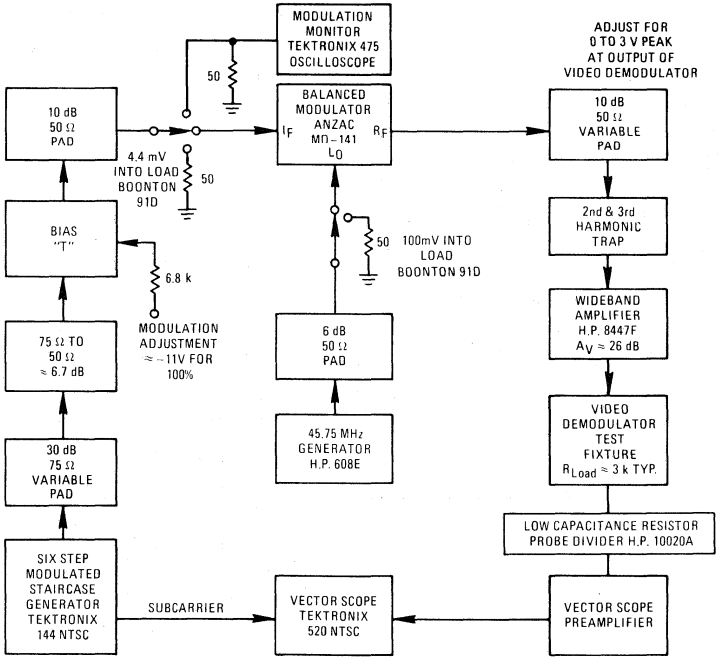
FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Typ	Unit
Input Resistance		7	4.9	kΩ
Input Capacitance		7	1.5	pF
Internal Resistance (Across Tuned Circuit)		2, 3	4.4	kΩ
Internal Capacitance (Across Tuned Circuit)		2, 3	1.0	pF
Negative Video Output Bandwidth (Figure 10)		4	10.8	MHz
Positive Video Output Bandwidth (Figure 10)		5	2.2	MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4	7.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4	4.0	%
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4	8.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4	6.0	%
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = - 6 dB 41.25 MHz = -20 dB		4	−38	dB
Video Output Resistance @ 1 MHz, 2 mA		4	94	Ω
Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.)	V_{CC} = 12 Vdc	7	2.0	Volts
	V_{CC} = 15 Vdc		2.6	
	V_{CC} = 20 Vdc		3.6	
	V_{CC} = 24 Vdc		4.6	
Power Supply Voltage Range		5	10 to 24	Volts

FIGURE 5 – DIFFERENTIAL PHASE AND GAIN TEST SET UP



TYPICAL CHARACTERISTICS

(V_{CC} = +20 Vdc, T_A = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

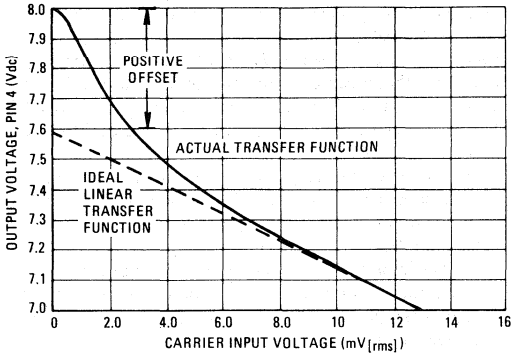


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

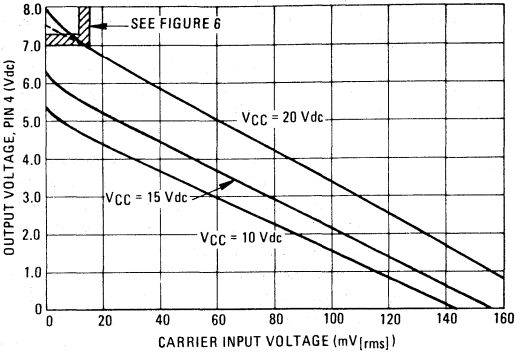


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

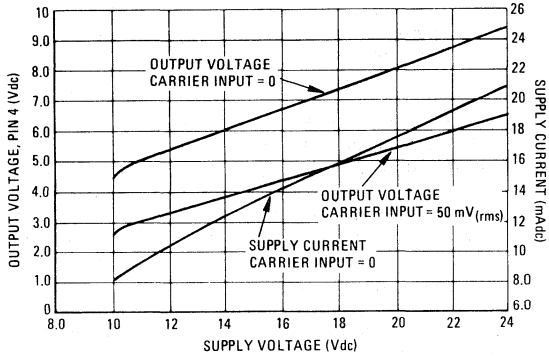


FIGURE 9 – AFT LIMITING

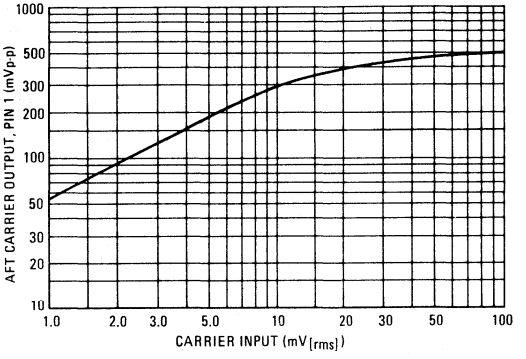


FIGURE 10 – VIDEO OUTPUT RESPONSE

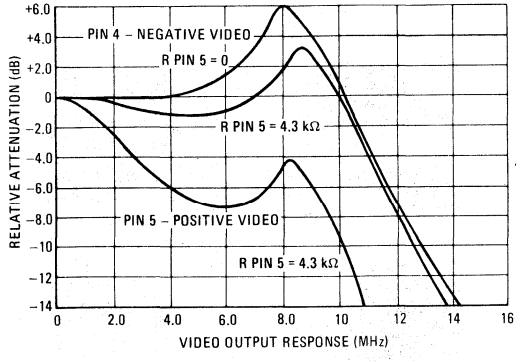
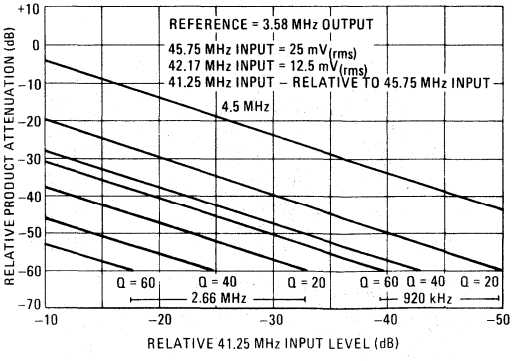


FIGURE 11 – VIDEO OUTPUT PRODUCTS



TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.

5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 – BYPASS DISPLAYED BY CONVENTIONAL SWEEP

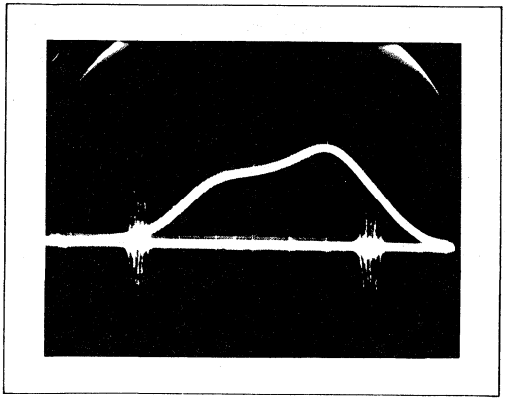


FIGURE 13 – BYPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION

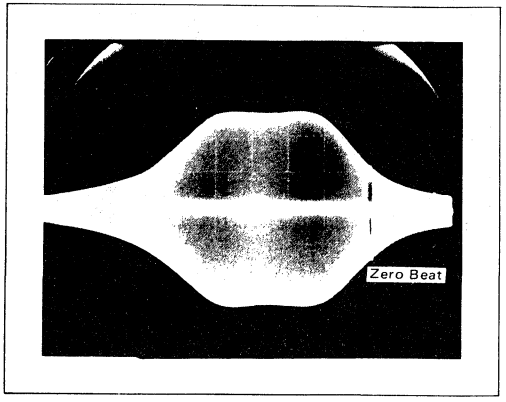
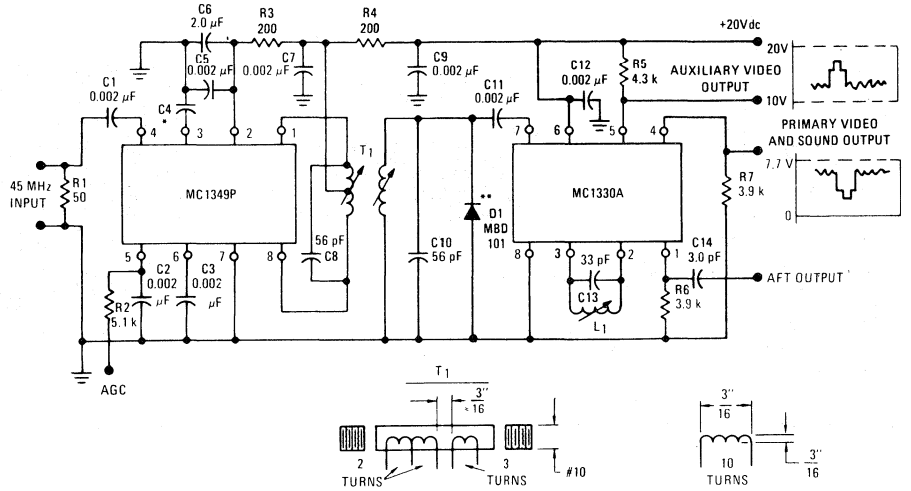


FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT



*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet.
**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6.

FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT

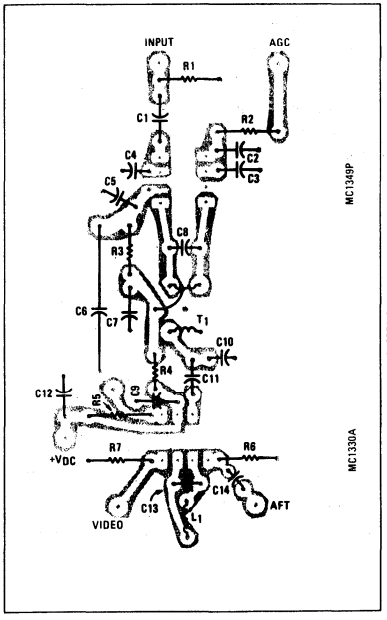
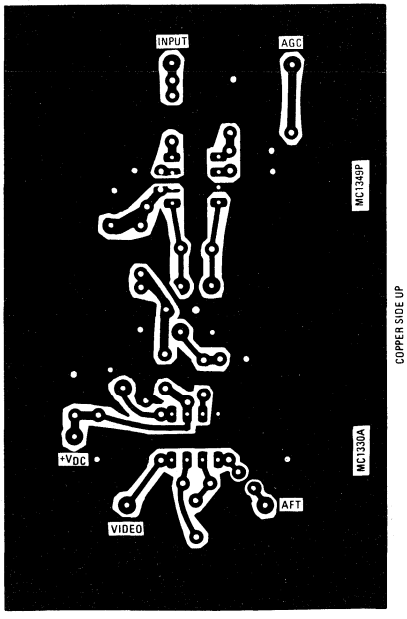
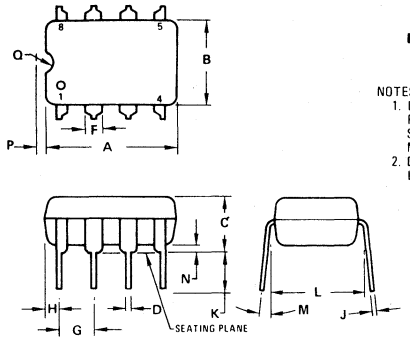


FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT



OUTLINE DIMENSIONS



PLASTIC PACKAGE
CASE 626

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

CASE 626

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

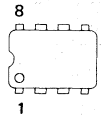
MONOLITHIC IF AMPLIFIER

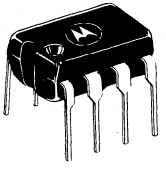
. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

- Power Gain – 60 dB typ at 45 MHz (pin 3 open)
  – 56 dB typ at 58 MHz (pin 3 open)
  – 61 dB typ at 45 MHz (pin 3 bypassed)
  – 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range – 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

IF AMPLIFIER

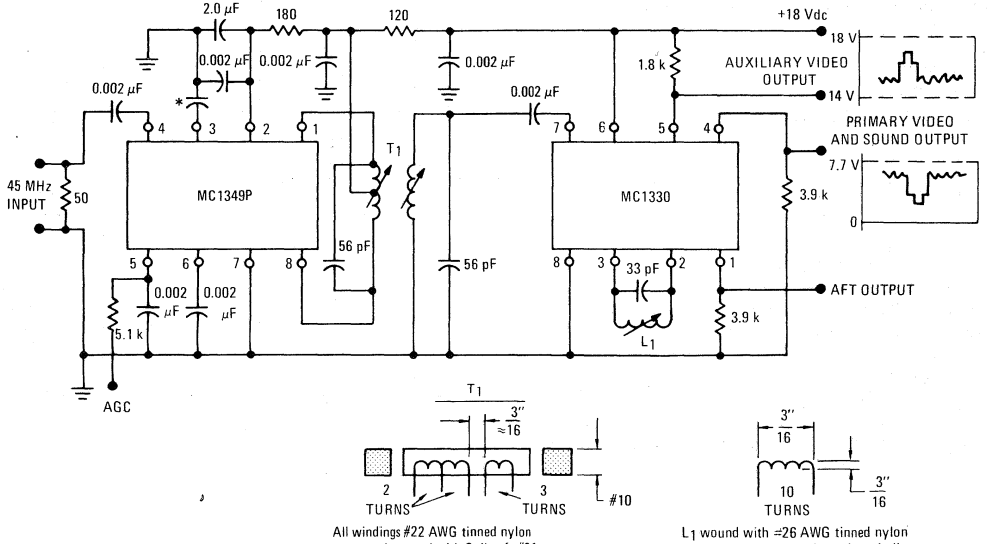
MONOLITHIC SILICON INTEGRATED CIRCUIT





PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L_1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage (V_{CC1})	+18	Vdc
Output Supply Voltage (V_{CC2})	+18	Vdc
AGC Supply Voltage	$\leq V_{CC1}$ (pin 2)	Vdc
Differential Input Voltage	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [pin 2], V_{CC2} = +15 Vdc [pins 1 and 8], T_A = +25°C unless otherwise noted.)

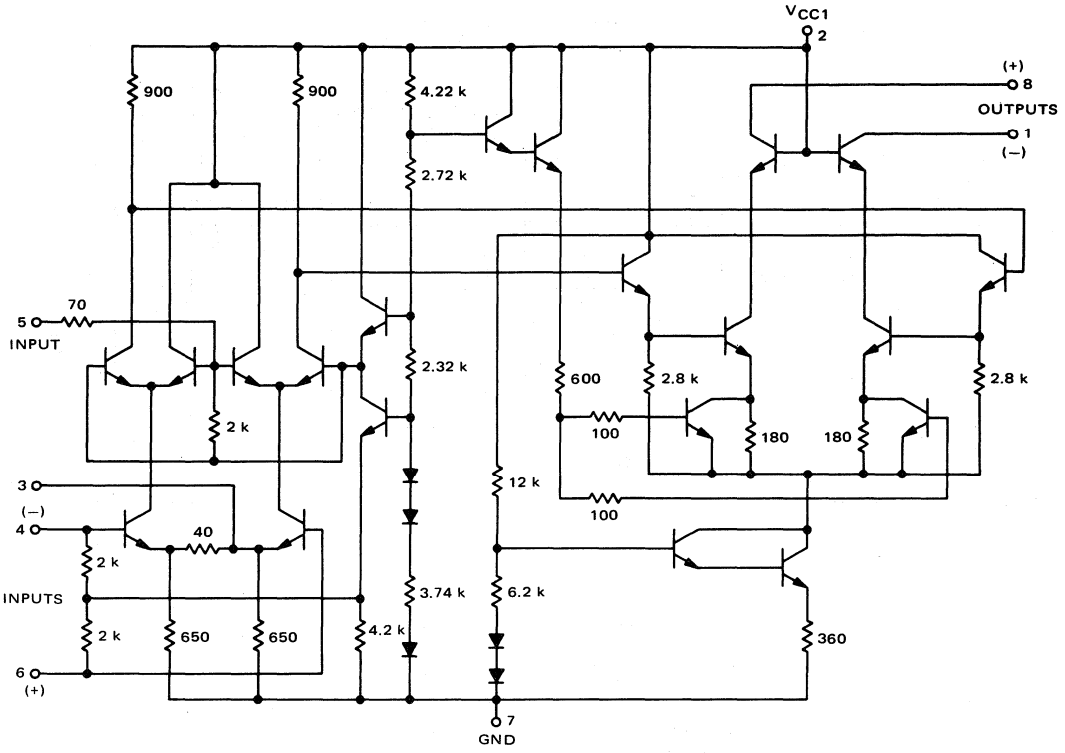
Characteristic	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3)	70	80	–	dB
Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed	 52 – – –	 60 61 56 59	 – – – –	dB
Maximum Differential Output Voltage Swing	–	6.0	–	Vp-p
Output Stage Current (pins 1 and 8)	–	9.0	–	mA
Amplifier Current (pin 2)	–	15	20	mAdc
Power Dissipation	–	315	400	mW
Noise Figure f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB	–	8.5	–	dB

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [pin 2], V_{CC2} = +15 Vdc, [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Frequency		Unit
		45 MHz	58 MHz	
Single-Ended Input Admittance, input pin 4, AGC min Pin 3 open Pin 3 open Pin 3 bypassed Pin 3 bypassed	 g11 b11 g11 b11	 0.74 1.9 4.1 6.5	 0.95 2.4 5.4 6.9	mmhos
Differential Output Admittance, AGC max	 g22 b22	 5.5 270	 8.3 360	μmhos
Reverse Transfer Admittance (magnitude)		1.5	2.0	μmhos
Forward Transfer Admittance Magnitude, pin 3 open Angle (0 dB AGC), pin 3 open Magnitude, pin 3 bypassed Angle (0 dB AGC), pin 3 bypassed		 520 100 1020 120	 400 130 800 400	 mmhos degrees mmhos degrees
Single-Ended Input Capacitance, AGC min Pin 3 open Pin 3 bypassed		 6.8 2.3	 6.7 20	pF
Differential Output Capacitance (AGC max)		1.0	1.0	pF

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 2 – CIRCUIT SCHEMATIC



GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

TEST CIRCUITS

FIGURE 3 – TUNED INPUT
(PIN 3 OPEN)

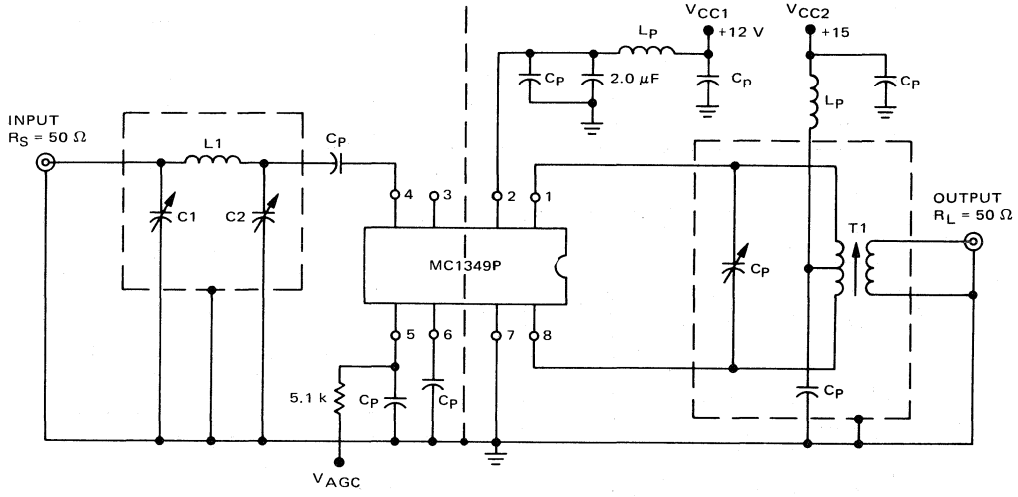
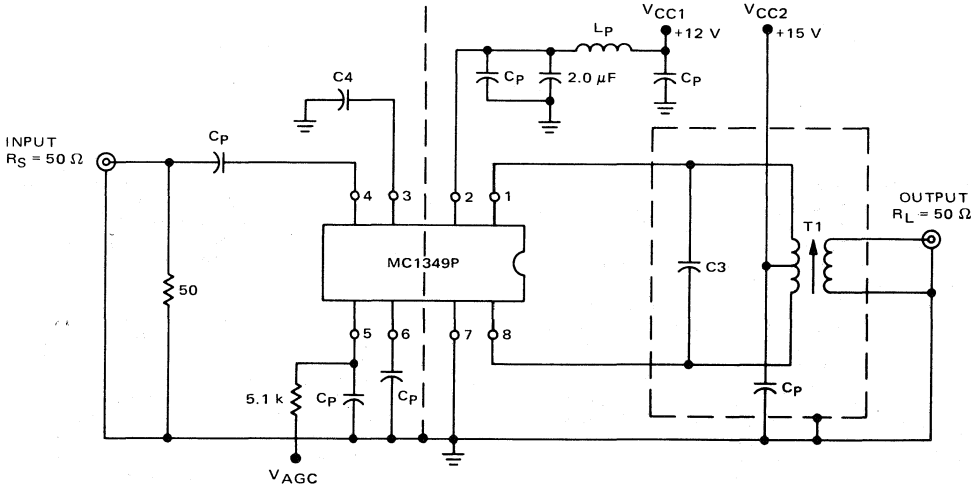


FIGURE 4 – UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)



PARTS LIST

COMPONENT	45 MHz	58 MHz
C1	8-60 pF	50-100 pF
C2	3-35 pF	3-35 pF
C3	1-7.0 pF	1-7.0 pF
C4	82-470 pF	82-470 pF
C_P	0.0015 μF	0.001 μF
L1	0.84 μH	0.33 μH
L_P	10 μH	10 μH

T1 Primary 14 turns center-tapped
Secondary 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
Wire: #26 AWG tinned nylon acetate wound on 1/4" diameter coil form
Core: Arnold Type TH, 1/2" long or equivalent.

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

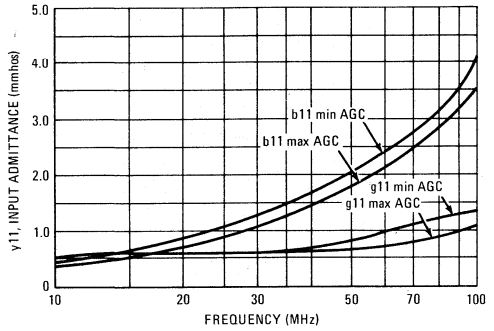


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

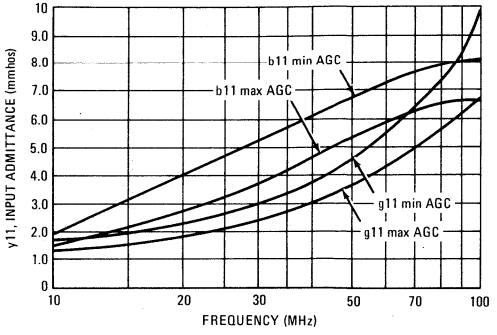


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

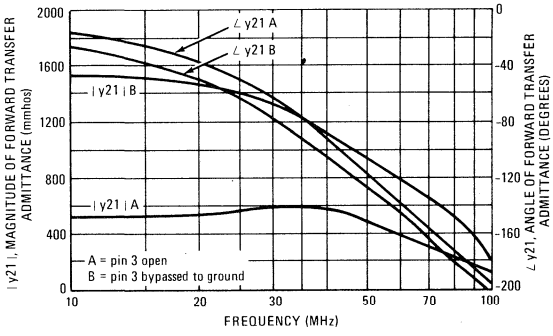


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

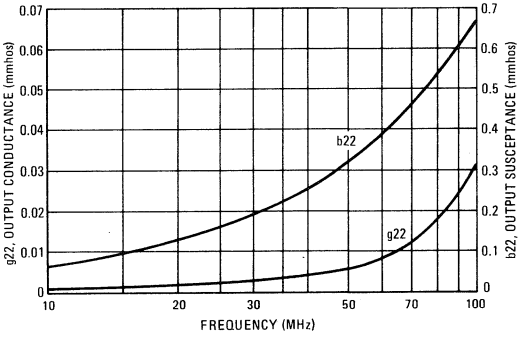


FIGURE 9 – NOISE FIGURE

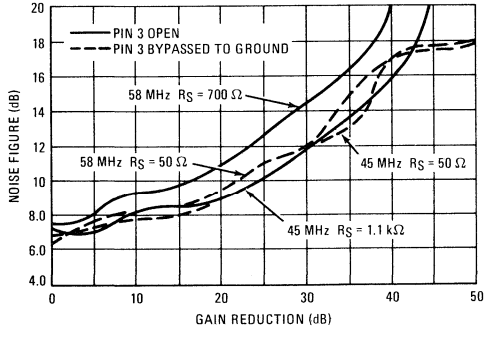
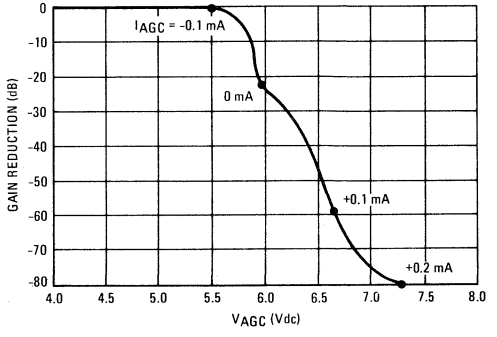
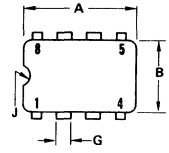
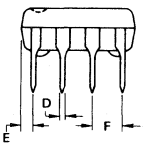


FIGURE 10 – GAIN REDUCTION

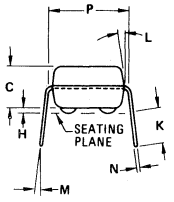


OUTLINE DIMENSIONS





Weight ≈ 0.446 gram



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.370	.390	9.39	9.90
B	.240	.250	6.09	6.35
C	.135	.155	3.43	3.94
D	.015	.019	.381	.483
E	–	.045	–	1.14
F	0.100 TP		2.54 TP	
G	.030	.060	.762	1.52
H	.020 NOM		.508 NOM	
J	.030	.040R	.762	1.02R
K	.115	.135	2.92	3.43
L	7° TYP		7° TYP	
M	0°	10°	0°	10°
N	.008	.011	.203	.279
P	.290	.310	7.37	7.87

NOTES:
1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL.
2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED.

CASE 626
PLASTIC PACKAGE

MONOLITHIC IF AMPLIFIER

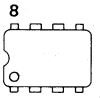
. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – $<<$ 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER

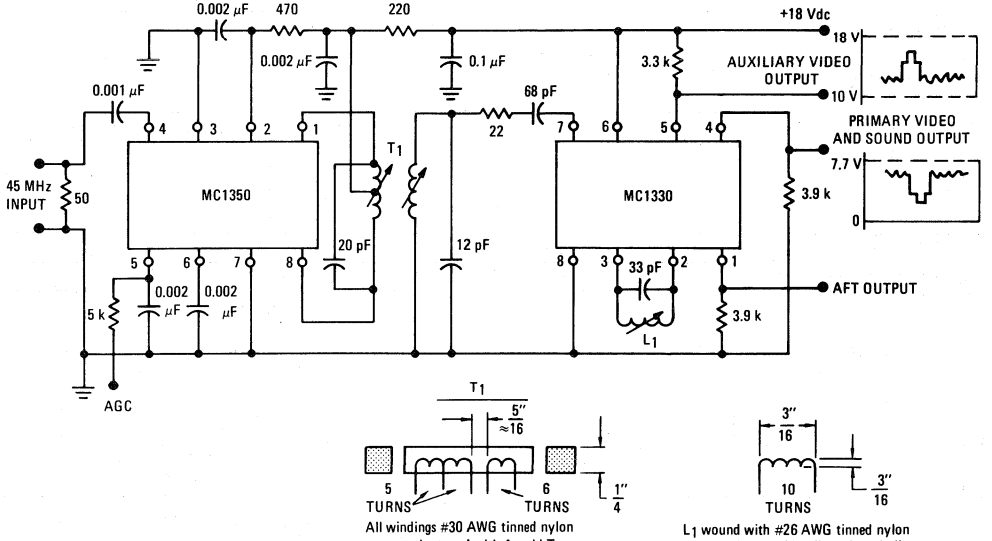
MONOLITHIC SILICON INTEGRATED CIRCUIT

NOVEMBER 1970 – DS 9127 R1



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)	A_p				dB
f = 58 MHz, BW = 4.5 MHz } See Figure 5		–	48	–	
f = 45 MHz, BW = 4.5 MHz } See Figure 5		46	50	–	
f = 10.7 MHz, BW = 350 kHz } See Figure 6		–	58	–	
f = 455 kHz, BW = 20 kHz } See Figure 6		–	62	–	
Maximum Differential Voltage Swing	V_o				V_{p-p}
0 dB AGC		–	20	–	
-30 dB AGC		–	8.0	–	
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	μmhos
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	$\ll$1.0	$\ll$1.0	$\ll$1.0	$\ll$1.0	μmho
Forward Transfer Admittance						
Magnitude	$\lvert y_{21} \rvert$	160	160	200	180	mmhos
Angle (0 dB AGC)	< y_{21}	-5.0	-20	-80	-105	degrees
Angle (-30 dB AGC)	< y_{21}	-3.0	-18	-69	-90	degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

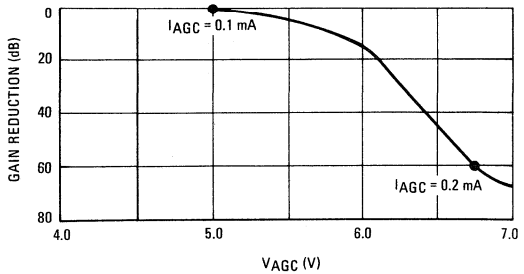
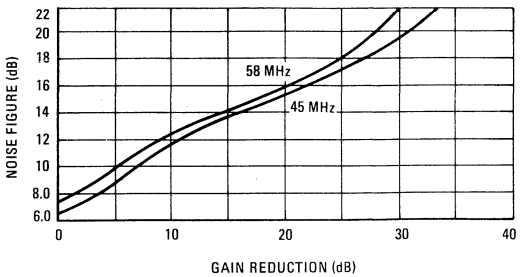


FIGURE 3 – NOISE FIGURE
(Figure 5)



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 – CIRCUIT SCHEMATIC

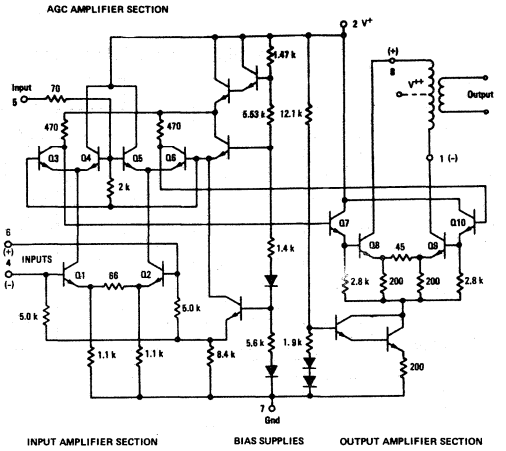
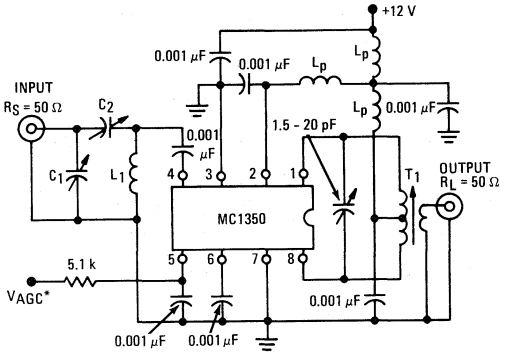


FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)

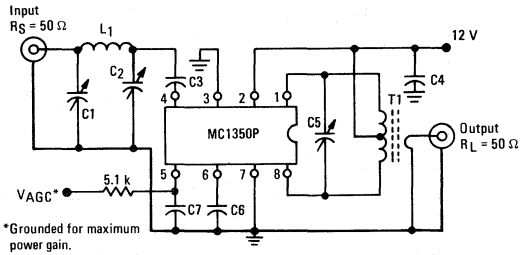


*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20\ k\Omega$
See Figure 10 for frequency response curve.

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2" Long

	45 MHz		58 MHz	
L_1	0.4 μH	Q ≥ 100	0.3 μH	Q ≥ 100
T_1	1.3 -3.4 μH	Q ≥ 100 @ 2 μH	1.2 -3.8 μH	Q ≥ 100 @ 2 μH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



*Grounded for maximum power gain.

Note 1. Primary: 120 μH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	–	4.6 μH
T1	Note 1	Note 2

TYPICAL CHARACTERISTICS

(V^+ = 12 V, T_A = +25°C)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

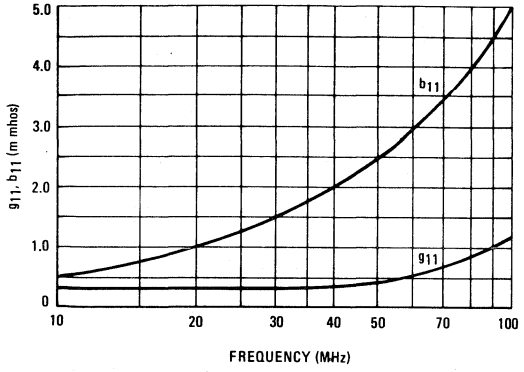


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

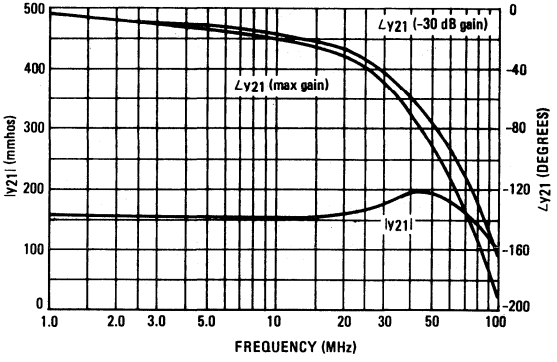


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

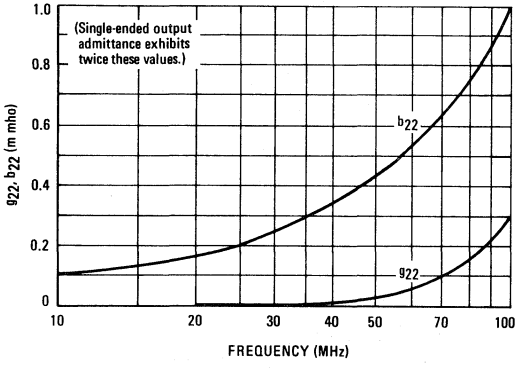


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)

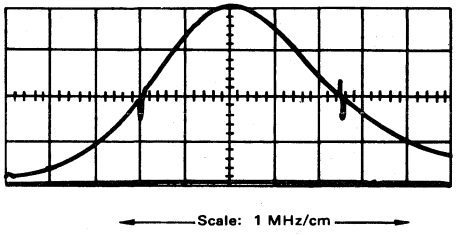
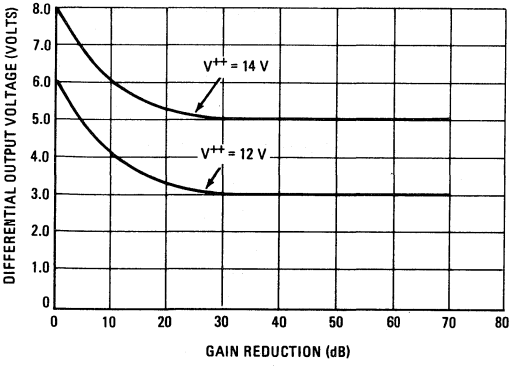
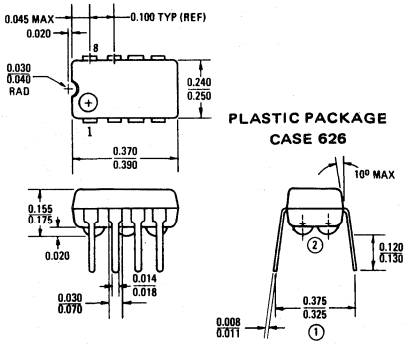


FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

OUTLINE DIMENSIONS



① This dimension is measured at the seating plane.
② Four insulating stand-offs are provided. Weight ≈ 0.446 gram.

To convert inches to millimeters multiply by 25.4.

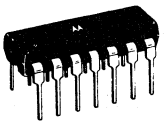
BALANCED FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

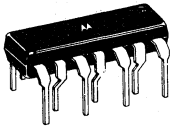
- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

LIMITING FM IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



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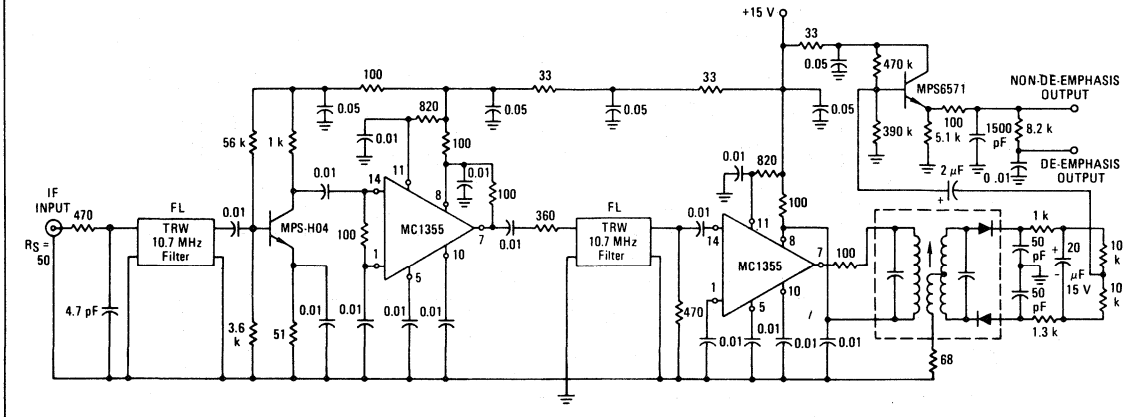
CASE 647

FIGURE 1 – DUAL MC1355 FM IF APPLICATION



*All other pins grounded
T-Ratio Detector (input impedance ≅ 1.5 k) G.1. #36231 or equivalent

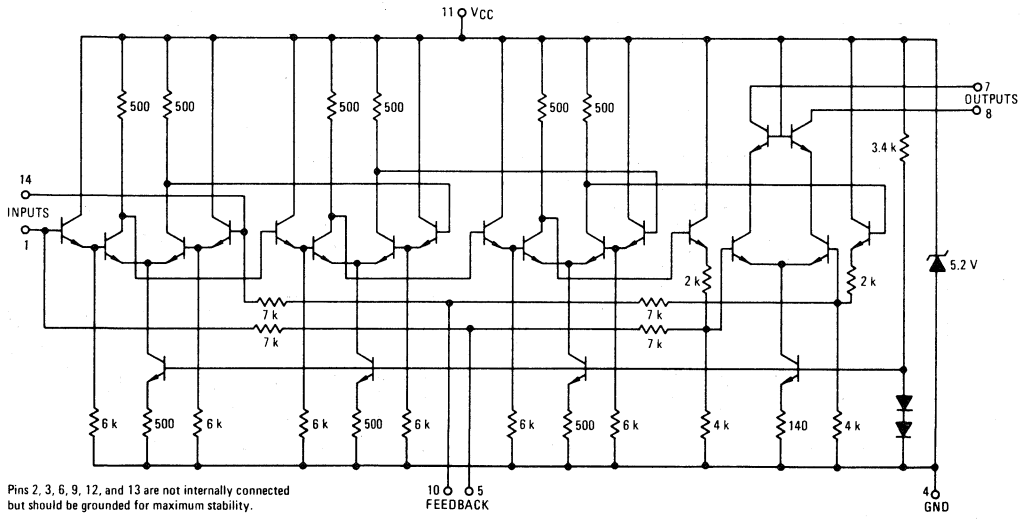
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Output Voltage (pins 7 & 8)	40	Vdc
Supply Current to pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, f = 10.7 MHz, T_A = +25°C)

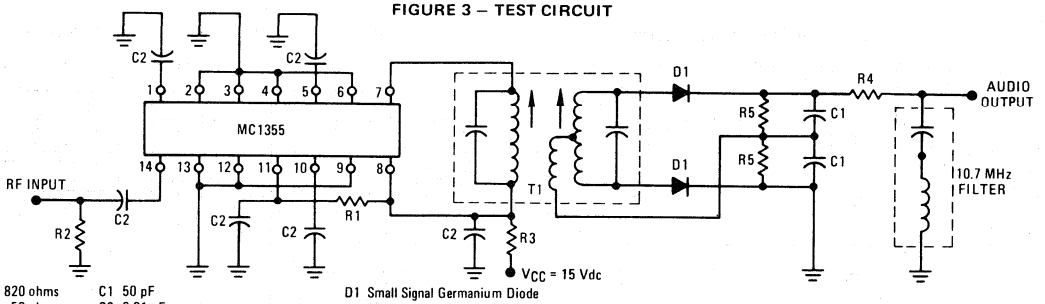
Characteristic		Min	Typ	Max	Units
Power Supply Voltage Range		8.0	15	18	Vdc
Total Circuit Current		–	16	–	mAdc
Total Output Stage Current		–	4.2	–	mA
Device Dissipation		–	125	–	mW
Internal Zener Voltage		–	5.2	–	Vdc
Input Signal for 3 dB Limiting		–	175	250	μV(rms)
Output Current Swing		3.5	4.2	5.0	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)		–	60	–	dB
Admittance Parameters	Y_{11}	–	120 + j320	–	μmhos
	Y_{12}	–	j0.6	–	μmho
	Y_{21}	–	8 + j5.9	–	mhos
	Y_{22}	–	15 + j230	–	μmhos

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT



R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0.01 μF
T1 10.7 MHz Foster-Seeley Discriminator, Primary Impedance = 3.9 k, Peak-to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

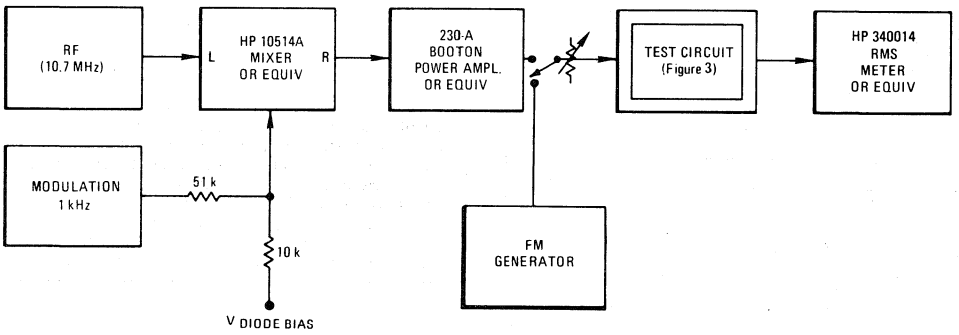


FIGURE 5 – LIMITING

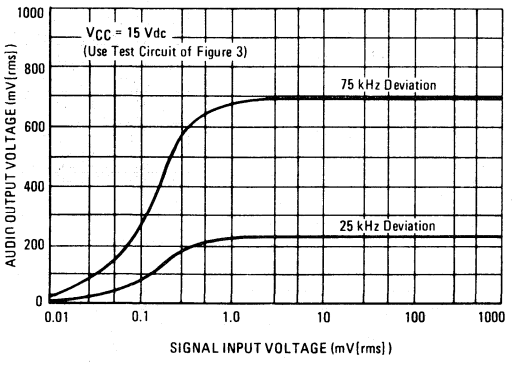
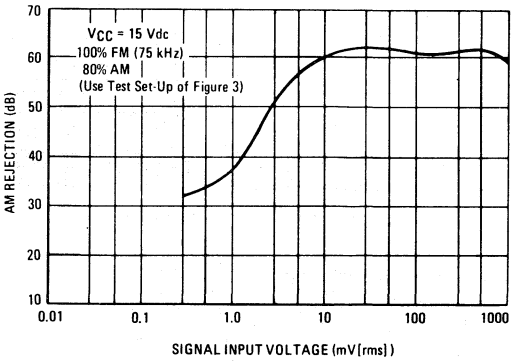


FIGURE 6 – AM REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

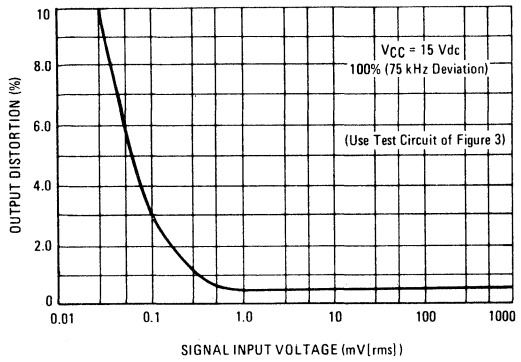


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

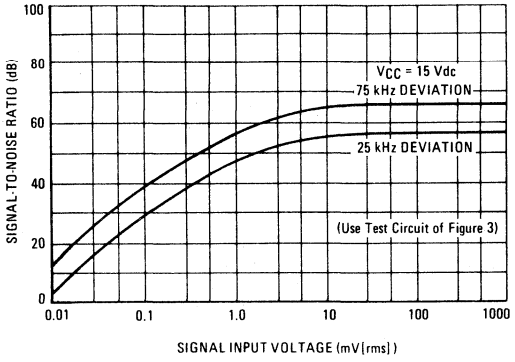
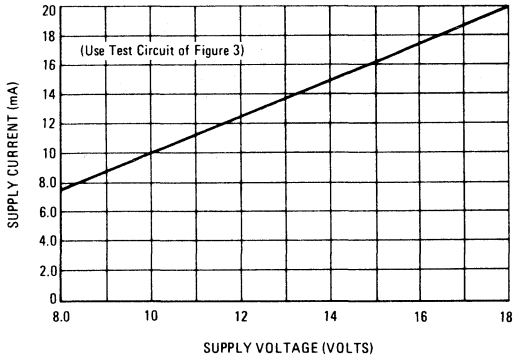


FIGURE 9 – TOTAL SUPPLY CURRENT



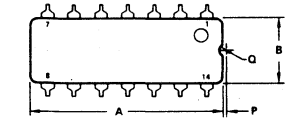
Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

OUTLINE DIMENSIONS

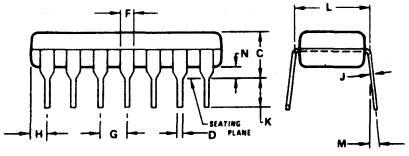
P SUFFIX
PLASTIC PACKAGE
CASE 646

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030



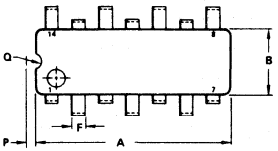
Weight ≈ 0.911 gram



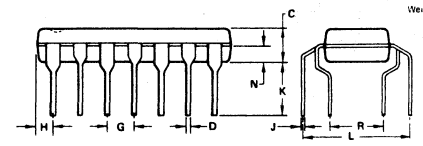
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	3.30	3.81	0.130	0.150
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	3.81	–	0.150	–
L	9.52	10.92	0.375	0.430
N	1.02	1.52	0.040	0.060
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030
R	4.70	5.97	0.185	0.235

NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION



Weight ≈ 0.911 gram



FM DETECTOR AND LIMITER

. . . includes a limiting amplifier, a quadrature discriminator, and a voltage regulator; and is designed primarily for FM receiver applications. It is similar to the MC1357 and includes built-in regulation capable of supplying 20 mA to external circuitry.

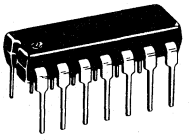
Features:

- Good Line and Load Regulation
- Low Harmonic Distortion
- Single Tuning Coil Design
- Direct Replacement for uLN2136

FM DETECTOR AND LIMITER

SILICON MONOLITHIC INTEGRATED CIRCUITS

P SUFFIX
PLASTIC PACKAGE
CASE 646



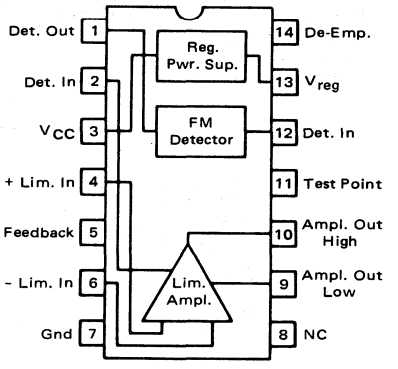
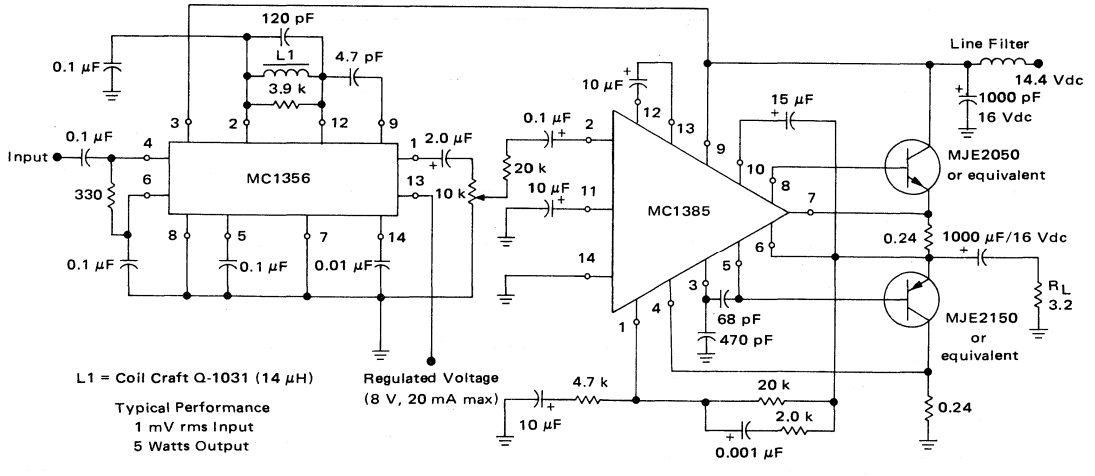


FIGURE 1 – TYPICAL AUTOMOTIVE APPLICATIONS CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	+16	Vdc
Power Dissipation @ T_A = +25°C (Package Limitation) Derate above 25°C	1.0 7.7	W mW/°C
Operating Temperature Range	-25 to +85	°C
Storage Temperature Range	-65 to +150	°C
Regulator Load (Pin 13)	20	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Recommended Operating Voltage	3	10	–	16	Vdc
Drain Current	3	14	16	19	mA
Amplifier Input Reference Voltage	6	1.3	1.4	1.5	Vdc
Detector Input Reference Voltage	2	3.3	3.5	3.7	Vdc
Detector Output Voltage	1	3.0	3.8	4.6	Vdc
Amplifier Input Resistance	4	–	15	–	kΩ
Amplifier Input Capacitance	4	–	7.0	–	pF
Amplfier Output Resistance	10	–	90	–	Ohms
De-Emphasis Resistance	14	7.0	8.8	10.5	kΩ
Temperature Sensitivity of Power Supply	13	–	+0.2	–	mV/°C
Temperature Sensitivity of Output Voltage	1	–	+0.3	–	mV/°C
Regulation Voltage	13	7.9	8.1	8.3	Vdc

DYNAMIC CHARACTERISTICS (FM Modulation Frequency = 1.0 kHz, T_A = 25°C)
(V_{CC} = 12 Vdc, f_o = 10.7 MHz, f = ±75 kHz)

Characteristic	Pin	Min	Typ	Max	Unit
AM Rejection (V_{IN} = 10 mVrms)	1	36	42	–	dB
Input Limiting Threshold Voltage (-3 dB, V_{IN} @ 10 mVrms)	4	380	400	500	μV(RMS)
Recovered Audio Output Voltage (V_{IN} = 10 mV(rms)	1	350	450	550	mV(RMS)
Output Distortion (V_{IN} = 10 mVrms)	1	–	1.0	2.0	%
Signal to Noise (V_{IN} = 10 mV rms)	1	–	70	–	dB

FIGURE 2 – MC1356P TEST CIRCUIT

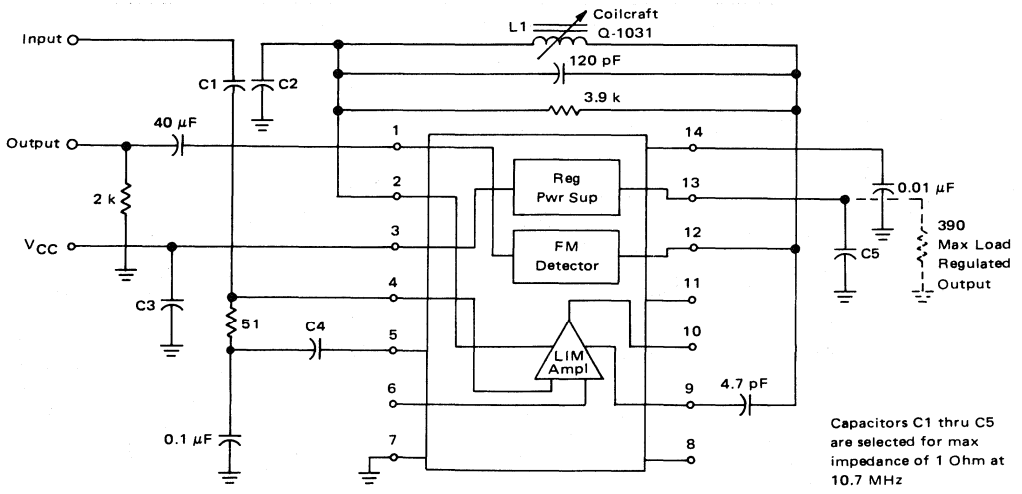


FIGURE 3 – AM REJECTION

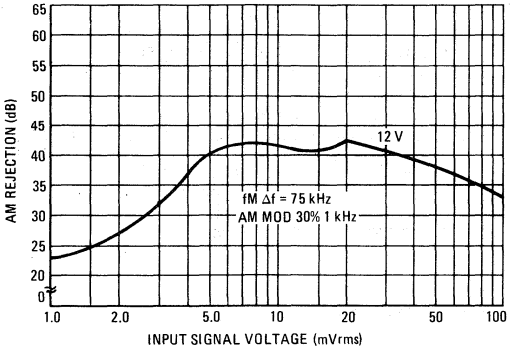


FIGURE 4 – SIGNAL-TO-NOISE RATIO

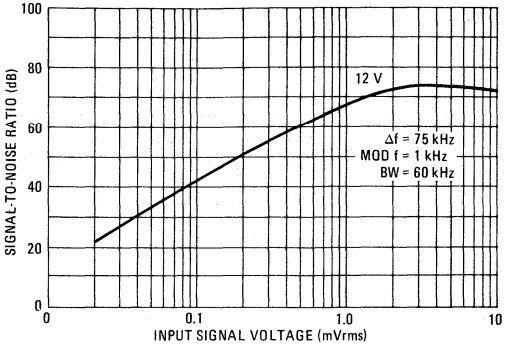


FIGURE 5 – RECOVERED AUDIO OUTPUT versus SIGNAL INPUT VOLTAGE

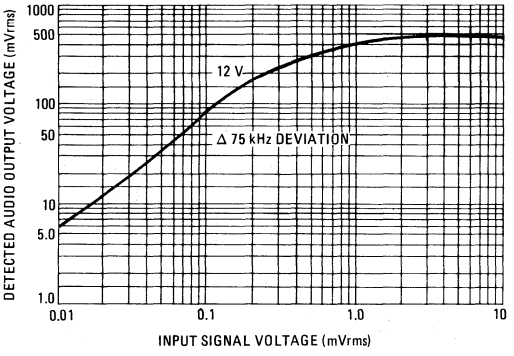


FIGURE 6 – REGULATED VOLTAGE versus SUPPLY VOLTAGE

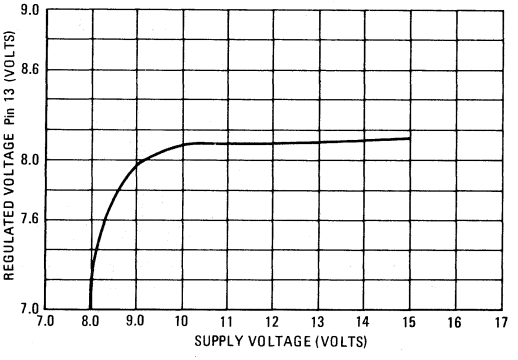


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC

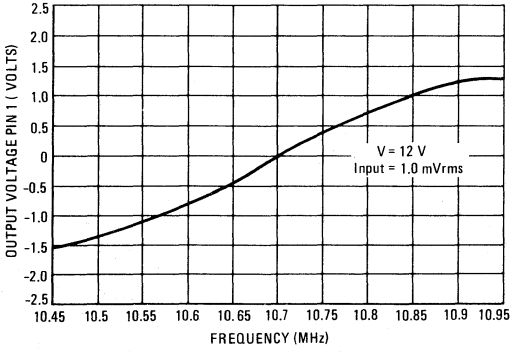


FIGURE 8 – TYPICAL FM RADIO RECEIVER BLOCK DIAGRAM USING MC1356P

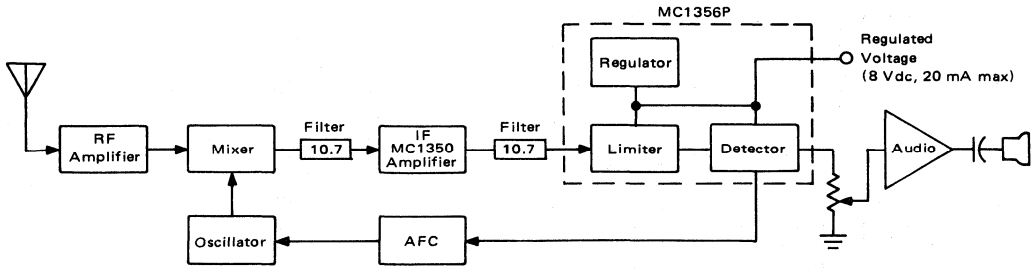
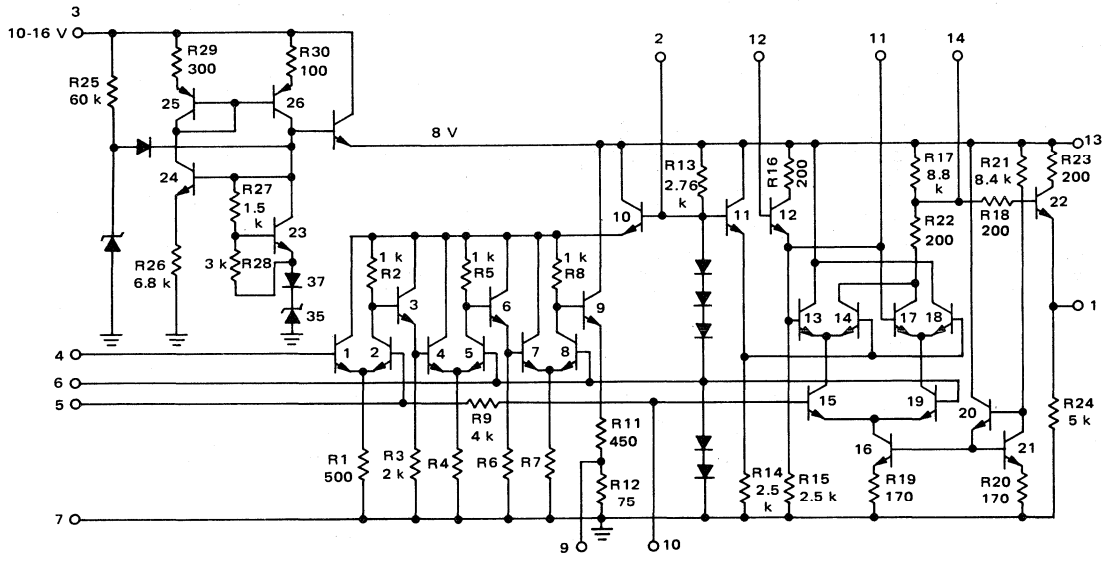
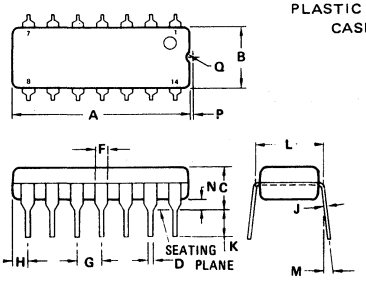


FIGURE 9 – MC1356P TEST CIRCUIT SCHEMATIC



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 646



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

TV SOUND IF AMPLIFIER

. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

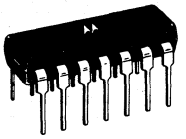
- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control – Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability – 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

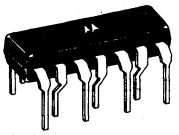
IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

JUNE 1971 – DS 9178

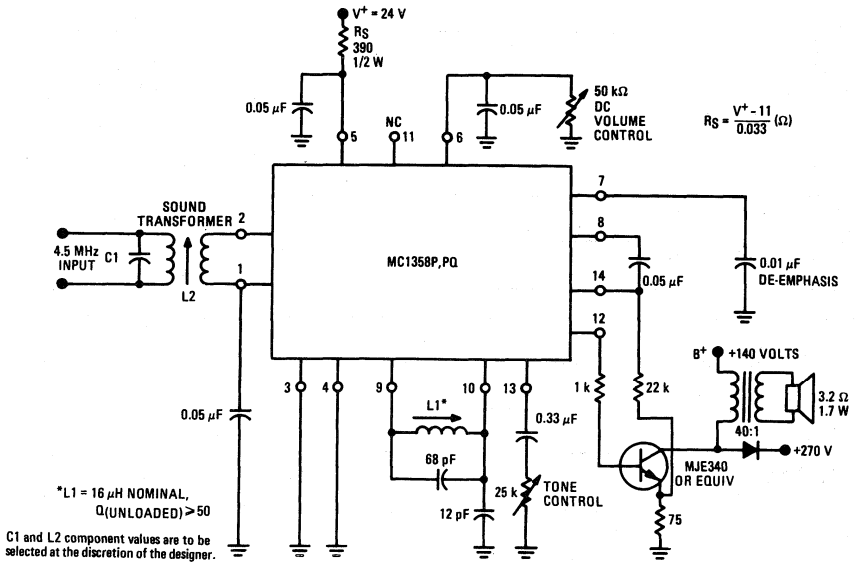
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116





PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0.5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0.91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between pin 9 and GND) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 – –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

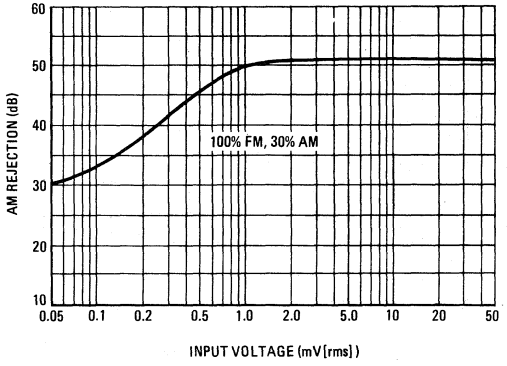
Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

(V^+ = 24 V, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

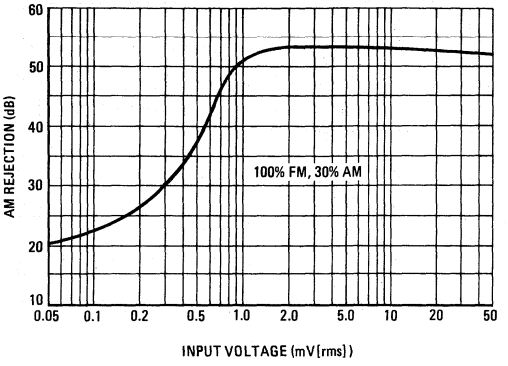


FIGURE 4 – DETECTED AUDIO OUTPUT

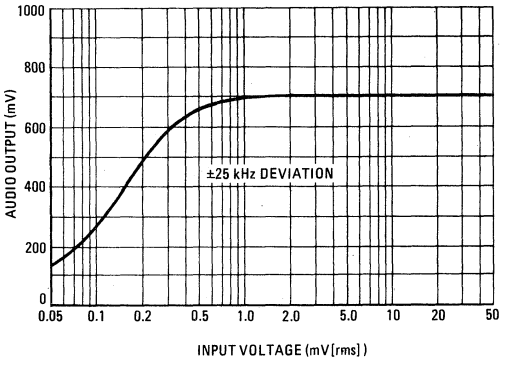


FIGURE 5 – DETECTED AUDIO OUTPUT

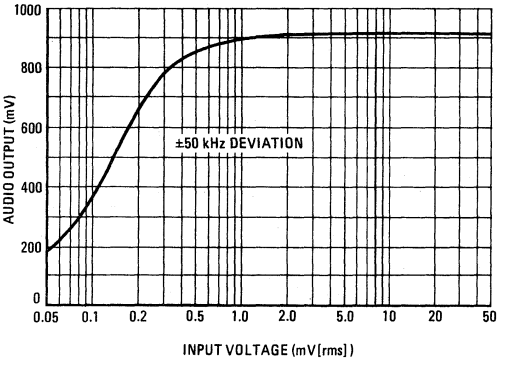


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD

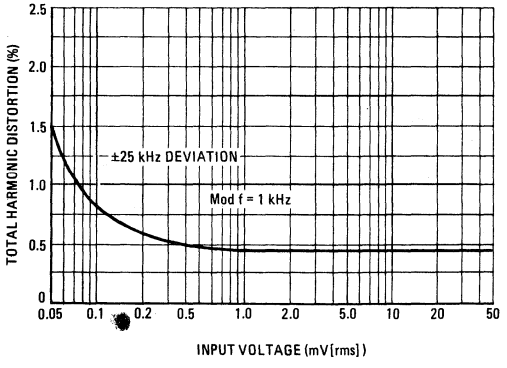
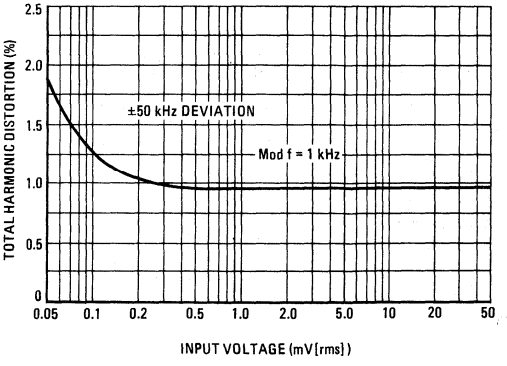


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

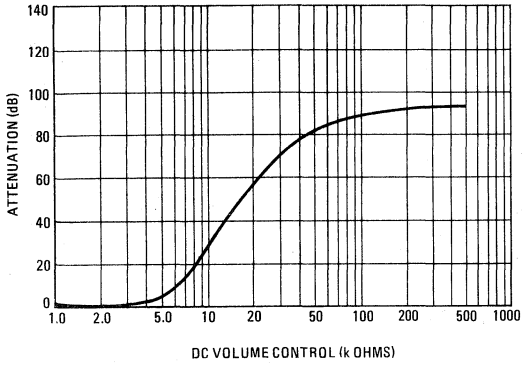


FIGURE 9 – AUDIO AMPLIFIER THD

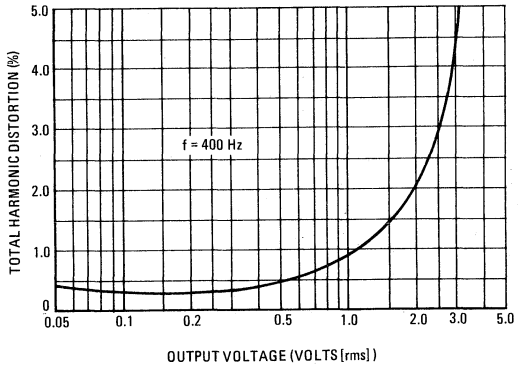


FIGURE 10 – IF FREQUENCY RESPONSE

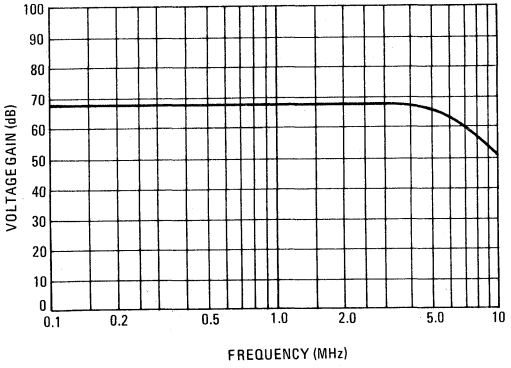


FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

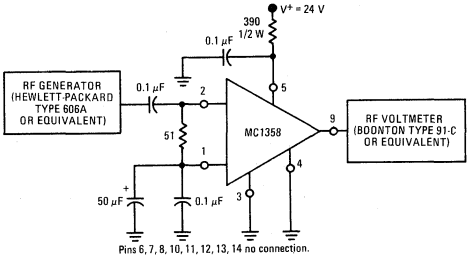


FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

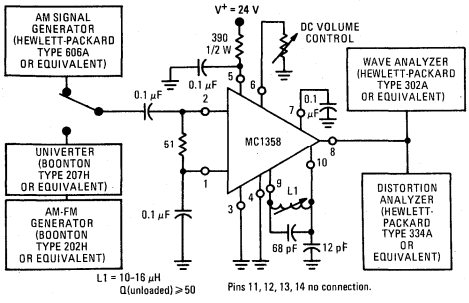


FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

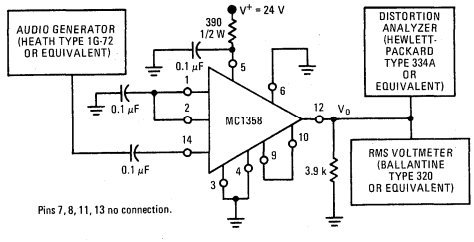


FIGURE 14 – CIRCUIT SCHEMATIC

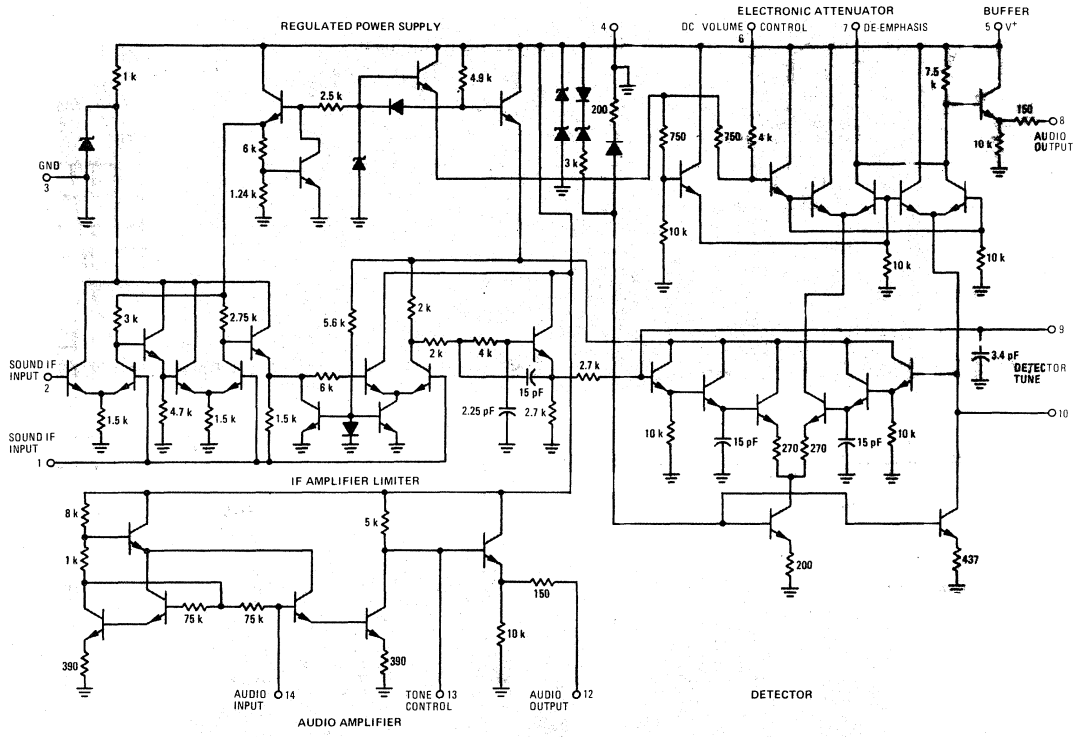


FIGURE 15 – ALTERNATE APPLICATION CIRCUIT

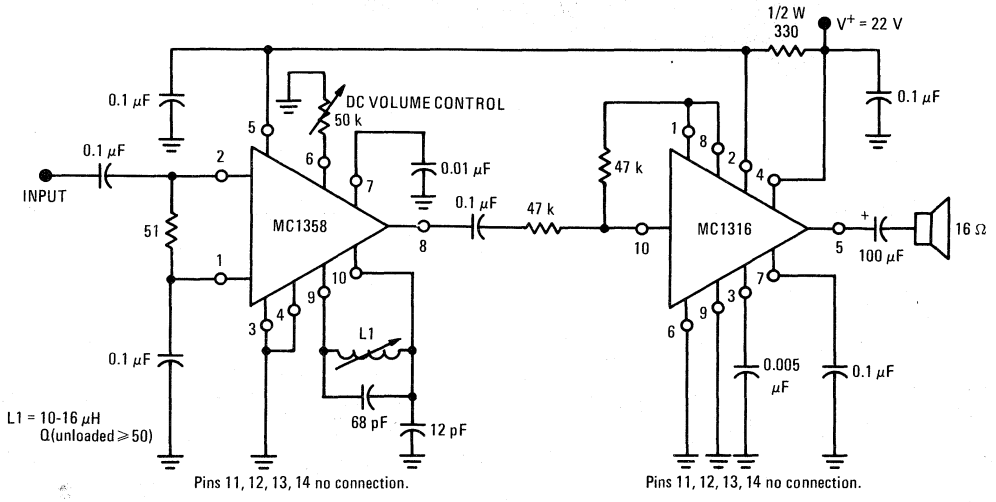
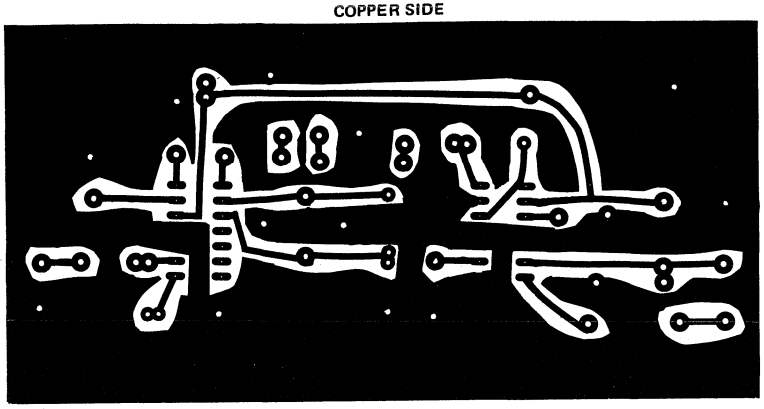
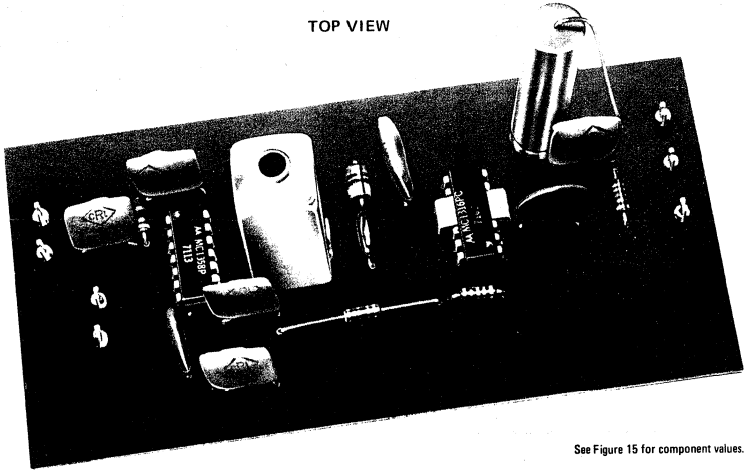


FIGURE 16 – MC1358/MC1316 PRINTED CIRCUIT BOARD

COPPER SIDE

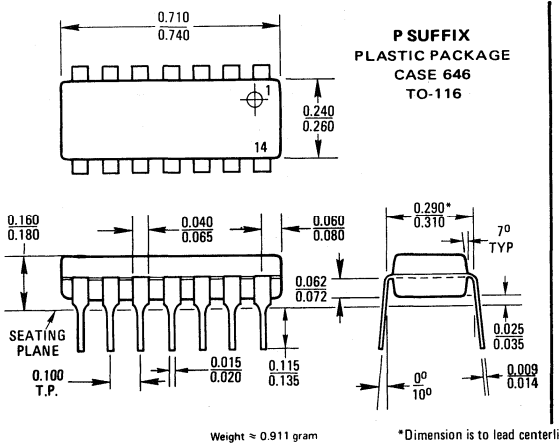


TOP VIEW



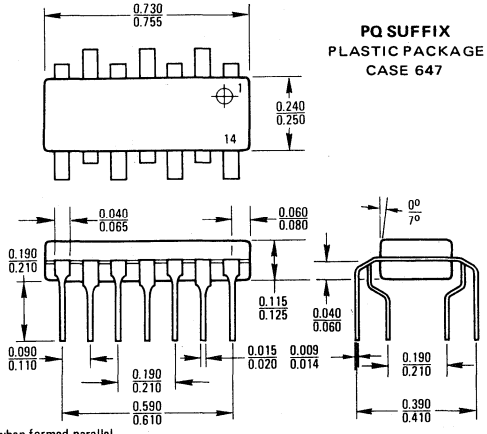
See Figure 15 for component values.

OUTLINE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

Weight ≈ 0.911 gram



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

Weight ≈ 0.911 gram

*Dimension is to lead centerline when formed parallel.
To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1496G	0°C to +70°C	Metal Can
MC1496L	0°C to +70°C	Ceramic DIP
MC1496P	0°C to +70°C	Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L	−55°C to +125°C	Ceramic DIP

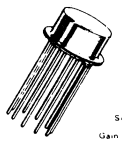
BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

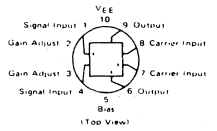
- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

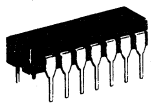
BALANCED MODULATOR – DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



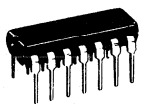
G SUFFIX
METAL PACKAGE
CASE 603

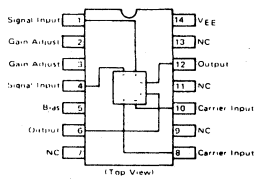




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1496 only)





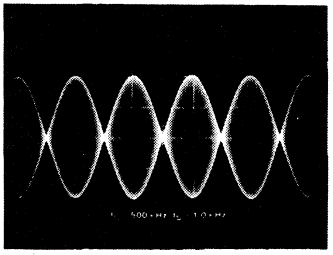


FIGURE 1
SUPPRESSED-CARRIER
OUTPUT WAVEFORM

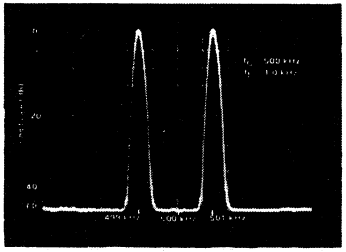


FIGURE 2 –
SUPPRESSED-CARRIER
SPECTRUM

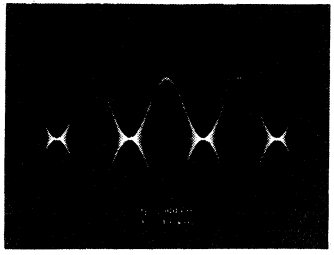
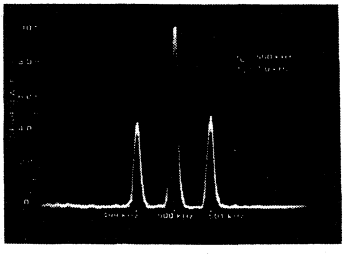


FIGURE 3 –
AMPLITUDE-MODULATION
OUTPUT WAVEFORM

FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5+I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°C		3.85	mW/°C*
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

Characteristic	Fig	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz				–	40	–	–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression	5	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave				–	300	–	–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sine wave										
Signal Input Port, V_S = 300 mV(rms) sine wave				–	80	–	–	80	–	
$\lvert V_C \rvert$ = 0.5 Vdc										
Signal Gain	10	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 Vdc										
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	6	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current	7	–								μA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current	7	–								μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$			$\lvert I_{ioS} \rvert$	–	0.7	5.0	–	0.7	7.0	
			$\lvert I_{ioC} \rvert$	–	0.7	5.0	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Iio} \rvert$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	7	–	$\lvert I_{oo} \rvert$	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Ioo} \rvert$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc	9	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_9$			I_{CC}	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_{EE}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

GENERAL OPERATING INFORMATION *

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\ I_5\ (V_6 - V_{10}) + I_5\ (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega$$ where: R_5 is the resistor between pin 5 and ground

ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y21C = \left.\frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\right| V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y21S = \left.\frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\right| V_c = 0.5\text{ Vdc}, V_o = 0$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

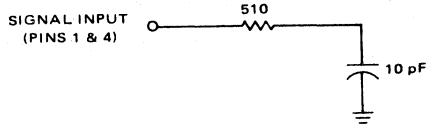
Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION

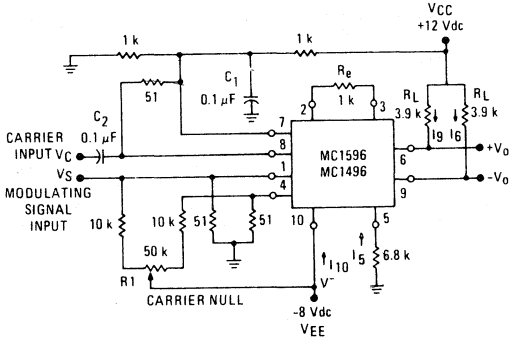


FIGURE 6 – INPUT-OUTPUT IMPEDANCE

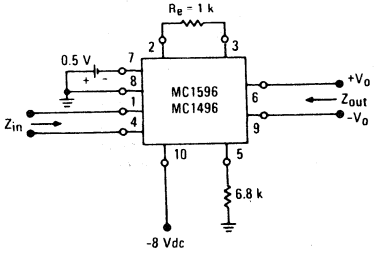


FIGURE 7 – BIAS AND OFFSET CURRENTS

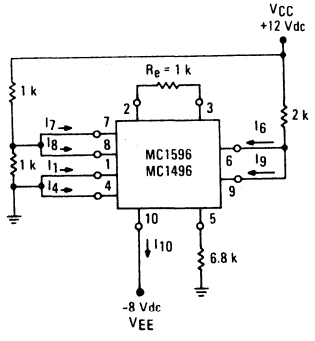
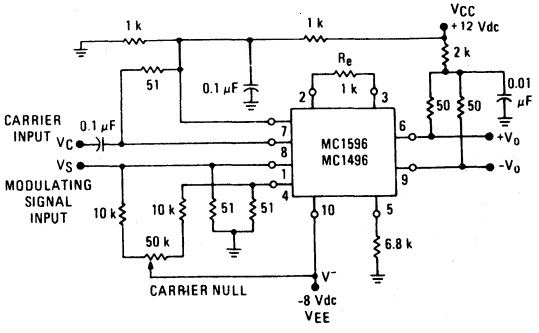


FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TEST CIRCUITS (continued)

FIGURE 9 – COMMON-MODE GAIN

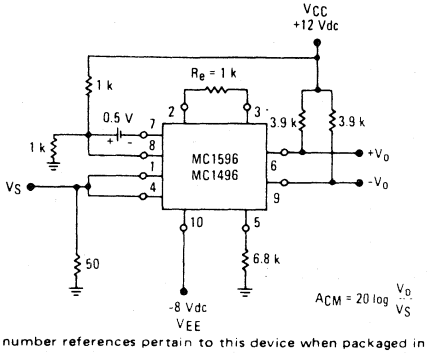
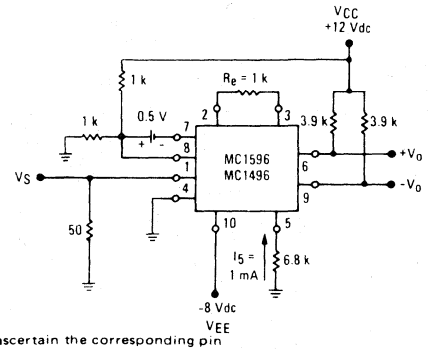


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

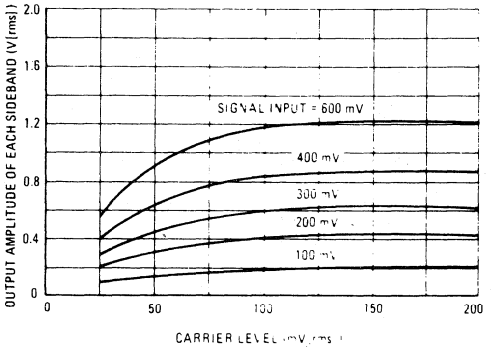


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

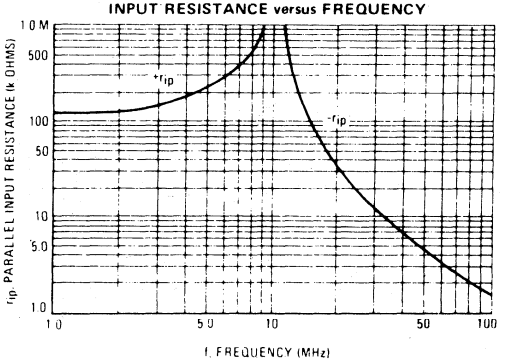


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

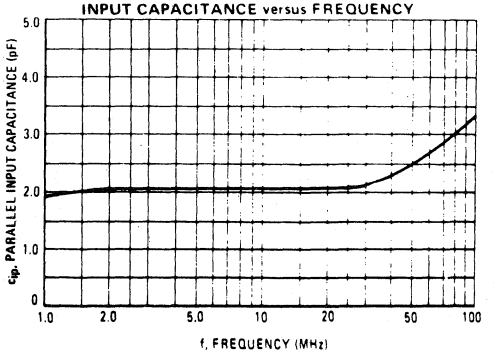
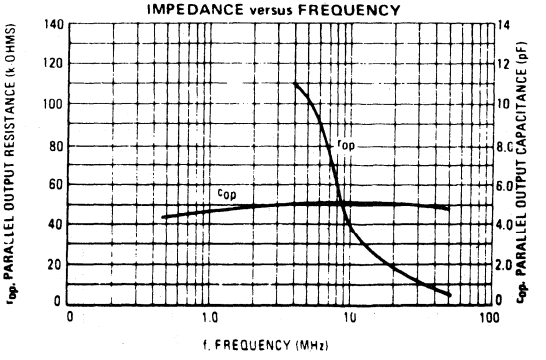


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

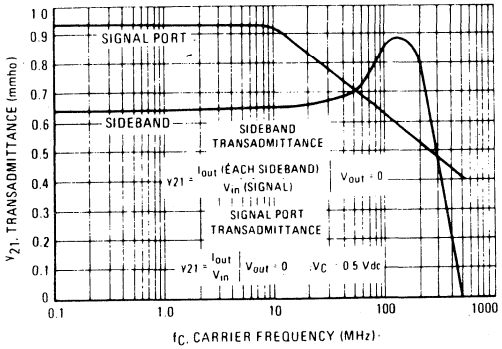


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

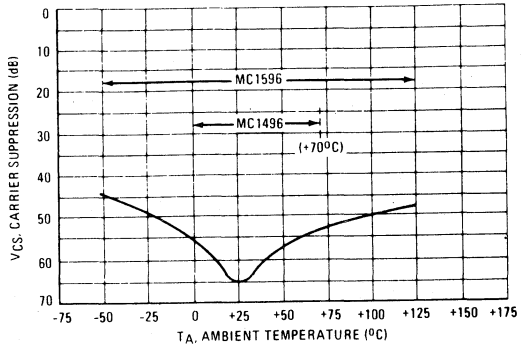


FIGURE 17 – SIGNAL PORT FREQUENCY RESPONSE

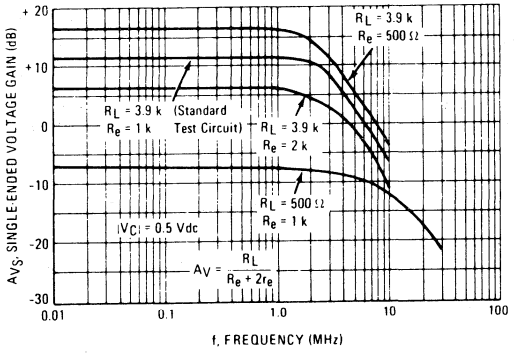


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

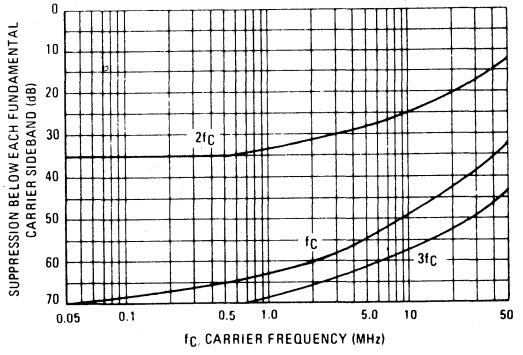


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

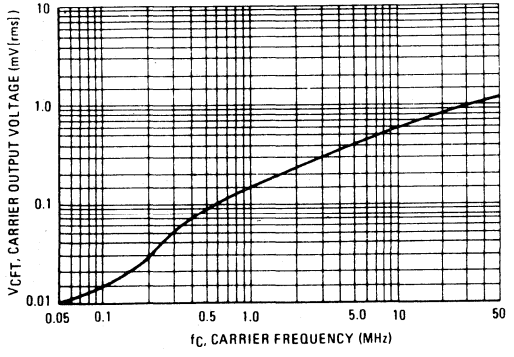
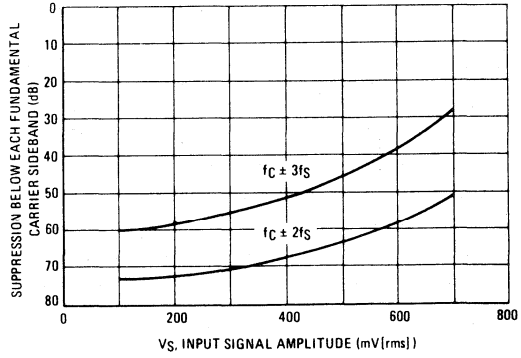


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

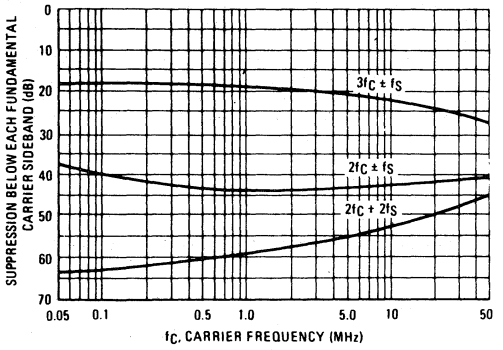
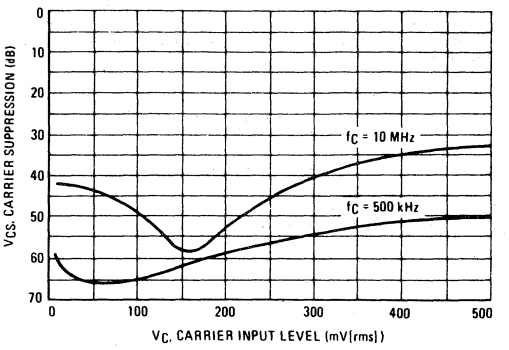


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

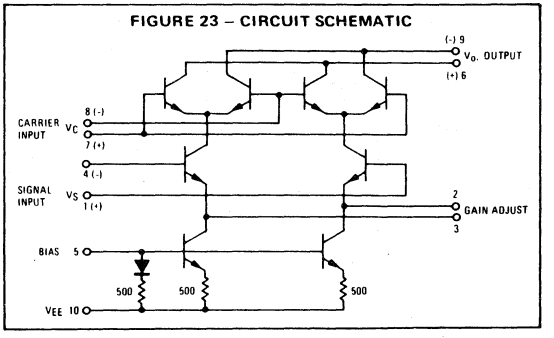
The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

FIGURE 23 – CIRCUIT SCHEMATIC



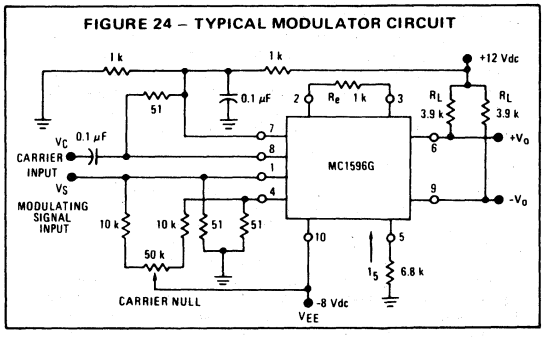
Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 24 – TYPICAL MODULATOR CIRCUIT



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, ...

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

APPLICATIONS INFORMATION (continued)

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

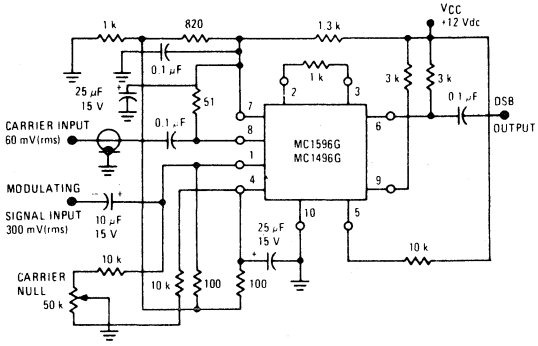


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

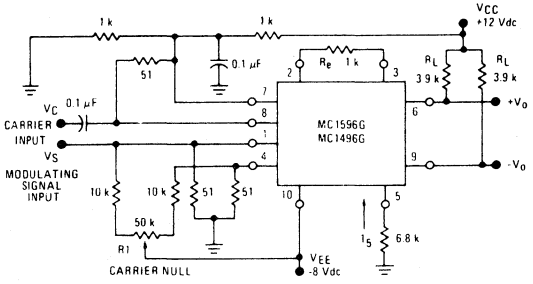


FIGURE 28 – AM MODULATOR CIRCUIT

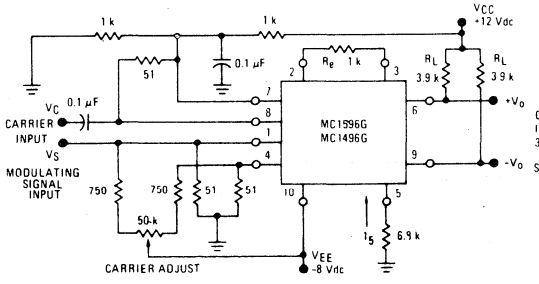
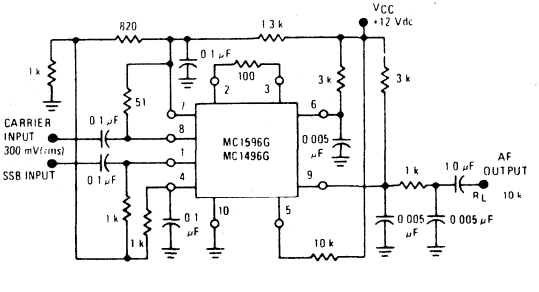
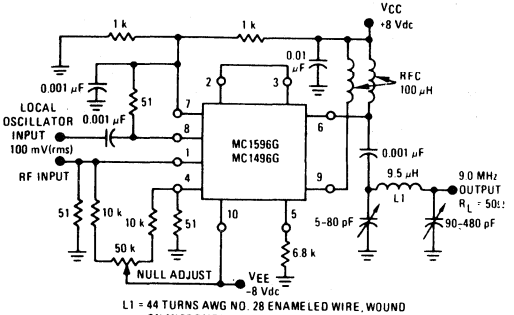


FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)



TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)



L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

FIGURE 31 – LOW-FREQUENCY DOUBLER

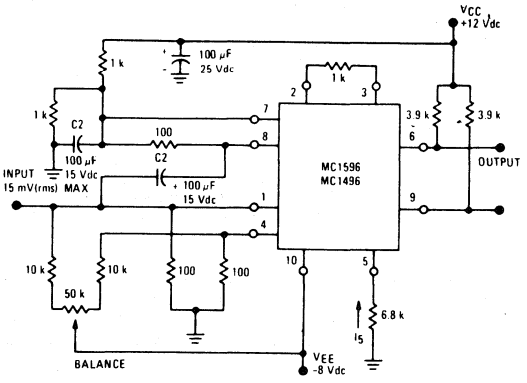
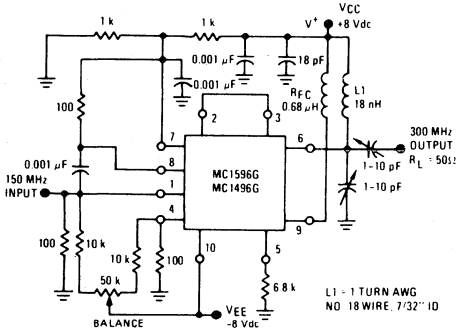
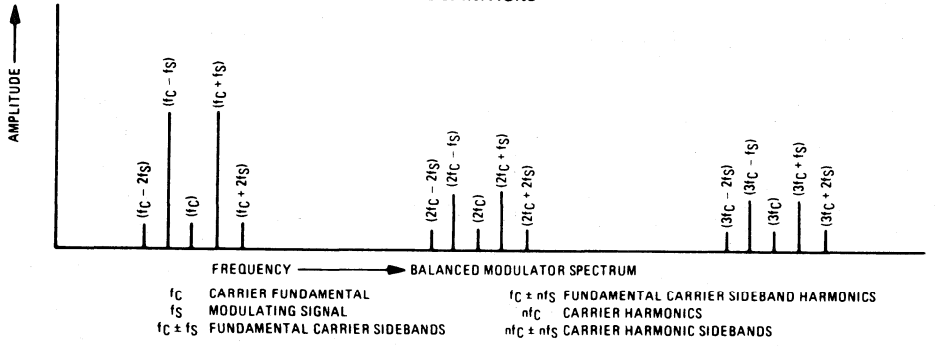


FIGURE 32 – 150 to 300 MHz DOUBLER



L1 = 1 TURN AWG NO. 18 WIRE, 7/32" ID

DEFINITIONS



f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

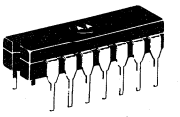
Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

MONOLITHIC QUAD
OPERATIONAL AMPLIFIER
INTEGRATED CIRCUIT
EPITAXIAL PASSIVATED

MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301P contains four independent amplifiers — making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range — -40 to +85°C
- Single-Supply Operation — +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 4.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 2000 V/V typical



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 — EQUIVALENT CIRCUIT

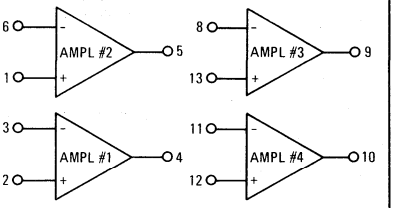
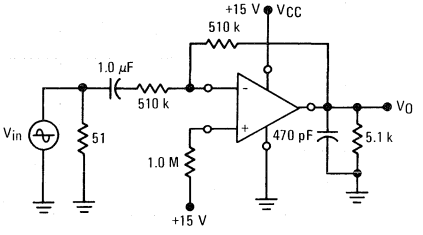


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE



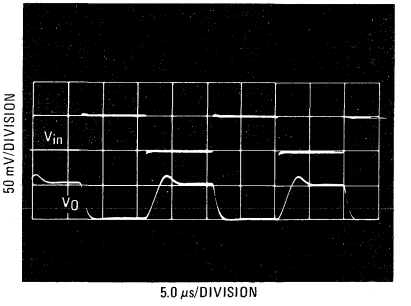


FIGURE 3 — INVERTING AMPLIFIER

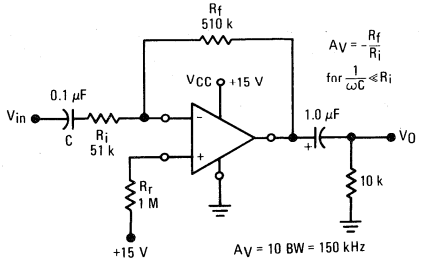
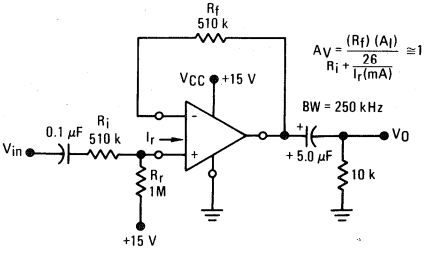


FIGURE 4 — NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+28	Vdc
Noninverting Input Current	I_r	5.0	mA
Sink Current	I_{sink}	50	mA
Source Current	I_{source}	50	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig.No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C -40°C ≤ T_A ≤ +85°C	5		A_{vol}	 1000 –	 2000 1600	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6	1	 I_{DO} I_{DG}	 – –	 6.9 7.8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C -40°C ≤ T_A ≤ +85°C	7	2	I_{IB}	 – –	 50 100	 300 –	nAdc
Current Mirror Gain (I_r = 200 μAdc)	7	3	A_I	0.80	0.98	1.16	A/A
Current Mirror Gain Drift -40°C ≤ T_A ≤ +85°C				 –	 ±2.5	 –	%
Output Current Source Capability (V_{OH} = 0.4 Vdc) (V_{OH} = 9.0 Vdc) Sink Capability (V_{OL} = 0.4 Vdc)	8		 I_{source} I_{sink}	 3.0 – 0.5	 10 7.0 0.87	 – – –	mAdc
Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven)	6		 V_{OH} $V_{OL(inv)}$ $V_{OL(non)}$	 13.5 – –	 14.2 0.03 0.6	 – 0.1 –	Vdc
Input Resistance (Inverting input only)			R_{in}	0.1	1.0	–	Meg Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth		4	BW	–	4.0	–	MHz
Phase Margin		4	ϕm	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)			PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

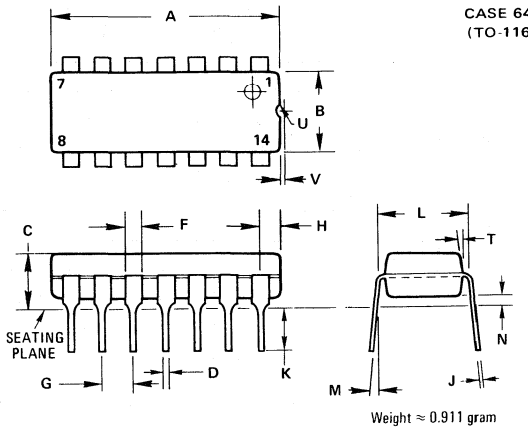
Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

NOTES:

1. The quiescent current drain will increase approximately 0.3 mA for each inverting or noninverting input that is grounded.
2. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
3. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
4. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.

OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 646
(TO-116)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.03	18.79	.710	.740
B	6.09	6.60	.240	.260
C	4.06	4.57	.160	.180
D	.38	.51	.015	.020
F	1.02	1.65	.040	.065
G	2.54 BSC		.100 BSC	
H	1.32	1.83	.052	.072
J	.23	.36	.009	.014
K	2.92	3.43	.115	.135
L	7.37	7.87	.290	.310
M	–	10°	–	10°
N	.64	.89	.025	.035
T	7° TYP		7° TYP	
U	.64 RAD		.025 RAD	
V	.13	.38	.005	.015

Dimension "L" to lead centerline when formed parallel.

Weight ≈ 0.911 gram

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN

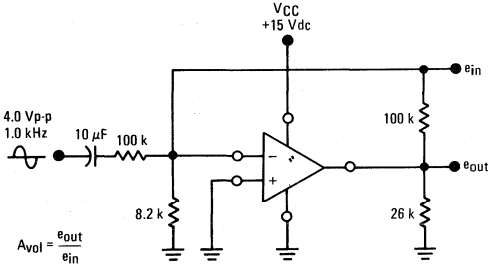
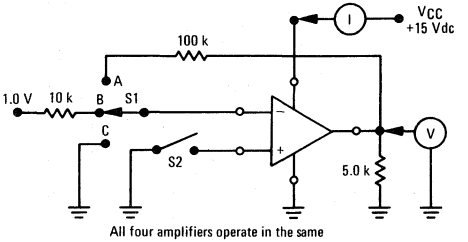


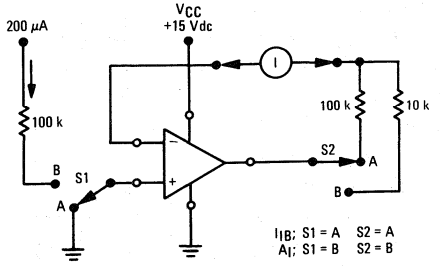
FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



All four amplifiers operate in the same configuration simultaneously.

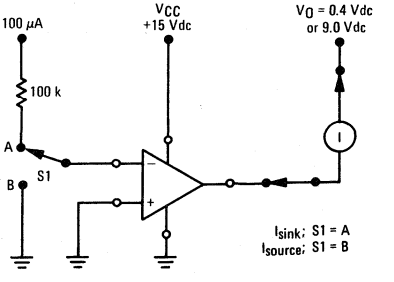
I_{DO}; S1 = A S2 = OPEN
I_{DG}; S1 = A S2 = CLOSED
V_{OH}(–); S1 = C S2 = CLOSED
V_{OL}(–); S1 = B S2 = CLOSED
V_{OL}(+); S1 = A S2 = CLOSED

FIGURE 7 – INPUT BIAS CURRENT AND CURRENT MIRROR GAIN



I_{IB}; S1 = A S2 = A
A_I; S1 = B S2 = B

FIGURE 8 – OUTPUT CURRENT



I_{sink}; S1 = A
I_{source}; S1 = B

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

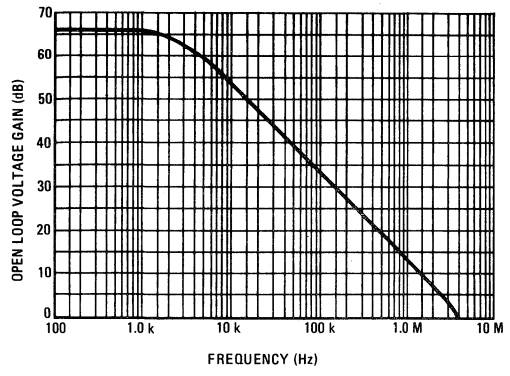


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

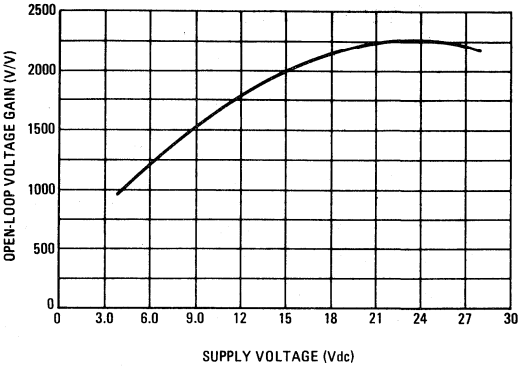


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

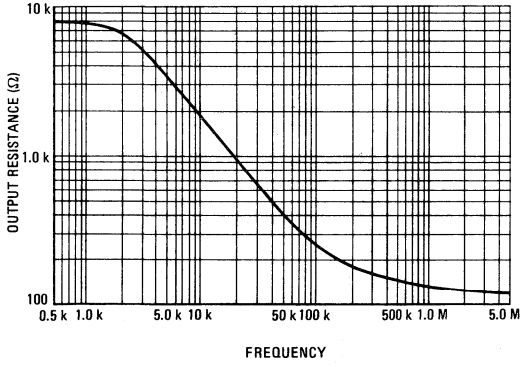


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

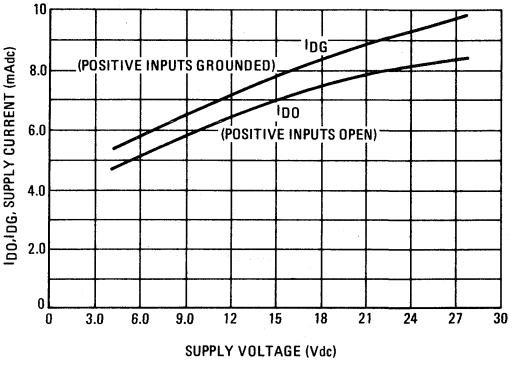


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

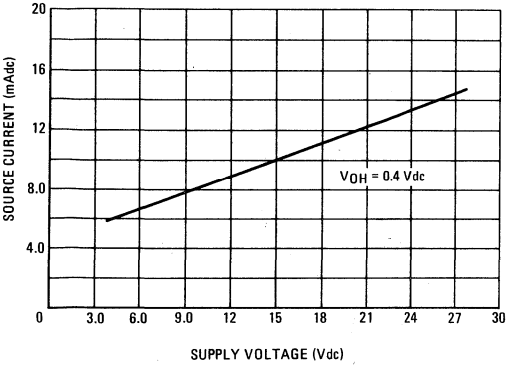
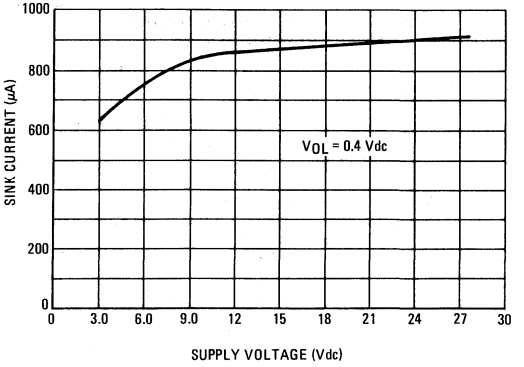


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE

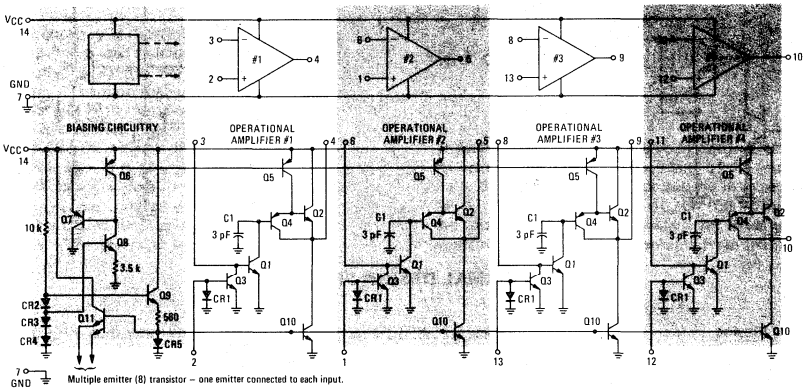


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page. No external compensation is required.

FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_r, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_r also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

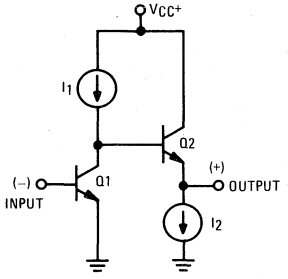
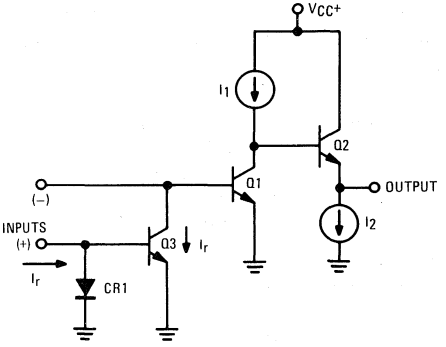


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

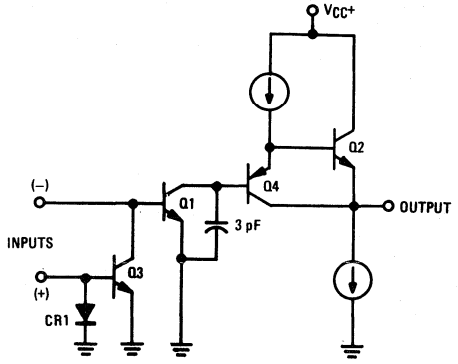
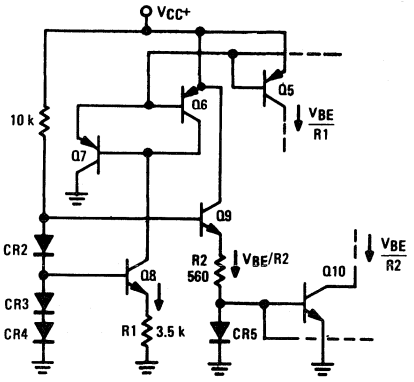


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 3 and 4)

   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 20)

   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 10 μA and 200 μA) the output dc level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_I)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_I\right)\phi$$

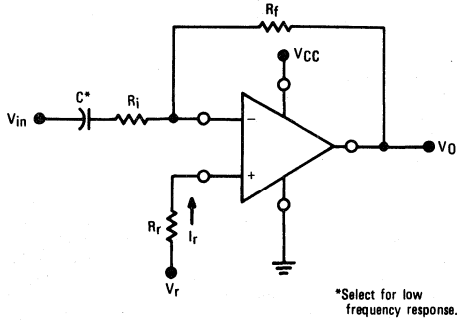
   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_I is the current mirror gain.

2. Gain Determination

   A. Inverting Amplifier

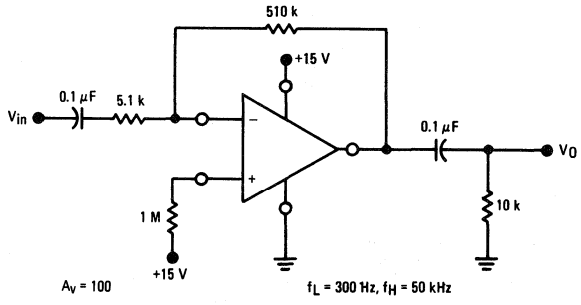
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH A_V = 100 AND $V_r = V_{CC}$



A_V = 100

f_L = 300 Hz, f_H = 50 kHz

NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

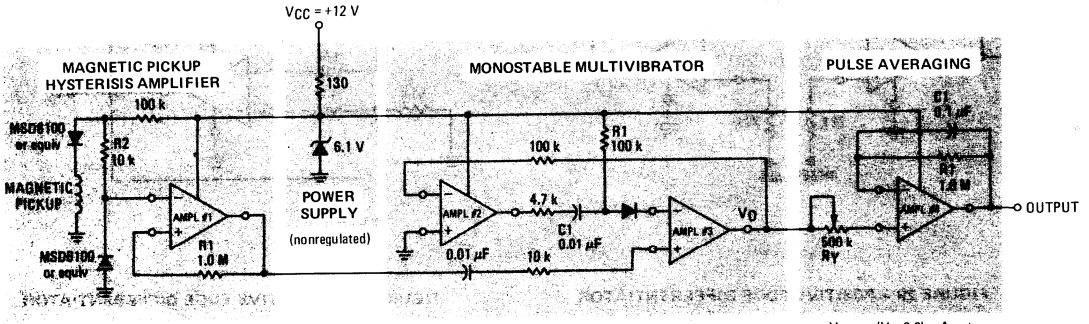
The MC3301P may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_v = \frac{(R_f)(A_I)}{R_i + \frac{26}{I_r\,(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT



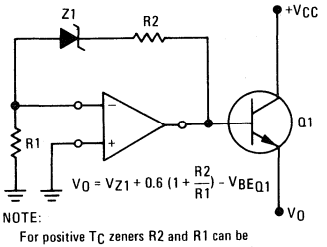
Hysterisis Voltage for Switching

$$V_H = \frac{A_I R2}{R1}\ (V_{CC} - 1.6)$$

Timing Interval: $t \approx 0.7\ R1\ C1$

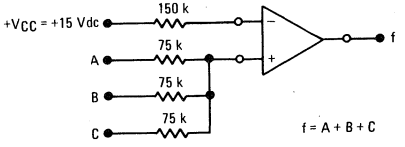
$$V_{p\text{-}p} \cong \frac{(V_O - 0.6) \cdot A_I \cdot t}{R_V C1}$$

FIGURE 23 – VOLTAGE REGULATOR



NOTE:
For positive T_C zeners R2 and R1 can be selected to give 0 T_C output.

FIGURE 24 – LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

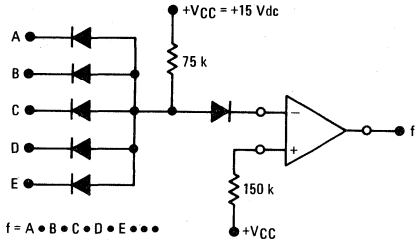


FIGURE 26 – LOGIC "NOR" GATE

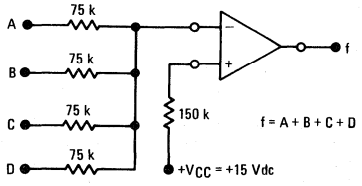


FIGURE 27 – R-S FLIP-FLOP

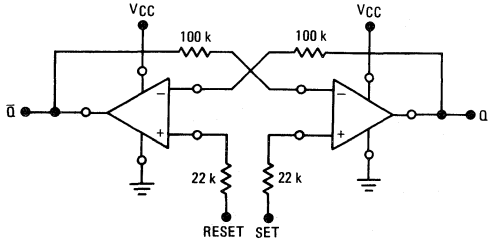


FIGURE 28 – ASTABLE MULTIVIBRATOR

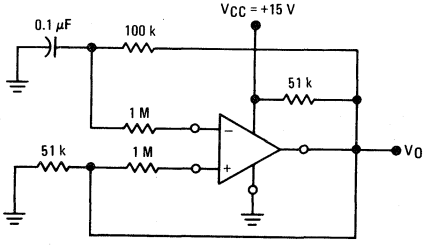


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

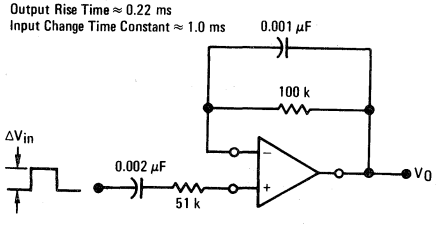
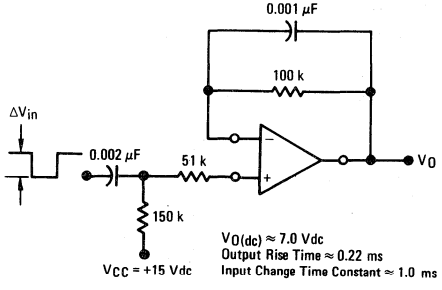


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



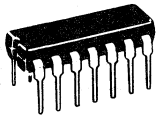
QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302 contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

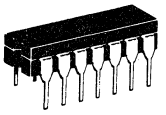
- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = $\pm V_{CC}$
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – 700 μA typical @ V_{CC} +5.0 to +28 Vdc
- Outputs can be Connected to Give the Implied AND Function

QUAD COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to +V_{CC}	Vdc
Power Dissipation @ T_A = 25°C	P_D		
Plastic Package – P Suffix		1.2	Watts
Derate above 25°C		10	mW/°C
Ceramic Package – L Suffix		1.2	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A		°C
Plastic Package		-40 to +85	
Ceramic Package		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Requires an external resistor, R_L, to limit current below maximum rating.

Note 2. If either (+) or (–) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

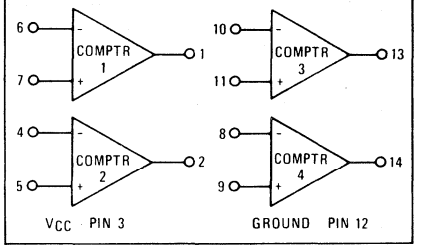
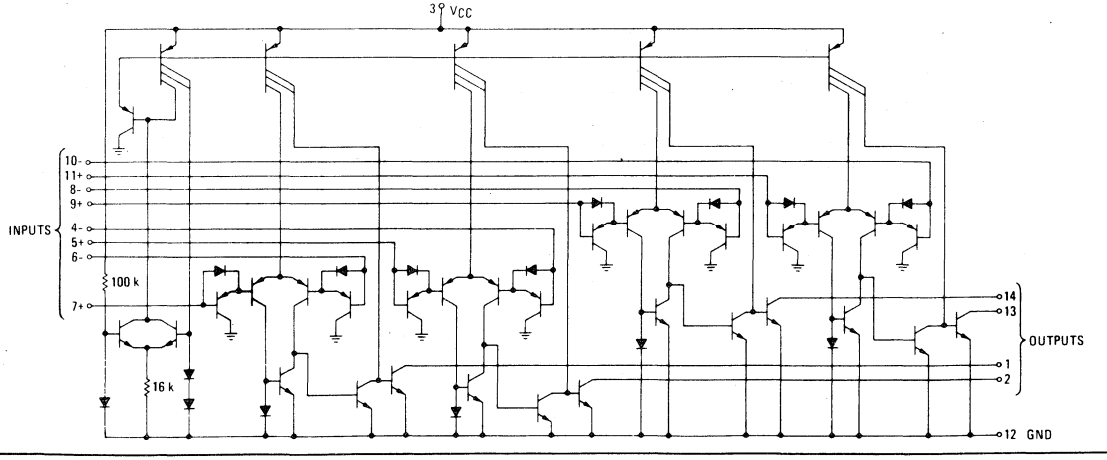
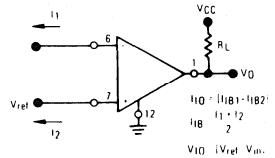
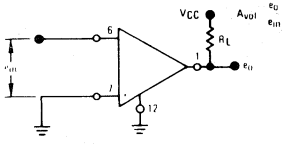
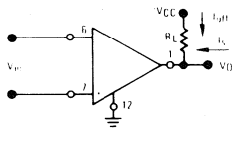
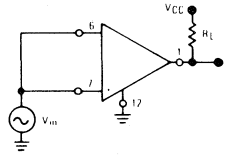
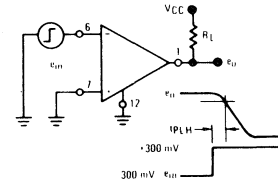
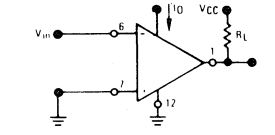


FIGURE 2 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Characteristic Definitions (1/4 Circuit Shown)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage (V_{ref} = 1.2 Vdc) (T_A = +25°C) (T_A = -40 to +85°C)	V_{IO}	– –	3.0 –	20 40	mVdc
	Input Offset Current	I_{IO}	–	3.0	–	nAdc
	Input Bias Current (T_A = +25°C) (T_A = -40 to +85°C)	I_{IB}	– –	30 –	500 1000	nAdc
	Voltage Gain (T_A = +25°C, R_L = 15 kΩ)	A_{vol}	2,000	30,000	–	V/V
	Transconductance	gm	–	2.0	–	mhos
	Input Differential Voltage Range	V_{IDR}	±V_{CC}	–	–	Vdc
	Output Leakage Current (Output Voltage High)	I_{OL}	–	–	1.0	μAdc
	Output Voltage - Low Logic State (I_s = 2.0 mA, V_{CC} = +5.0 to +28 Vdc)	V_{OL}	–	150	400	mVdc
	Output Sink Current (V_{CC} = +5.0 Vdc) (T_A = +25°C, V_{OL} = 400 mV) (T_A = -40 to +85°C, V_{OL} = 800 mV)	I_{sink}	– 2.0	6.0 –	– –	mAdc
	Input Common-Mode Voltage Range (V_{CC} = +28 Vdc)	V_{ICR}	0-26	–	–	Volts
	Common-Mode Rejection Ratio	CMRR	–	60	–	dB
	Propagation Delay Time For Positive and Negative-Going Input Pulse	$t_{PHL/LH}$	–	2.0	–	μs
	Slew Rate (R_L = 15 kΩ)	SR	– –	200 50	– –	V/μs
	Power Supply Current (Total of four comparators) (I_s = 0, V_{CC} = +5.0 to +28 Vdc)	I_{CC} I_{EE}	–	0.7	1.5	mAdc

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A +25°C (each comparator) unless otherwise noted.)

FIGURE 3 – INPUT OFFSET VOLTAGE

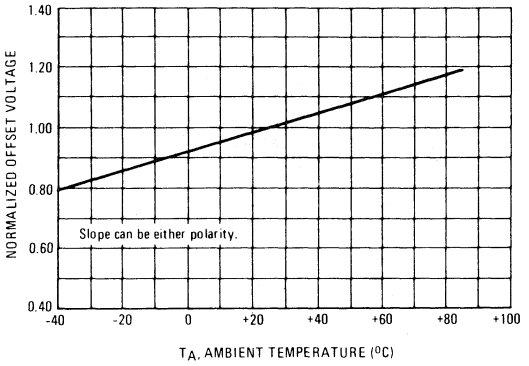


FIGURE 4 – OFFSET BIAS CURRENT

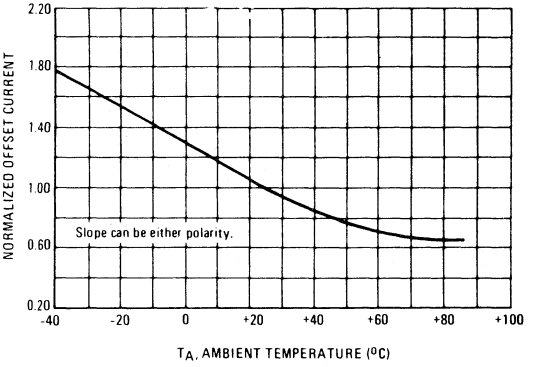
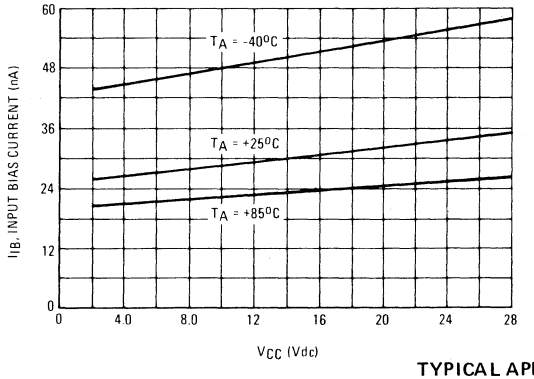


FIGURE 5 – INPUT BIAS CURRENT



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

TYPICAL APPLICATIONS

FIGURE 6 – FREE-RUNNING SQUARE-WAVE OSCILLATOR

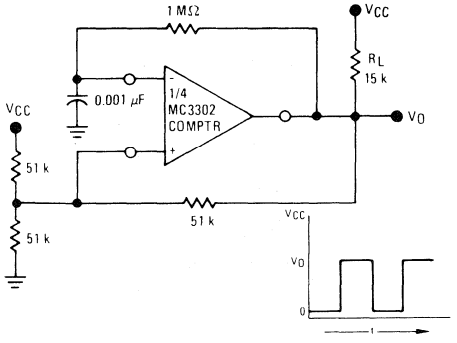
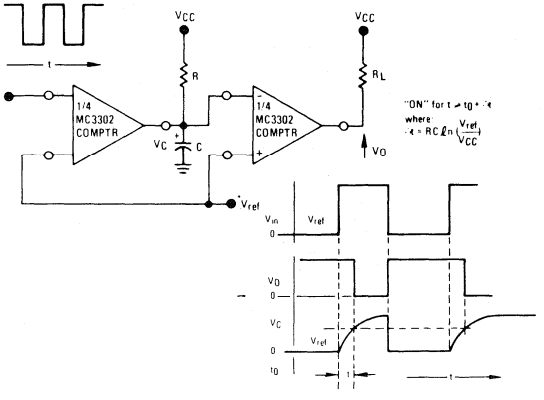
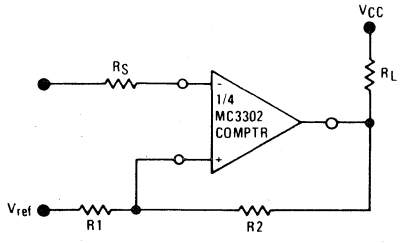


FIGURE 7 – TIME DELAY GENERATOR



TYPICAL APPLICATIONS (continued)

FIGURE 8 – COMPARATOR WITH HYSTERESIS

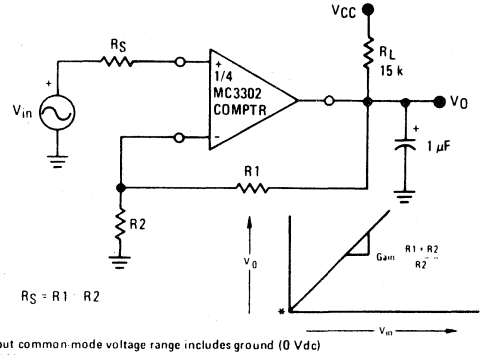


$R_S = R1 \parallel R2$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\ Low})\,R1}{R1 + R2 + R_L}$$

FIGURE 9 – THE COMPARATOR AS AN OPERATIONAL AMPLIFIER

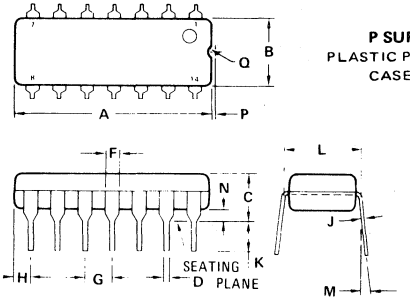


$R_S = R1 \parallel R2$

*Input common-mode voltage range includes ground (0 Vdc) and V_O can go to approximately 0 Vdc.

OUTLINE DIMENSIONS

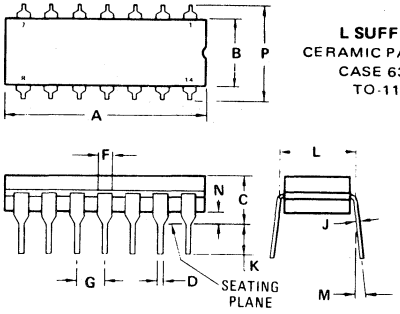
P SUFFIX
PLASTIC PACKAGE
CASE 646



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	L02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

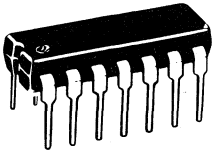
AUTOMOTIVE VOLTAGE REGULATOR

. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

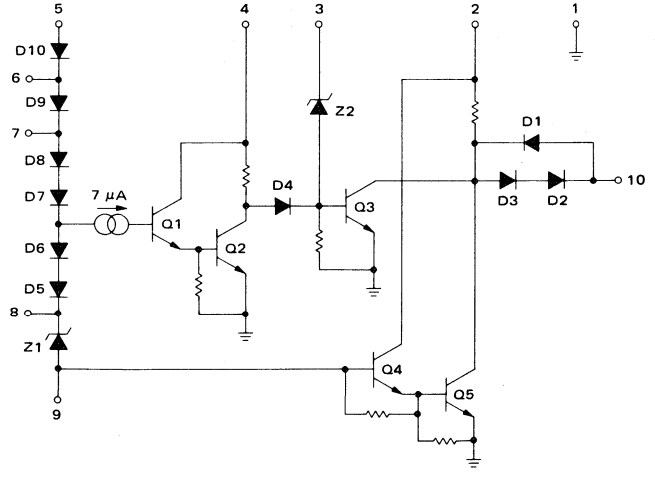
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

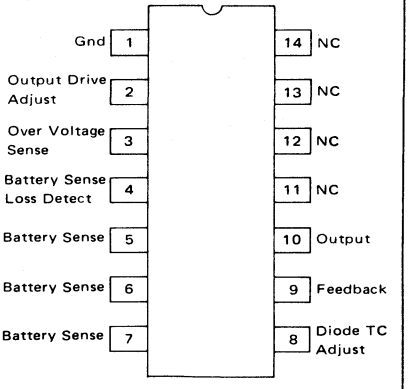


P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5, 6, or 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	^oC
Operating Temperature Range	T_A	-40 to +85	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC

ELECTRICAL CHARACTERISTICS (T_A = 25^{o}C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7.9	–	8.8	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	–	13.3	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	–	12.6	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	–	11.8	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	–	–	400	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq$ 400 μA, Figure 2)	V_4	1.3	–	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	–	–	400	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq$ 400 μA, Figure 2)	V_3	6.7	–	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 (I_2 = 10 mA, Figure 3)	V_2	1.9	–	2.4	V
Low State Output Voltage at Pin 10 (I_3 = 12 mA, I_2 = 120 mA, Figure 4)	V_{10}	–	–	0.7	V

TEST CIRCUITS

FIGURE 1

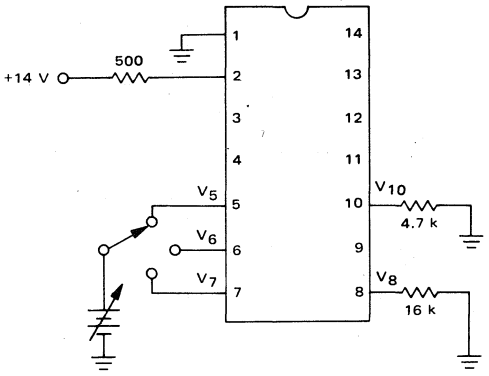


FIGURE 2

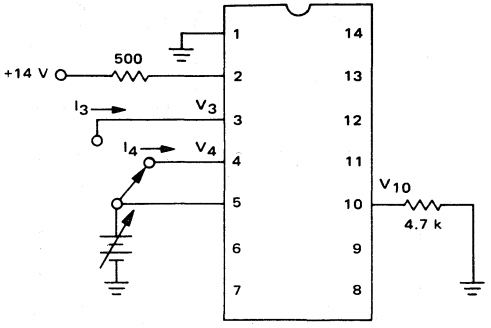


FIGURE 3

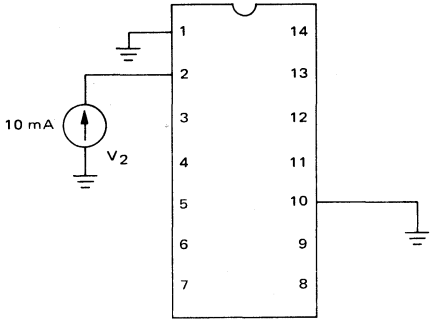


FIGURE 4

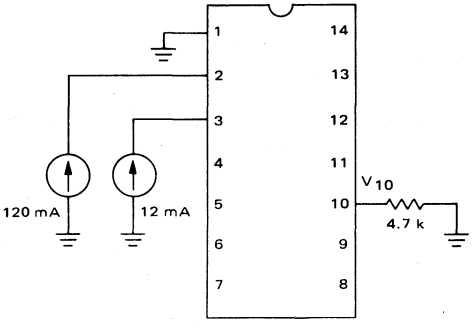
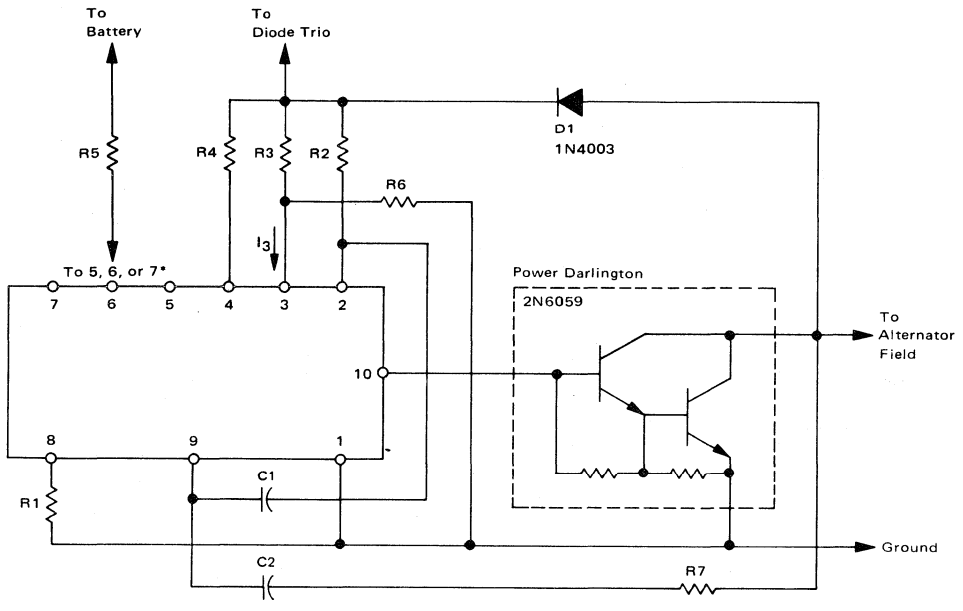


FIGURE 5 – APPLICATION CIRCUIT



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is -2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have -2.0 mV for Q5, -2.0 mV for Q4, +3.0 mV for Z1, -8.0 mV for D5 thru D8, and an additional -2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately -9.0 mV/°C to -13 mV/°C depending on the number of the diodes in the diode string that are utilized.

APPLICATIONS CIRCUIT INFORMATION

(See Figure 5)

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as defined by the following equation:

$$V_{reg} = \left(1 + \frac{R5}{R1}\right) 8.4 + \left(n + \frac{R5}{5K}\right) (0.7)$$

n = number of diodes used in diode string
$(4 \leqslant n \leqslant 6)$

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the maximum overvoltage.

$$\text{Maximum overvoltage} \cong \frac{R3 + R6}{R6} \quad (7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

C1, C2 Used for compensation (Approximately 0.01 μF)

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

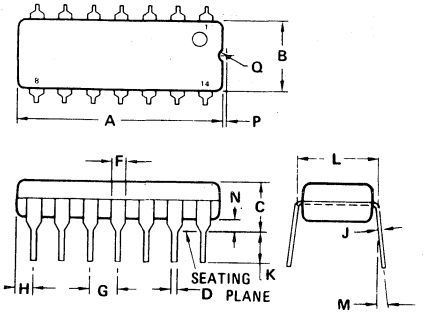
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 646
$R_{\theta JA}$ = 100°C/W (Typ)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

MC3333

VARI-DWELL IGNITION CIRCUIT

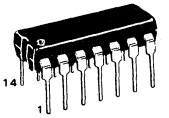
. . . designed for use in conjunction with a flux averaging sensor and a high energy ignition coil to provide regulated current pulses to the coil from information supplied by the sensor.

- Wide Supply Voltage Operating Range (4 to 24 V)
- Externally Adjustable Overvoltage Shutdown
- Externally Adjustable Dwell Time and Spark Energy
- Extremely Stable Output Current Pulses
- Variable Input Threshold Compensates for Low Supply Voltage Conditions
- Low Static Current Drain
- Also Available in Flip-Chip (MCCF3333) and Standard Chip (MCC3333) Form

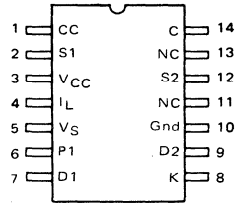
VARI-DWELL IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646



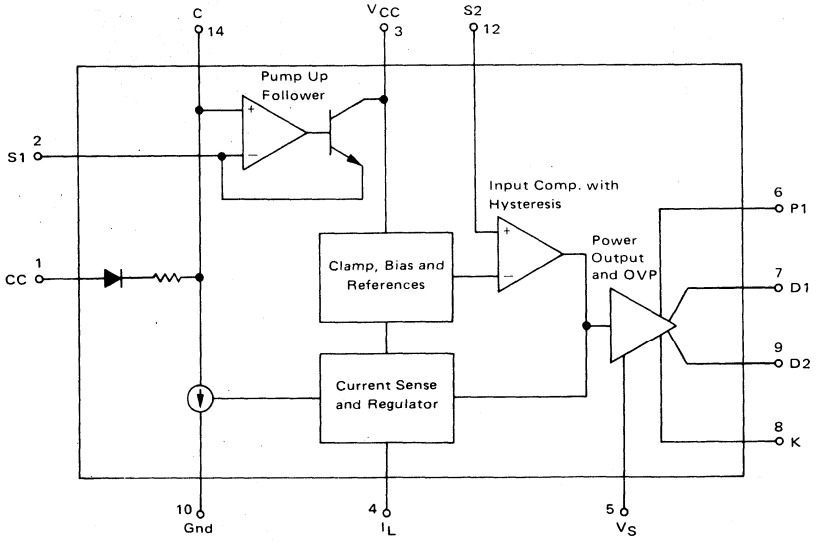
PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3333P	-40 to +85	Plastic DIP

FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Steady State (Through 400 Ω, see Fig. 2)	V_{CC}	24	Vdc
Transients of 300 ms or less		90	
Peak Output Sink Current	$I_{S(PEAK)}$		A
Transients of 300 ms or less		1.3	
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, T_A = 25°C unless otherwise specified; Figure 2.)

Characteristic	Symbol	Pin(s) Under Test	S1	S2	S3	S4	S5	S6	Min	Typ	Max	Unit
Current Drain	I_D	3	A	A	A	A	A	A	8.0	15	25	mA
Pre-Driver On	V_{P1}	6	A	A	A	A	A	A	–	.90	2.0	V
D1, D2 Output On	$V_{D1, D2}$	7&9	A	A	A	A	A	A	–	110	500	mV
Kelvin Contact	V_K	8	A	A	A	A	A	A	–	40	200	mV
CC Charge Circuit	V1	1	B	A	A	A	A	E	700	800	900	mV
S1 Follower	V_{S1}	2	A	B	A	A	A	C	1.4	1.6	1.8	V
C Clamp High	V_c	14	A	A	A	A	A	D	–	8.4	8.8	V
S2 Turn On (measure V_{S2} ramp value at P1 switch point.)	V_{S2}	12	A	A	A	A	B	A	1.6	1.9	2.1	V
Overvoltage Protection	V_S	5	A	A	A	B	C	A	8.0	9.1	10	V
Current Limit Trip	V_{IL}	4	A	A	B	A	C	B	150	180	220	mV

FIGURE 2 – TEST CIRCUIT

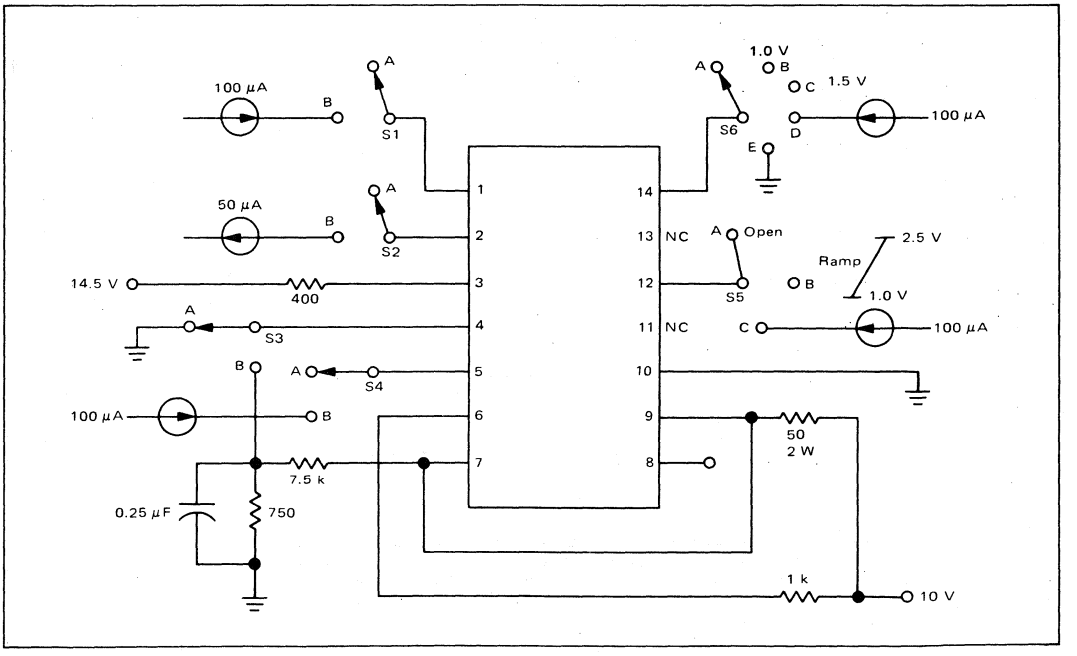
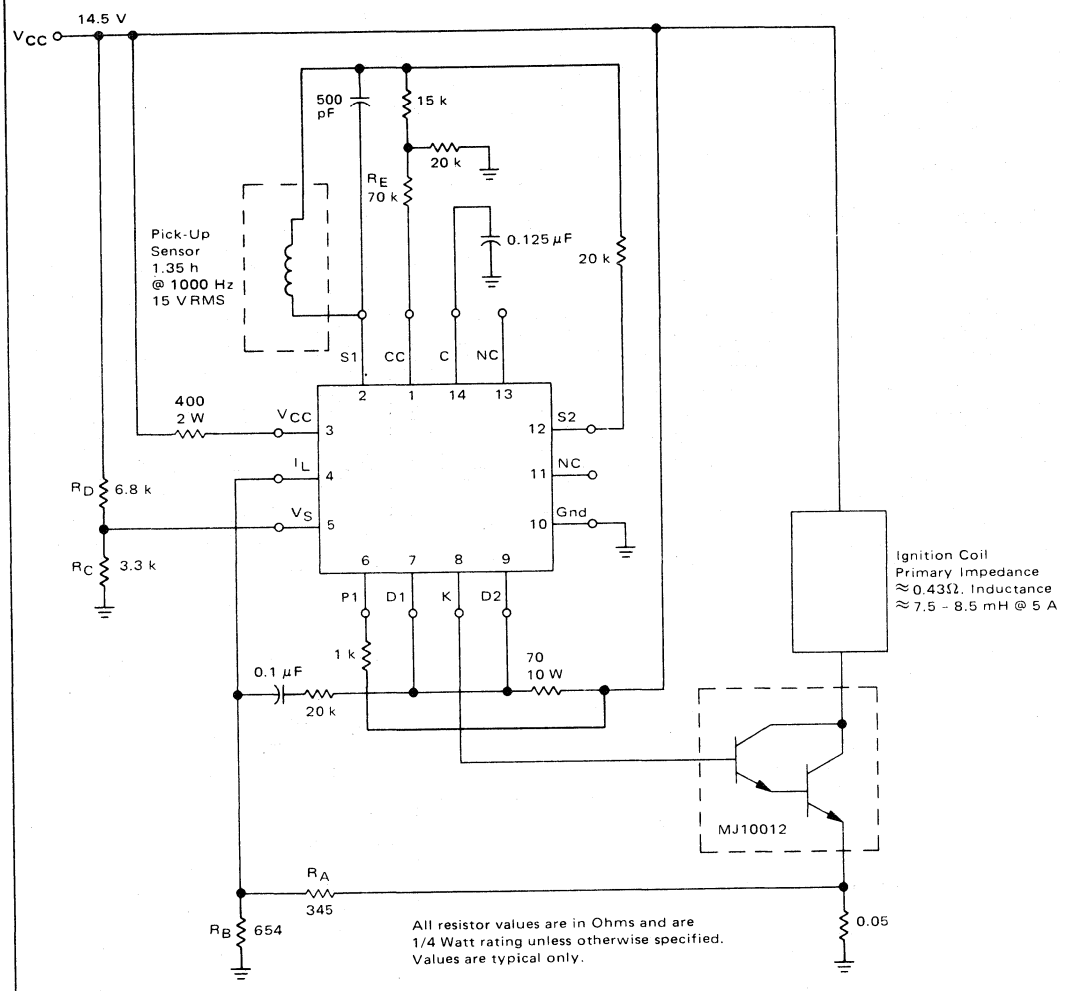


FIGURE 3 – TYPICAL APPLICATION CIRCUIT



Notes:

1. The ratio of R_A to R_B controls the ignition coil regulated current:

$$I_{COIL} \approx 3.6 \left(\frac{R_A + R_B}{R_B} \right) \qquad R_A + R_B \approx 1\ k\Omega$$

2. The ratio of R_D to R_C sets the over-voltage shutdown point with respect to B+.

$$B+_{overvoltage} \approx 8 \left(\frac{R_C + R_D}{R_C} \right) \qquad R_C + R_D \approx 10\ k\Omega$$

3. R_E is active region dwell control. R_E = 70 kΩ results in output current limit time of approximately 10% at 1000 RPM (with respect to one distributor cycle in an 8 cylinder engine). Values less than 70 kΩ lengthen this limit time and values higher shorten this limit time.
4. The 0.1 µF capacitor at pin 4 may be eliminated and stability maintained. A readjustment of the R_A and R_B resistors will be required.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

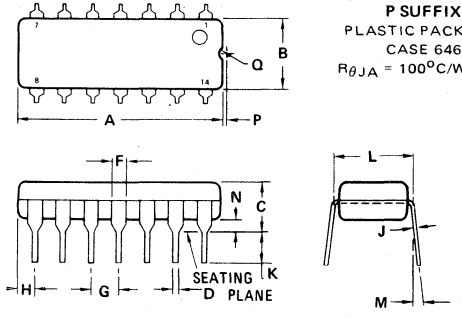
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

OUTLINE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 646
$R_{\theta JA}$ = 100°C/W(Typ)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

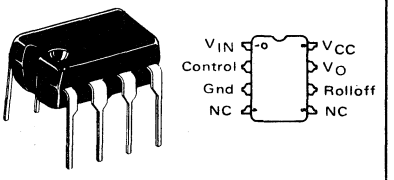
MC3340

ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual In-Line Package
- Formerly MFC6040 in Case 643A Package

ELECTRONIC ATTENUATOR

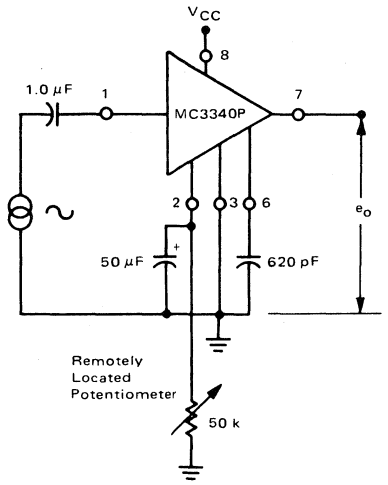
SILICON MONOLITHIC INTEGRATED CIRCUIT

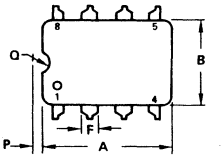


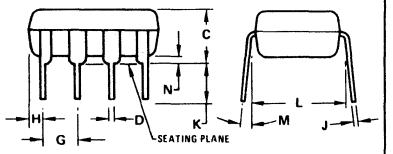
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	20	Vdc
Power Dissipation @ T_A = 25°C	1.2	Watts
Derate above T_A = 25°C	10	mW/°C
Operating Ambient Temperature Range	0 to +75	°C

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL







NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

CASE 626-03

ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV (RMS), f = 1.0 kHz, R1 = 0, V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

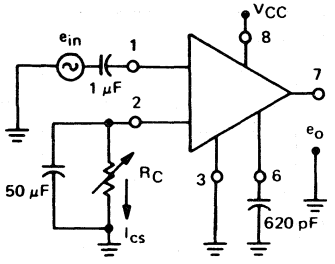
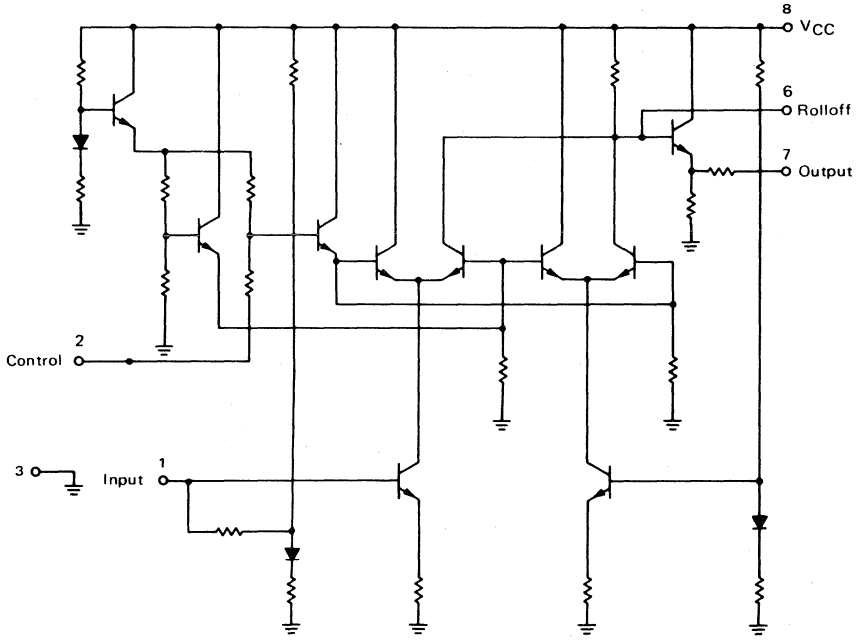
Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	9.0	–	18	Vdc
	Control Terminal Sink Current (e_{in} = 0)	–	–	2.0	mAdc
	Maximum Input Voltage	–	–	0.5	V(RMS)
	Voltage Gain	11	13	–	dB
	Attenuation Range (R_C = 33 k ohms)	70	90	–	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mV (RMS), $e_o = A_v \times e_{in}$)	–	0.6	1.0	%

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

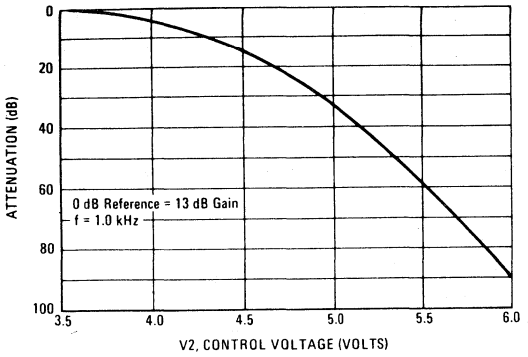


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

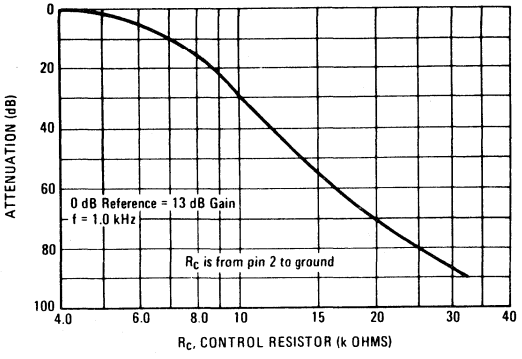


FIGURE 5 – FREQUENCY RESPONSE

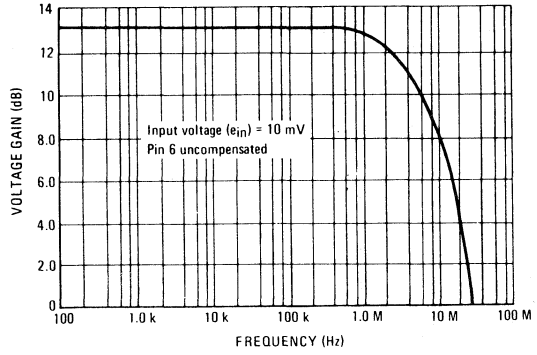


FIGURE 6 – OUTPUT VOLTAGE SWING

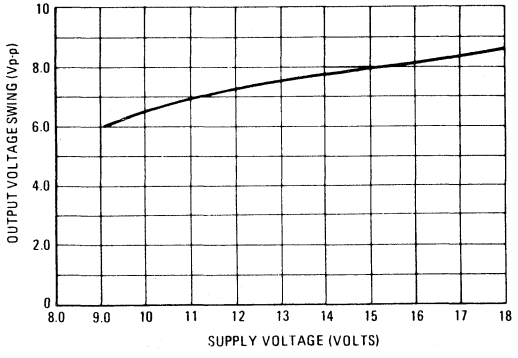
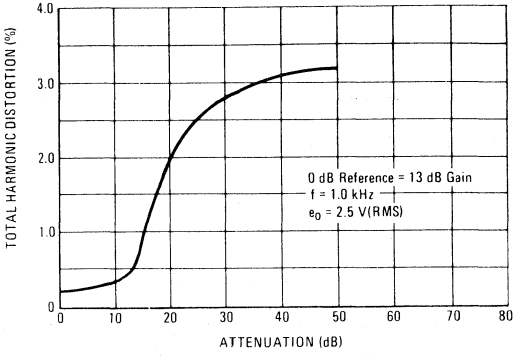


FIGURE 7 – TOTAL HARMONIC DISTORTION

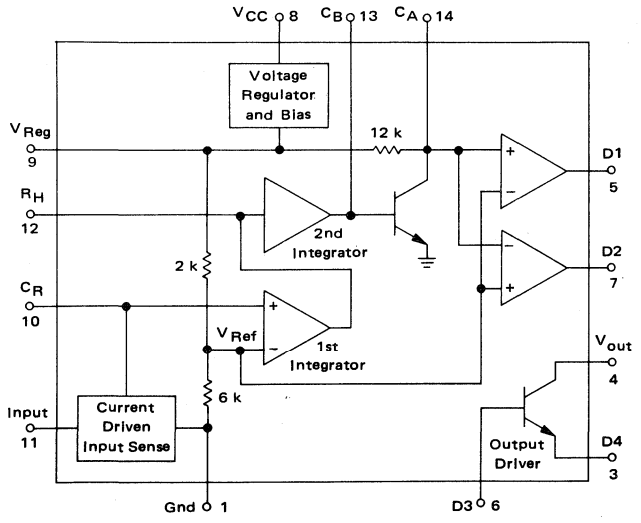


PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor (R_R) and capacitor (C_R). Hysteresis is adjustable and determined by an external resistor (R_H).

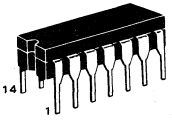
- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

FIGURE 1 – CIRCUIT BLOCK DIAGRAM



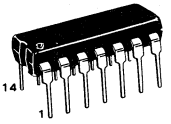
PROGRAMMABLE FREQUENCY SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

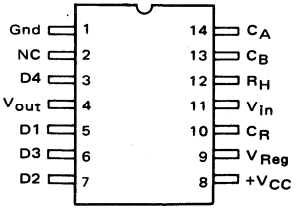


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO - 116

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	24	Vdc
Peak Input Current	I_I	10	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +15 Vdc unless otherwise specified)

Characteristic	Test Ckts	Symbol	Min	Typ	Max	Unit
Supply Current	2	I_D	–	2.5	4.0	mA
Trigger Reset Voltage	3					Vdc
I_{in} = 200 μA		V_{CR1}	0.25	–	–	
I_{in} = 600 μA		V_{CR2}	–	–	0.25	
Regulator Output Voltage	4	V_{Reg}	4.0	4.5	5.0	Vdc
Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$	5	V_{TCR}	0.739	0.750	0.761	V/V
Hysteresis Sink Current	6	I_H	100	400	–	μA
Second Comparator Output	7					
D1 Leakage		I_{D1L}	–	–	100	nA
D2 Source		I_{D2S}	100	250	–	μA
D1 Source		I_{D1S}	100	200	–	μA
D2 Leakage		I_{D2L}	–	–	100	nA
Output Driver Gain I_C = 5.0 mA	8	h_{FE1}	50	100	–	–
Output Driver Voltage Standoff I_D = 5.0 mA	9	BV_{CEO}	25	30	–	Vdc
Integrator Transistor Gain $h_{FE2} = \Delta I_C/\Delta I_B$, I_{C1} = 0.4 mA, I_{C2} = 0.6 mA	10	h_{FE2}	50	200	300	–

TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

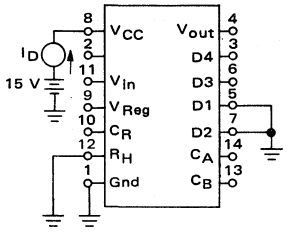
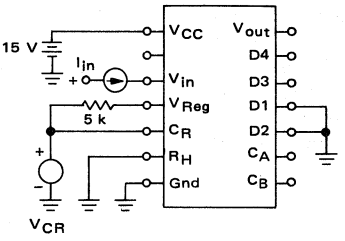


FIGURE 3 – TRIGGER RESET VOLTAGE



I_{in} = 200 μA, $V_{CR} \geq 0.25$ V

I_{in} = 600 μA, $V_{CR} \leq 0.25$ V

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

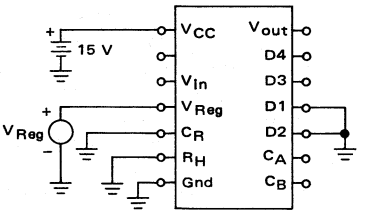
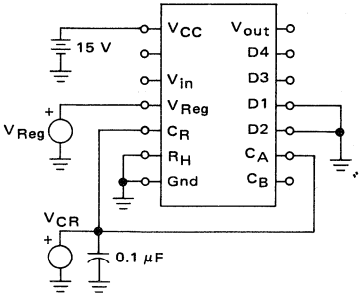


FIGURE 5 – THRESHOLD VOLTAGE RATIO



$V_{TCR} = V_{CR}/V_{Reg}$

FIGURE 6 – HYSTERESIS SINK CURRENT

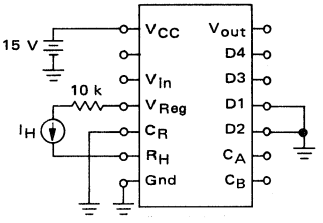
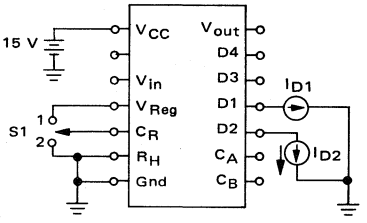


FIGURE 7 – I_{D1L}/I_{D2S}, I_{D2L}/I_{D1S}



I_{D1L}/I_{D2S} – S1 in position 1

I_{D2L}/I_{D1S} – S1 in position 2

FIGURE 8 – OUTPUT DRIVER GAIN

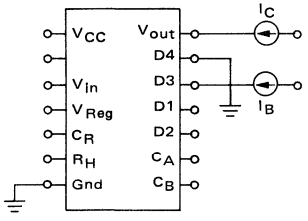


FIGURE 9 – BV_{CEO} OF OUTPUT TRANSISTOR

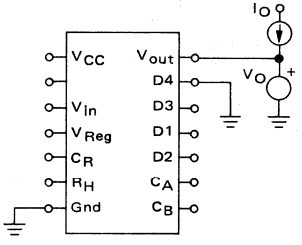
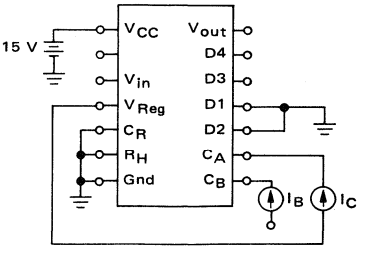


FIGURE 10 – INTEGRATOR TRANSISTOR GAIN



APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor C_R. This establishes the initial ramp voltage (V_{sat}) and allows initiation of a new voltage ramp after each positive transistion of the input waveform.

The voltage, V_{CR}, ramps from V_{sat} to the final value, V_{Reg}, charging through R_R.

If V_{CR} is never allowed to reach V_{Ref} due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor C_{AB} is allowed to charge through the 12 kΩ resistor until V_{CA} is greater than V_{Ref}. At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If V_{CR} is allowed to ramp above V_{Ref} before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor C_{AB} keeping V_{CA} low with respect to V_{Ref}.

V_{CA} will always be low with respect to V_{Ref} if the time from reset C_R to $V_{CR} = V_{Ref}$ is less than the time from reset C_{AB} to $V_{CA} = V_{Ref}$.

Resistor R_H provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the R_H resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is
$T1 = R_H \parallel R_R\, C_R$. If R_H is omitted then
$T1 = R_R\, C_R$.

The second integrator time constant is
$T2 = (12\text{ k})\,(h_{FE2})\,(C_{AB})$.

$$f1 = \text{Switch Point frequency} \cong \frac{1}{1.39\, R_R\, C_R}$$

$$f2 = \text{Hysteresis Switch Point frequency} \approx \frac{1}{R_R \parallel R_H\, C_R \ln\left[\frac{R_H}{0.25\, R_H - 0.75\, R_R}\right]}$$

FIGURE 11 – TYPICAL APPLICATION

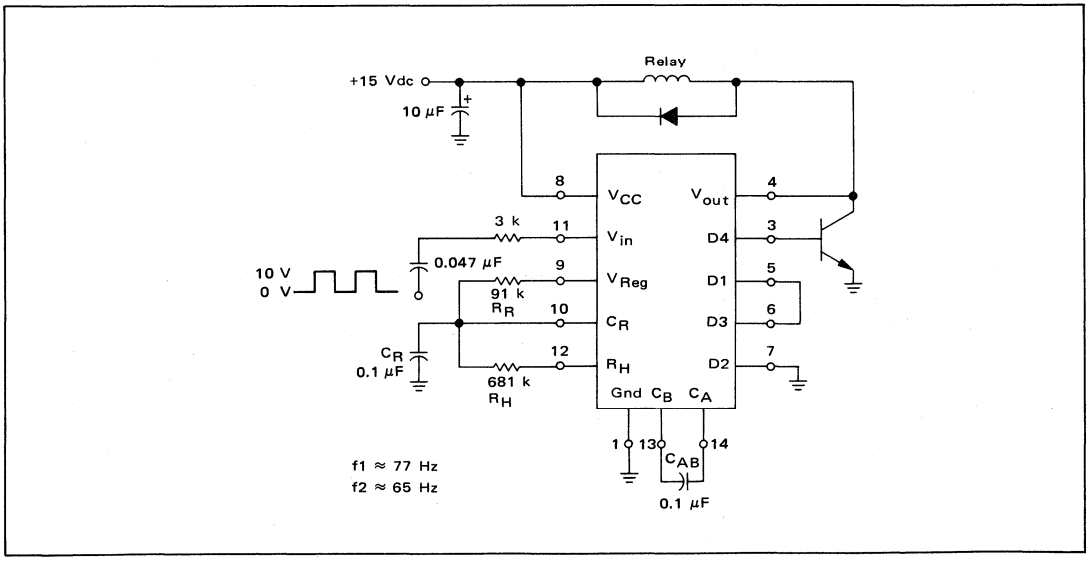
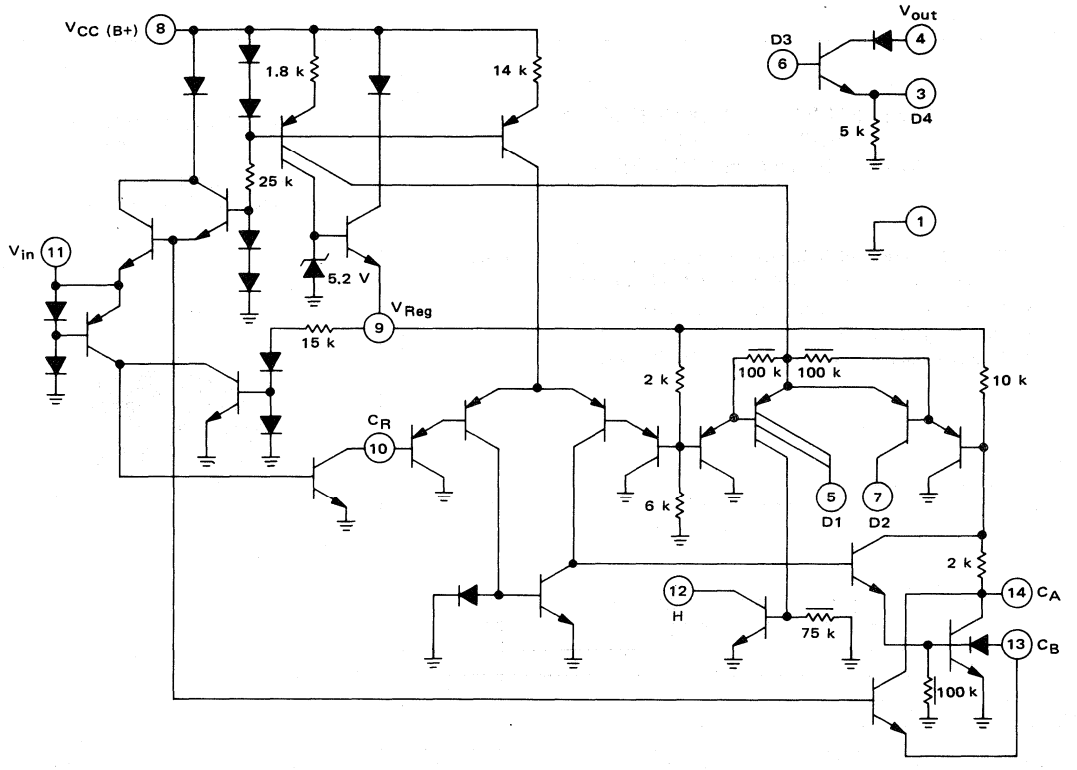
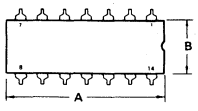


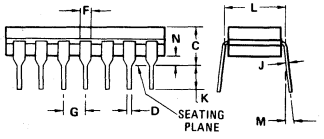
FIGURE 12 – CIRCUIT SCHEMATIC



OUTLINE DIMENSIONS

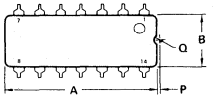


L SUFFIX
CERAMIC PACKAGE
CASE 632-03
$R_{\theta JC}$ = 100°C/W (Typ)



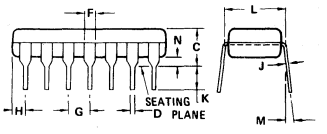
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.45	1.60	0.057	0.063
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030

NOTE:
1. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



P SUFFIX
PLASTIC PACKAGE
CASE 646-03
$R_{\theta JC}$ = 100°C/W (Typ)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

MC3346
MC3386

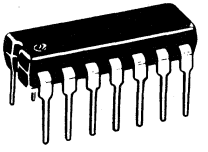
ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346P and MC3386P are designed for general-purpose, low power applications for consumer and industrial designs.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified – 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

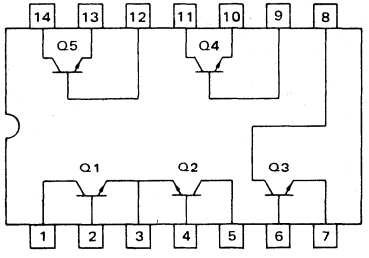
GENERAL-PURPOSE TRANSISTOR ARRAY

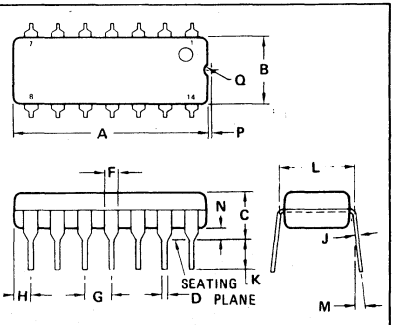
SILICON MONOLITHIC INTEGRATED CIRCUIT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/°C mW/°C
Operating Junction Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C





NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3346P			MC3386P			Unit
		Min	Typ	Max	Min	Typ	Max	
STATIC CHARACTERISTICS								
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	BV_{CBO}	20	60	–	20	60	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	BV_{CEO}	15	–	–	15	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	BV_{CIO}	20	60	–	20	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	BV_{EBO}	5.0	7.0	–	5.0	7.0	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	40	–	–	100	nAdc
DC Current Gain	h_{FE}							–
(I_C = 10 mAdc, V_{CE} = 3.0 Vdc)		–	140	–	–	–	–	
(I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc)		40	130	–	40	130	–	
(I_C = 10 μAdc, V_{CE} = 3.0 Vdc)		–	60	–	–	–	–	
Base-Emitter Voltage	V_{BE}							Vdc
(V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc)		–	0.72	–	–	0.72	–	
(V_{CE} = 3.0 Vdc, I_E = 10 mAdc)		–	0.80	–	–	0.80	–	
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\lvert I_{IO1} - I_{IO2} \rvert$	–	0.3	2.0	–	0.3	–	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	–	–	0.5	5.0	–	0.5	–	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	–	-1.9	–	–	-1.9	–	mV/°C
Temperature Coefficient	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	–	1.0	–	–	1.0	–	μV/°C
Collector-Emitter Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CEO}	–	–	0.5	–	–	5.0	μAdc
DYNAMIC CHARACTERISTICS								
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	–	3.25	–	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	–	110	–	–	110	–	–
Short-Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	–	3.5	–	–	3.5	–	kΩ
Open-Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	–	15.6	–	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	–	1.8	–	–	1.8	–	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	–	31-j1.5	–	–	31-j1.5	–	–
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	–	0.3+j0.04	–	–	0.3+j0.04	–	–
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	–	0.001+j0.03	–	–	0.001+j0.03	–	–
Current-Gain – Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	–	–	550	–	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	–	0.6	–	–	0.6	–	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	–	0.58	–	–	0.58	–	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	–	2.8	–	–	2.8	–	pF

TYPICAL CHARACTERISTICS

FIGURE 1 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

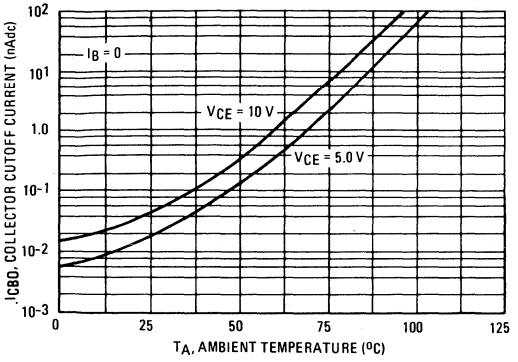


FIGURE 2 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

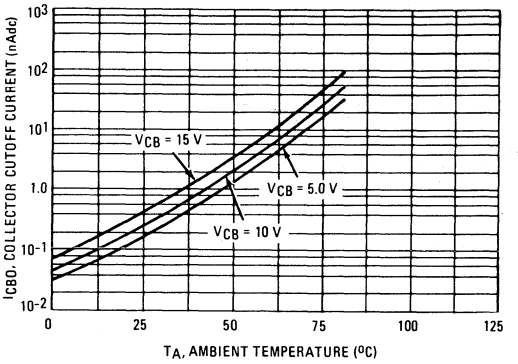


FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2

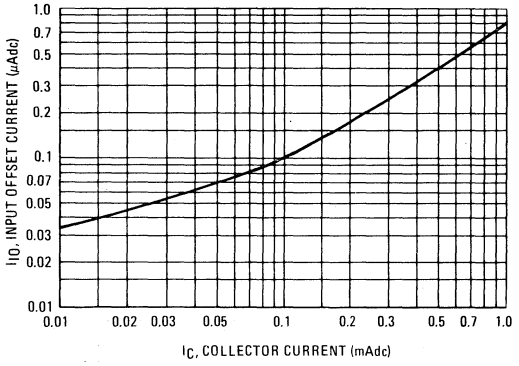


FIGURE 4 – BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS

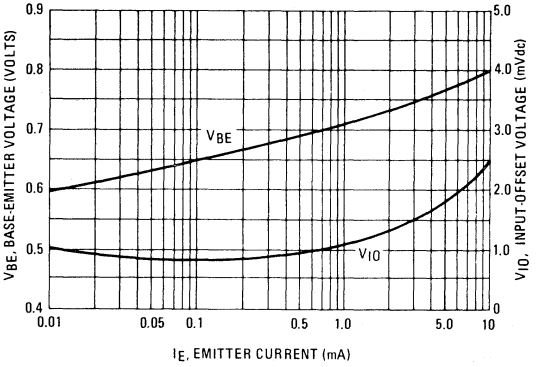
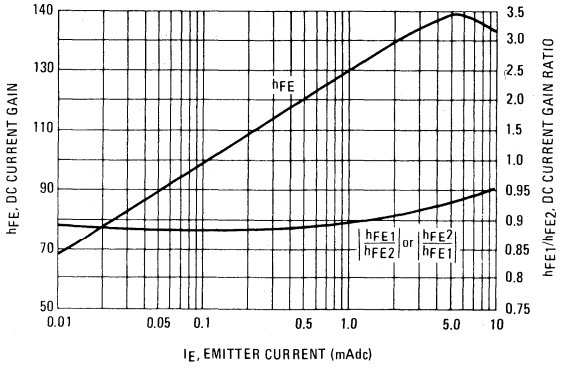


FIGURE 5 – DC CURRENT GAIN



Specifications and Applications Information

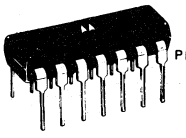
MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications such as are found in industrial control systems and automotive electronics. Each MC3401P device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages. Specifications are given for the MC3401P over the operating temperature range of 0 to +75°C.

- Single-Supply Operation — +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 5.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 1000 V/V minimum

MONOLITHIC QUAD OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 – EQUIVALENT CIRCUIT

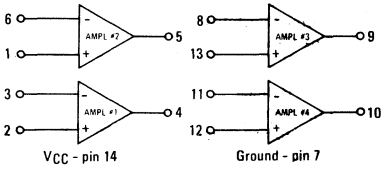
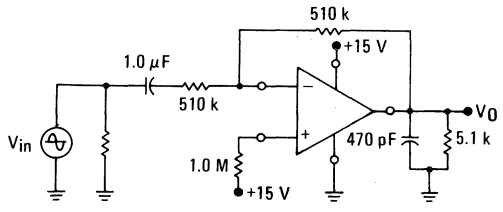


FIGURE 2 – SMALL-SIGNAL TRANSIENT RESPONSE



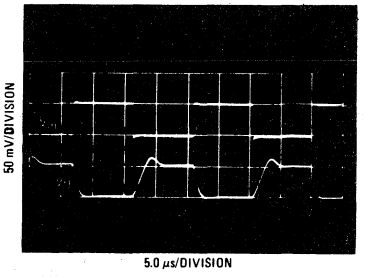


FIGURE 3 – INVERTING AMPLIFIER

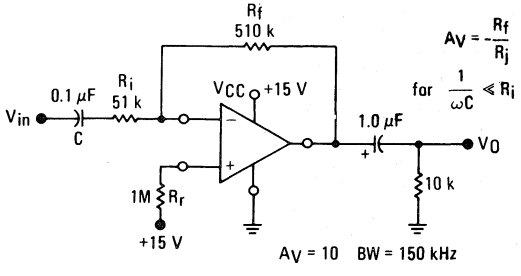
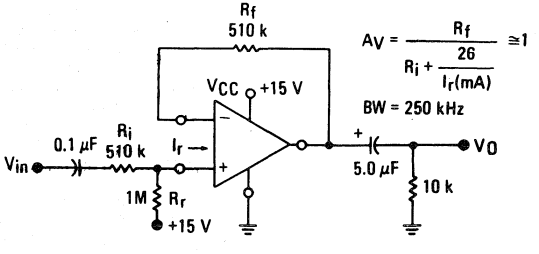


FIGURE 4 – NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Non-inverting Input Current	I_{in}	5.0	mA
Power Dissipation Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

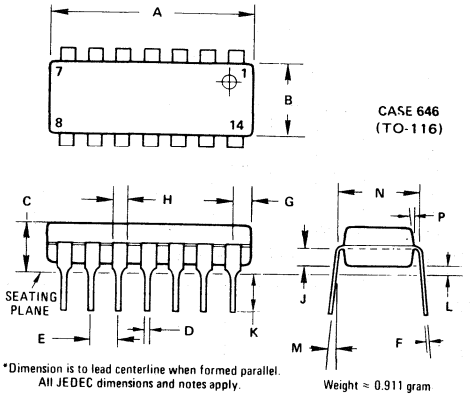
Characteristic	Fig. No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain	5,9,10	1	A_{vol}				V/V
T_A = +25°C				1000	2000	–	
0°C ≤ T_A ≤ +75°C				800	–	–	
Quiescent Power Supply Current (Total for four amplifiers)	6,12	2					mAdc
Noninverting inputs open			I_{DO}	–	6.9	10	
Noninverting inputs grounded			I_{DG}	–	7.8	14	
Input Bias Current, R_L = ∞	5	3	I_{IB}				nAdc
T_A = +25°C				–	50	300	
0°C ≤ T_A ≤ +75°C				–	–	500	
Output Current	5	4					mAdc
Source Capability	13		I_{source}	5.0	10	–	
Sink Capability	14		I_{sink}	0.5	1.0	–	
Output Voltage							Vdc
High Voltage	7	5	V_{OH}	13.5	14.2	–	
Low Voltage	7	5	V_{OL}	–	0.03	0.1	
Undistorted Output Swing (0°C < T_A < +75°C)	8	6	$V_{O(p-p)}$	10	13.5	–	$V_{(p-p)}$
Input Resistance	5		R_{in}	0.1	1.0	–	MEG Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth			BW	–	5.0	–	MHz
Phase Margin			ϕ_m	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)		7	PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

NOTES

1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
5. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
6. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
7. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

OUTLINE DIMENSIONS



*Dimension is to lead centerline when formed parallel.
All JEDEC dimensions and notes apply.

Weight ≈ 0.911 gram

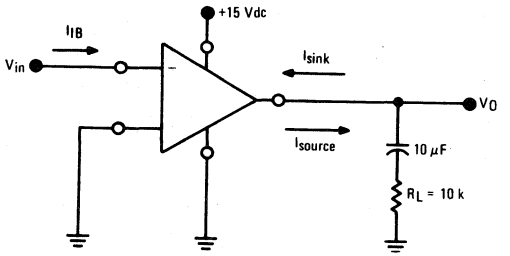
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.710	0.740	18.030	18.790
B	0.240	0.260	6.090	6.600
C	0.160	0.180	4.060	4.570
D	0.015	0.020	0.381	0.508
E	0.100 T.P.		2.54 T.P.	
F	0.009	0.014	0.228	0.355
G	0.060	0.080	1.520	2.030
H	0.040	0.065	1.020	1.650
J	0.062	0.072	1.570	1.830
K	0.115	0.135	2.920	3.430
L	0.025	0.035	0.635	0.889
M	0°	10°	0°	10°
N	0.290	0.310	7.360	7.870
P	7° TYP		7° TYP	

1. DIM "N" TO LEAD CENTERLINE WHEN FORMED PARALLEL.

SIMPLIFIED TEST CIRCUITS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

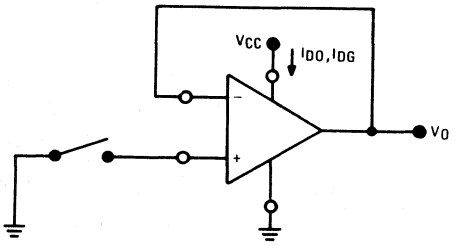
FIGURE 5 – OPEN LOOP GAIN AND INPUT RESISTANCE
(INPUT BIAS CURRENT, OUTPUT CURRENT)



$$R_{in} = \frac{\Delta V_{in}}{\Delta I_{IB}} \quad A_{vol} = -\frac{\Delta V_O}{\Delta V_{in}}$$

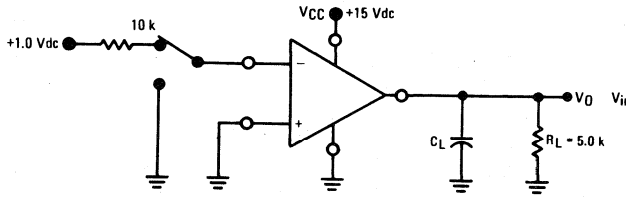
Amplifier must be biased (by V_{in}) in the linear operating region.

FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



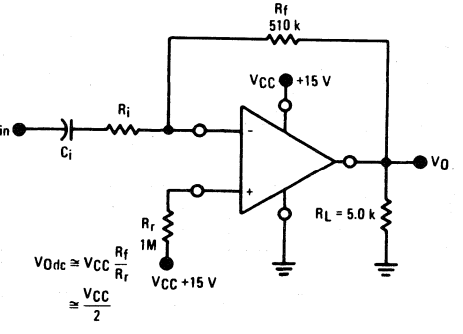
I_{DO} is total supply current with "+" input open.
I_{DG} is total supply current with "+" input grounded.

FIGURE 7 – OUTPUT VOLTAGE SWING



V_{OL} measured with "–" input biased up as shown.
V_{OH} measured with "–" input grounded.

FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{Odc} \cong V_{CC}\frac{R_f}{R_r} \cong \frac{V_{CC}}{2}$$

for $R_r \cong 2R_f$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

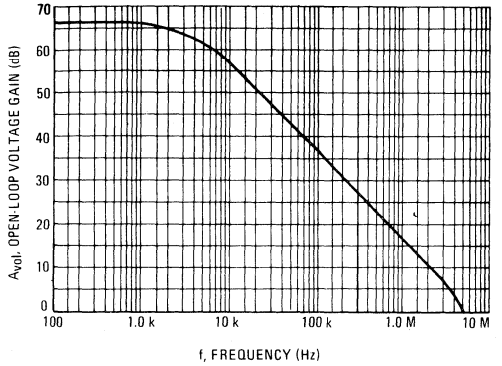


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

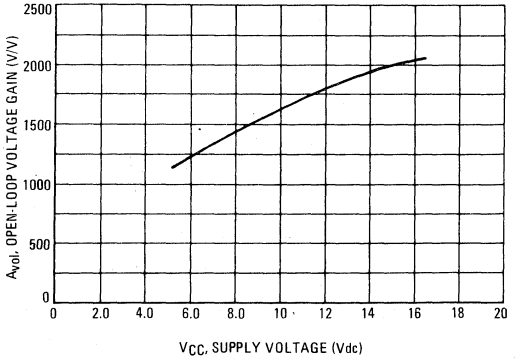


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

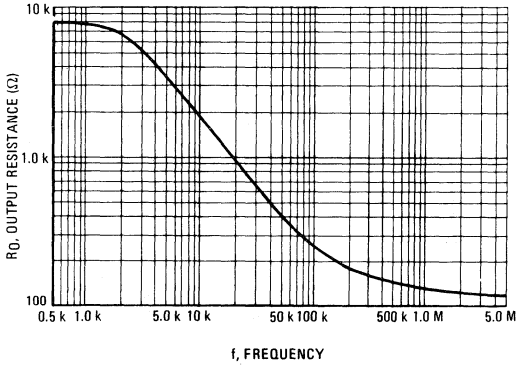


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

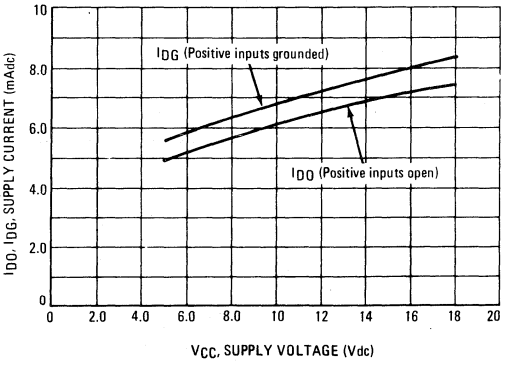


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

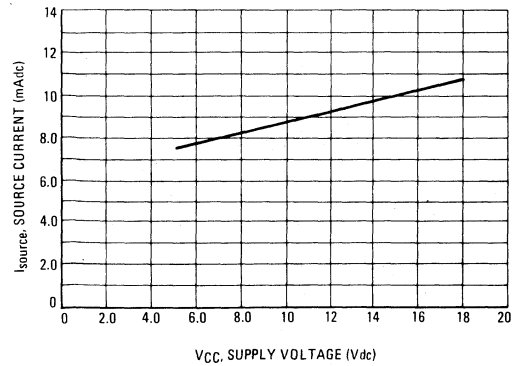
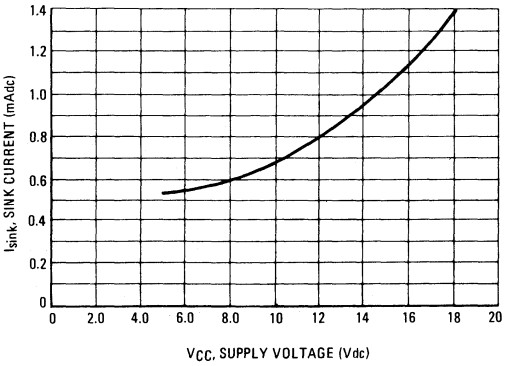


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE

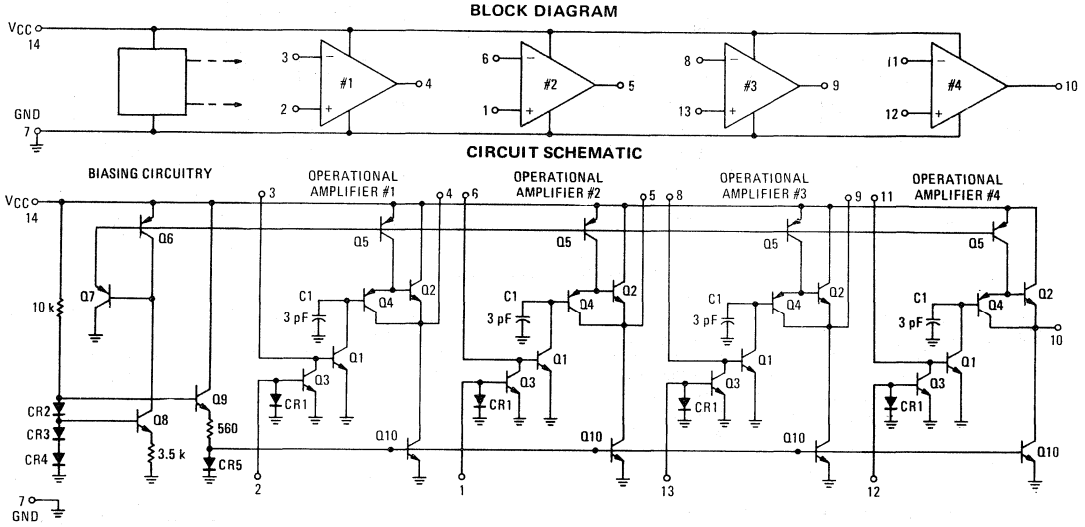


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_{in2}, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2}. Since the alpha current gain of Q3 $\approx$ 1, its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

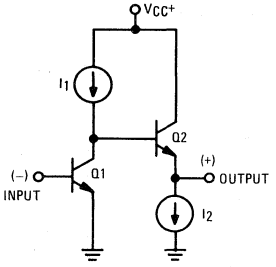
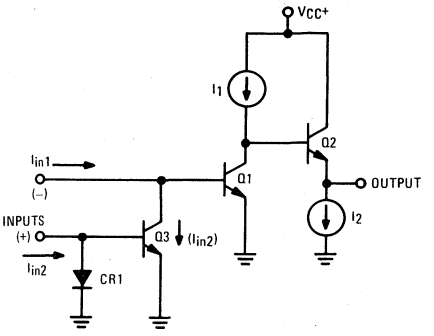


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR2 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

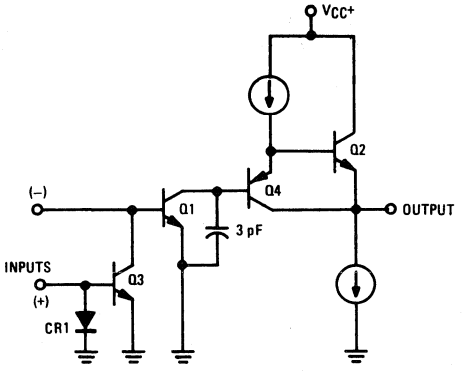
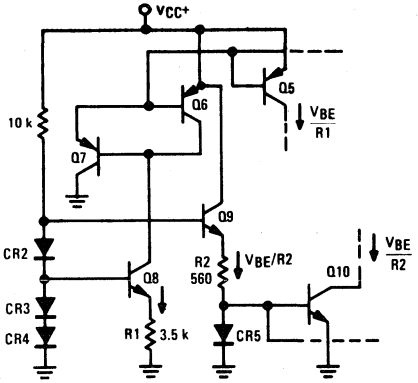


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 5 μA to 100 μA range.
   B. V_{CC} Reference Voltage (see Figures 3 and 4)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.
   C. Reference Voltage other than V_{CC} (See Figure 20).
   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 5 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

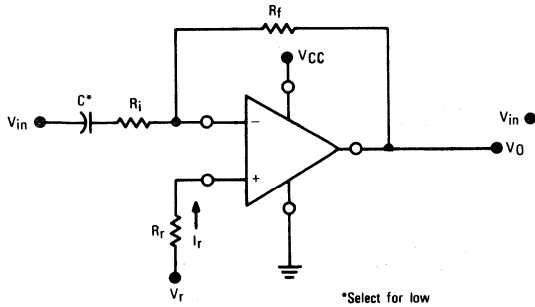
$$V_{Odc} = \frac{(V_r)\ (R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 Vdc @ +25°C).

   The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μA to 100 μA.

2. Gain Determination
   A. Inverting Amplifier
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

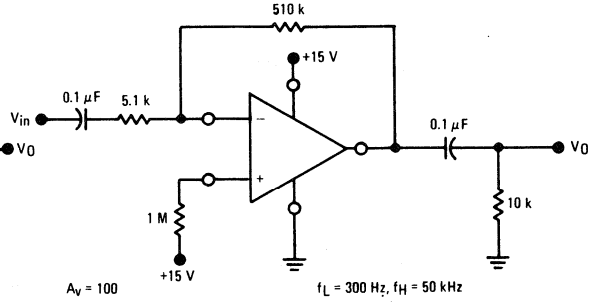
FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



$$V_O = \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

*Select for low frequency response.

FIGURE 21 – INVERTING AMPLIFIER WITH A_v = 100 AND $V_r = V_{CC}$



A_v = 100

f_L = 300 Hz, f_H = 50 kHz

NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

Although recommended as an inverting amplifier, the MC 3401P may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as ±20% from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting gain expression is given by:

$$A_v = \frac{R_f}{R_i + \frac{26}{I_r\ (mA)}} \quad \pm 20\%.$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE

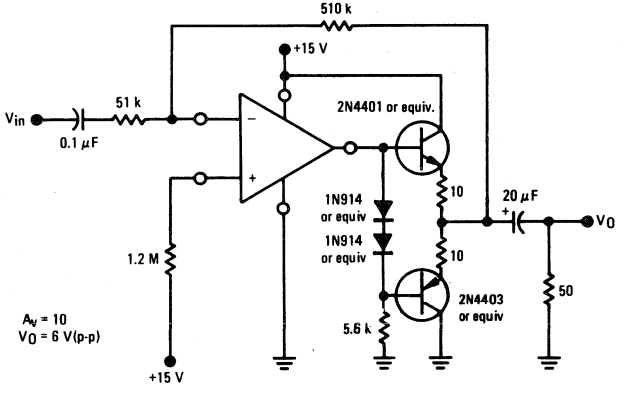
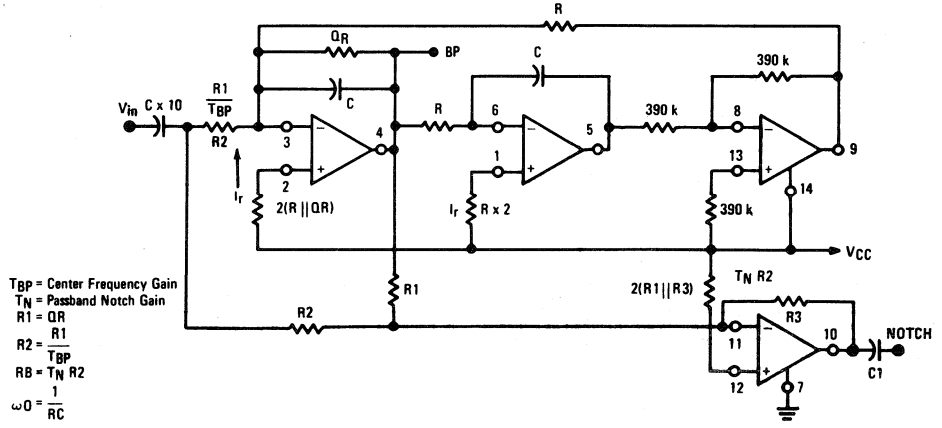


FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



TYPICAL APPLICATIONS (continued)

FIGURE 24 – BANDPASS AND NOTCH FILTER

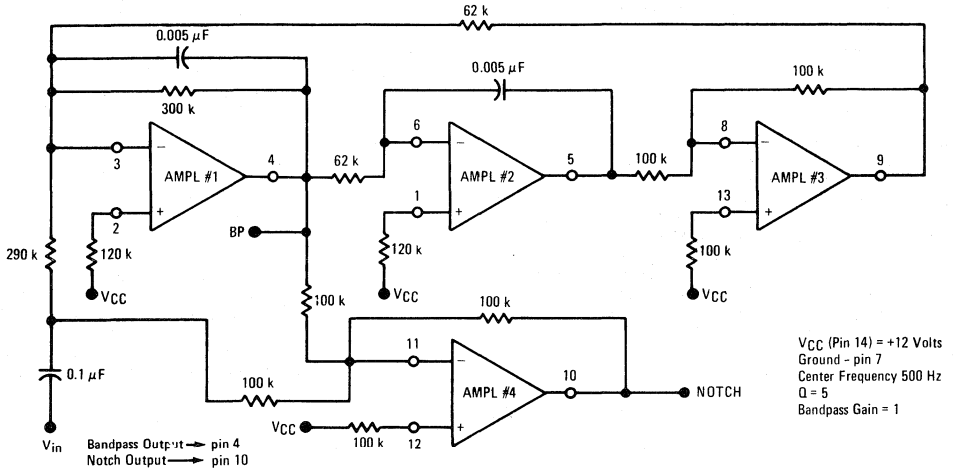
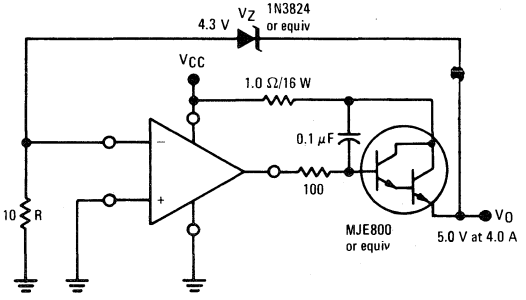


FIGURE 25 – VOLTAGE REGULATOR

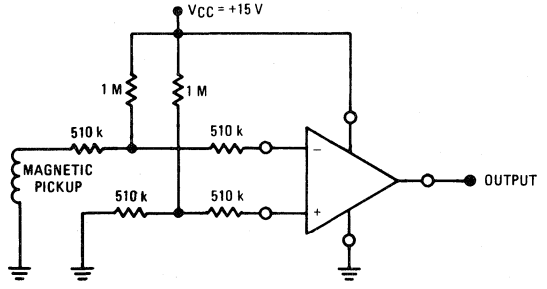


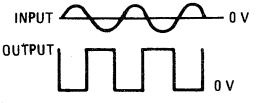
$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈ 2.0 mV/°C), the output is zero-TC. A 7.0-Volt Zener will give approximately zero-TC.

FIGURE 26 – ZERO CROSSING DETECTOR





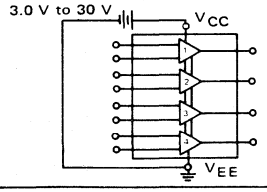
Specifications and Applications Information

QUAD LOW POWER OPERATIONAL AMPLIFIERS

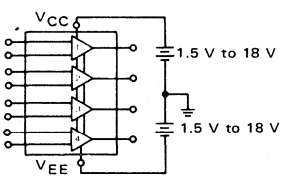
The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741

SINGLE SUPPLY



SPLIT SUPPLIES



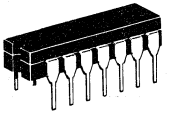
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC} V_{EE}	 36 +18 -18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±15	Vdc
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Operating Ambient Temperature Range MC3503 MC3403 MC3303	T_A	 -55 to +125 0 to +70 -40 to +85	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

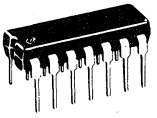
(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

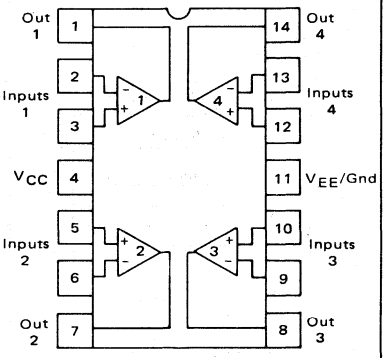


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 only)

PIN CONNECTIONS



ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	PACKAGE
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	-55°C to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V for MC3503, MC3403, V_{CC} = +14 V, V_{EE} = Gnd for MCC3303. T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	8.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	6.0	–	–	12	–	–	10	
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	30	75	nA
$T_A = T_{high}$ to T_{low}		–	–	200	–	–	200	–	–	250	
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
V_O = ±10 V, R_L = 2.0 kΩ,		50	200	–	20	200	–	20	200	–	
$T_A = T_{high}$ to T_{low}		25	300	–	15	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	-200	-500	nA
$T_A = T_{high}$ to T_{low}		–	-300	-1500	–	–	-800	–	–	-1000	
Output Impedance	z_o	–	75	–	–	75	–	–	75	–	Ω
f = 20 Hz											
Input Impedance	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
f = 20 Hz											
Output Voltage Range	V_{OR}										V
R_L = 10 kΩ		±12	±13.5	–	±12	±13.5	–	+12	+12.5	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	+10	+12	–	
R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}		±10	–	–	±10	–	–	+10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13V -V_{EE}	+13.5V -V_{EE}	–	V
Common-Mode Rejection Ratio	CMRR	70	90	–	70	90	–	70	90	–	dB
$R_S \leq$ 10 kΩ											
Power Supply Current (V_O = 0)	I_{CC},I_{EE}	–	2.8	4.0	–	2.8	7.0	–	2.8	7.0	mA
$R_L = \infty$											
Individual Output Short-Circuit Current (2)	$I_{OS\pm}$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
$T_A = T_{high}$ to T_{low}											
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
$T_A = T_{high}$ to T_{low}											
Power Bandwidth	BWp	–	9.0	–	–	9.0	–	–	9.0	–	kHz
A_V = 1, R_L = 2.0 kΩ, V_O = 20 V(p-p), THD = 5%											
Small-Signal Bandwidth	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
A_V = 1, R_L = 10 kΩ, V_O = 50 mV											
Slew Rate	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
A_V = 1, V_i = -10 V to +10 V											
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
A_V = 1, R_L = 10 kΩ, V_O = 50 mV											
Fall Time	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
A_V = 1, R_L = 10 kΩ, V_O = 50 mV											
Overshoot	OS	–	20	–	–	20	–	–	20	–	%
A_V = 1, R_L = 10 kΩ, V_O = 50 mV											
Phase Margin	φm	–	60	–	–	60	–	–	60	–	Degrees
A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF											
Crossover Distortion	–	–	1.0	–	–	1.0	–	–	1.0	–	%
(V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)											

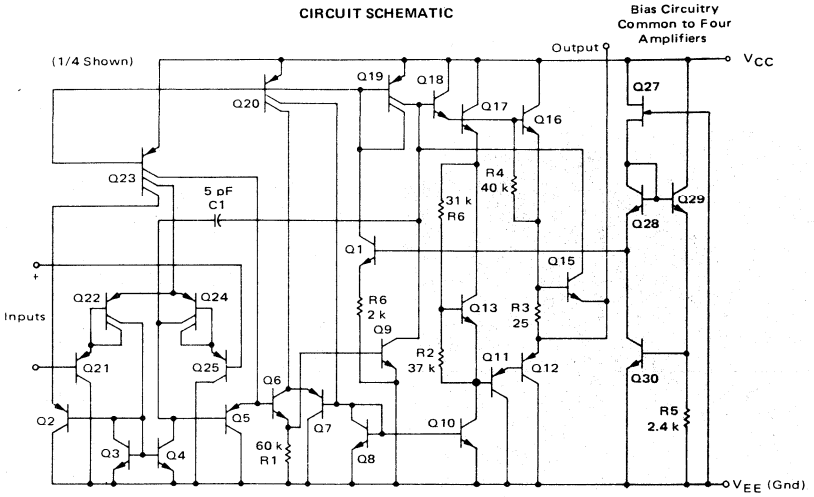
(1) T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = -55°C for MC3503, 0°C for MC3403, -40°C for MC3303

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

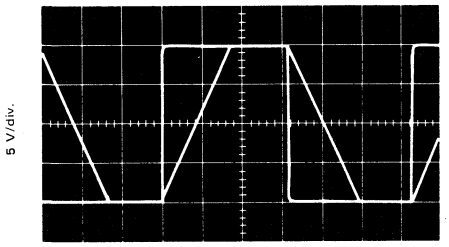
Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
R_L = 2.0 kΩ											
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3)	V_{OR}										Vp-p
R_L = 10 kΩ, V_{CC} = 5.0 V		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V		V_{CC}-1.7	V_{CC}-1.5	–	V_{CC}-1.7	V_{CC}-1.5	–	V_{CC}-1.7	V_{CC}-1.5	–	
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation	–	–	-120	–	–	-120	–	–	-120	–	dB
f = 1.0 kHz to 20 kHz (Input Referenced)											

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

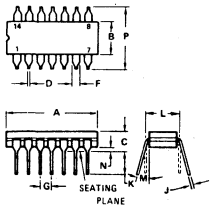
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116
$R_{\theta JA}$ = 100°C/W Typical



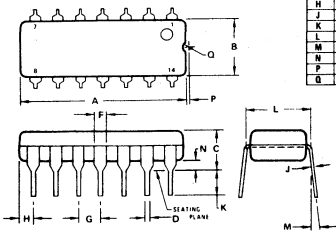
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

NOTE:
DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

weight = 1.954 grams

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 only)
$R_{\theta JA}$ = 100°C/W Typical



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

weight = 0.911 gram

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

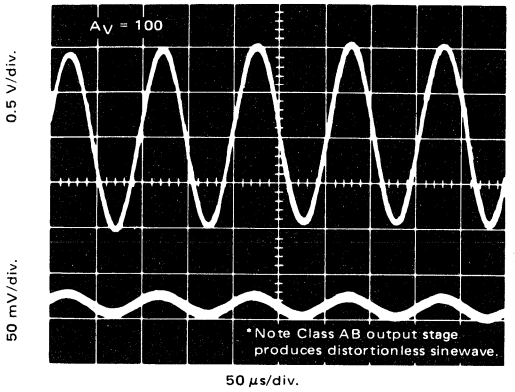


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

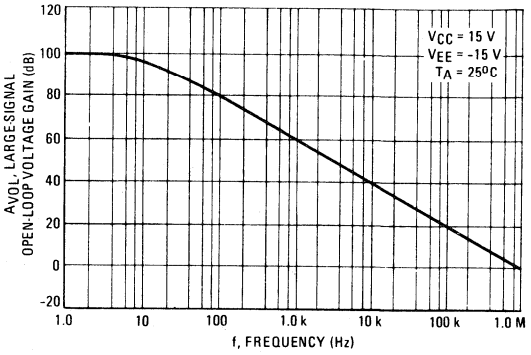


FIGURE 3 – POWER BANDWIDTH

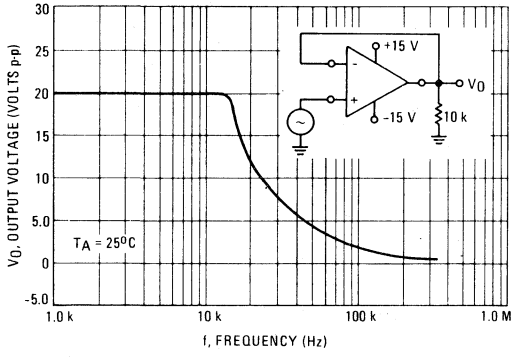


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

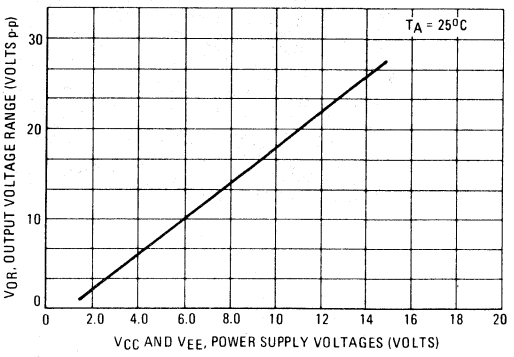


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

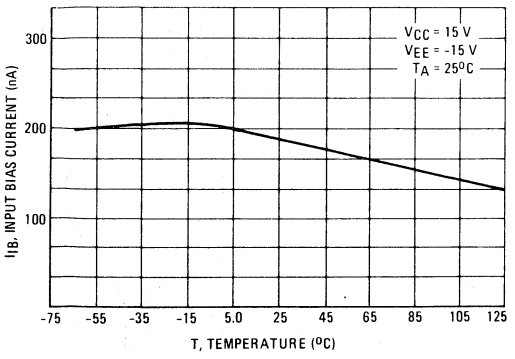
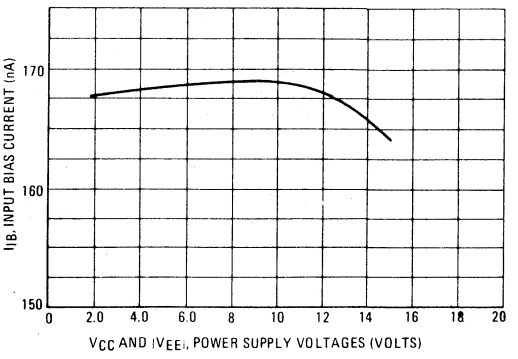
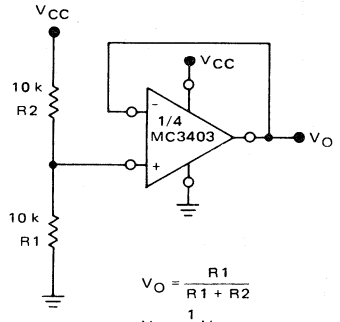


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

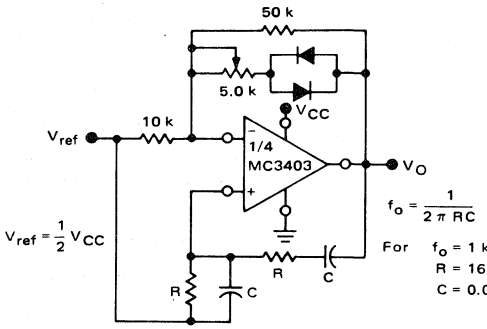
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

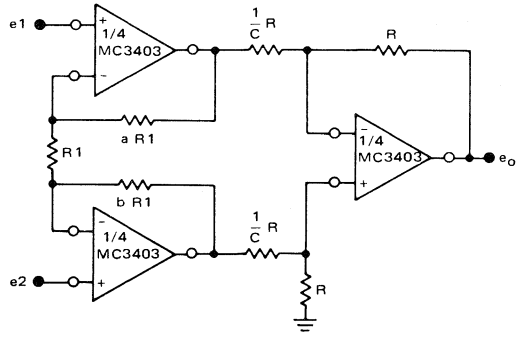


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

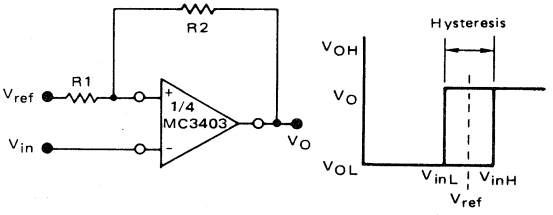
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\ (1 + a + b)\ (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

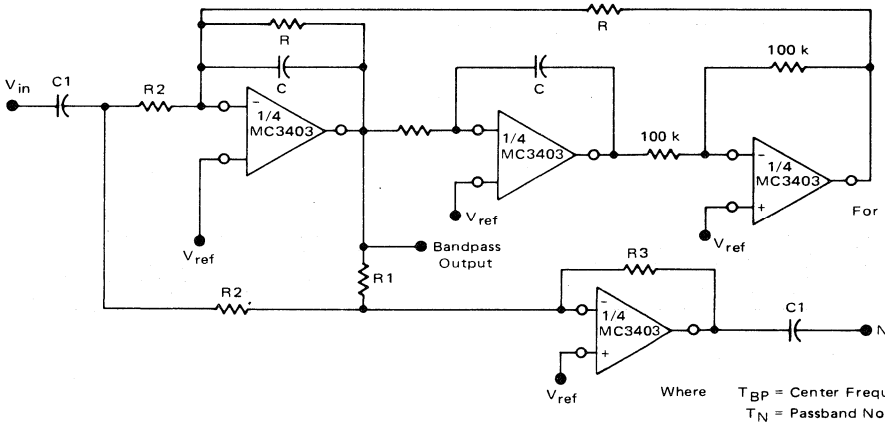


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

C1 = 10 C

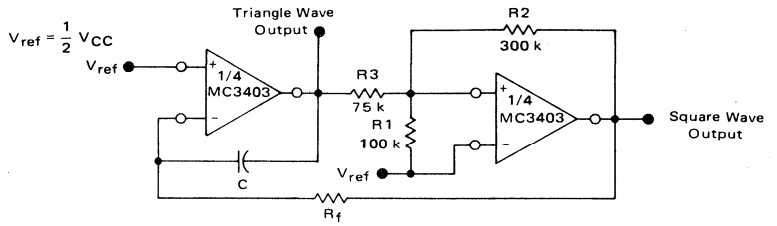
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

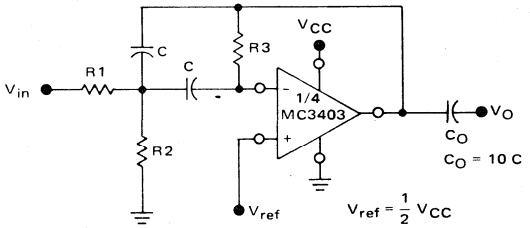
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R5}{4Q^2 R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

SWITCHMODE REGULATOR CONTROL CIRCUIT

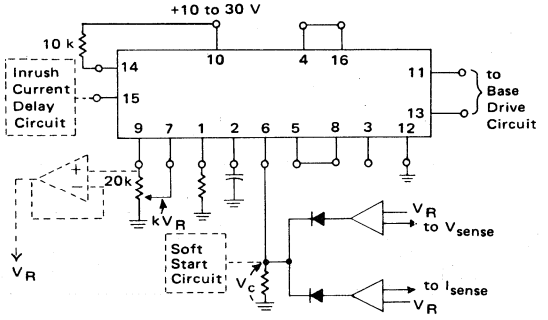
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

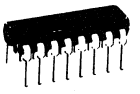
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1–TYPICAL APPLICATION

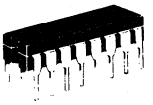


SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS

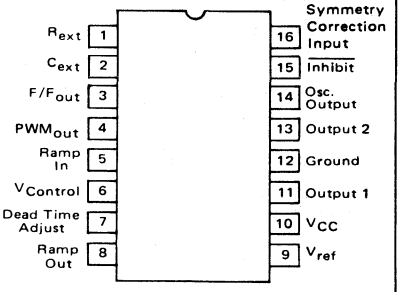


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature	T_J			°C
Plastic Package		–	125	
Ceramic Package		150	150	
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 to 30 V, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
REFERENCE SECTION									
Reference Voltage (I_{ref} = 400 μA)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage (V_{CC} = 15 V, I_{ref} = 400 μA)	5	TCV_{ref}	–	0.008	0.03	–	0.008	0.03	%/°C
Input Regulation of Reference Voltage	5	$Reg_{(in)}$							mV/V
(I_{ref} = 400 μA)			–	3.0	7.5	–	4.0	7.5	
(I_{ref} = 1.0 mA)			–	5.0	–	–	5.0	–	
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	–	30	10	–	30	V
Supply Current (R_{ext} = 10 kΩ, excluding load and current and reference current)	5	I_D	–	–	16	–	–	22	mA
OSCILLATOR SECTION									
Line Frequency Stability	5								
(f = 20 kHz)		Δf	–	–	3.0	–	–	5.0	%
(f = 20 kHz, V_{CC} = 15 V, T_{low} to T_{high})		Δf	–	0.03	–	–	0.04	–	%/°C
Maximum Output Frequency (V_{CC} = 15 V)	6	f_{max}	100	200	–	100	200	–	kHz
Minimum Output Frequency (V_{CC} = 15 V)	6	f_{min}	–	2.0	5.0	–	2.0	5.0	kHz
Oscillator Output Saturation Voltage ($I_{14\ sink}$ = 5.0 mA)	11	$V_{osc(sat)}$	–	0.2	0.5	–	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage	7	$V_{CE(sat)}$							V
(I_L = 40 mA, T_{high} to T_{low})			–	0.33	0.5	–	0.33	0.5	
(I_L = 25 mA, T_{high} to T_{low})			–	0.22	–	–	0.22	–	
Output Leakage Current (V_{CE} = 40 V, pins 11 and 13)	8	I_{CE}	–	–	50	–	–	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	–	100	0	–	100	%
Dead Time Adjustment Range	9	ΔDT	0	–	100	0	–	100	%
Temperature Coefficient of Dead Time	–	TCDT	–	0.1	–	–	0.1	–	%/°C
Comparator Bias Currents	12, 13, 14	I_{IB}	–	5.0	15	–	5.0	15	μA

ELECTRICAL CHARACTERISTICS (continued)

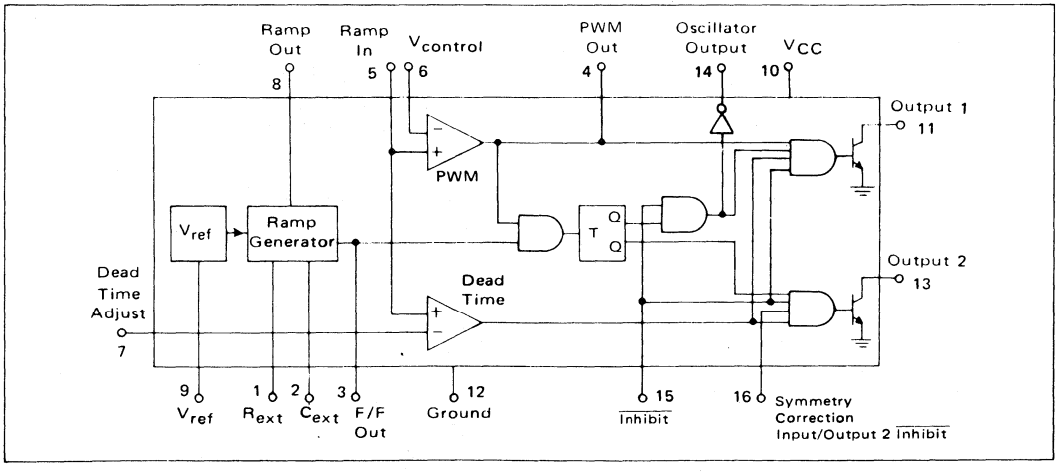
Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
AUXILIARY INPUTS/OUTPUTS									
Ramp Voltage Peak High Peak Low	5	 $V_{ramp(Hi)}$ $V_{ramp(Low)}$	 5.5 2.0	 6.0 2.4	 6.5 2.8	 5.5 2.0	 6.0 2.4	 6.5 2.8	V
Ramp Voltage Change ($V_{ramp\ Hi} - V_{ramp\ Low}$)	5	ΔV_{ramp}	3.0	3.5	4.0	3.0	3.5	4.0	V
Ramp Out Sink Current	5	I_{sink}	–	400	–	–	400	–	μA
Ramp Out Source Current	5	I_{source}	–	3.0	–	–	3.0	–	mA
$\overline{\text{Inhibit}}$ Input Current – High (V_{IH} = 2.0 V)	10	I_{IH}	–	–	40	–	–	40	μA
$\overline{\text{Inhibit}}$ Input Current – Low (V_{IL} = 0.8 V)	10	I_{IL}	–	–25	–180	–	–25	–180	μA
Symmetry Correction Input/Output 2 Inhibit Current – High (V_{SY} = 2.0 V, pin 16)	10	$I_{SY/H}$	–	–	40	–	–	40	μA
Symmetry Correction Input/Output 2 Inhibit Current – Low (V_{SY} = 0.8 V, pin 16)	10	$I_{SY/L}$	–	–10	–180	–	–10	–180	μA
F/F_{out} Source Current	–	I_{source}	–	2.0	–	–	2.0	–	mA
OUTPUT AC CHARACTERISTICS ($T_A = T_{high}$, V_{CC} = +15 V, f = 20 kHz)									
Rise Time	15	t_r	–	40	–	–	40	–	ns
Fall Time	15	t_f	–	150	–	–	150	–	ns
Overlap Time	15	t_{ov}	–	275	–	–	275	–	ns
Assymmetry (Duty Cycle = 50%)	15	$\frac{t_{on1} - t_{on2}}{t_{on1}}$	–	±1.0	–	–	±1.0	–	%

NOTE:

T_{high} = +125°C for MC3520
+70°C for MC3420

T_{low} = -55°C for MC3520
0°C for MC3420

FIGURE 2–EQUIVALENT CIRCUIT



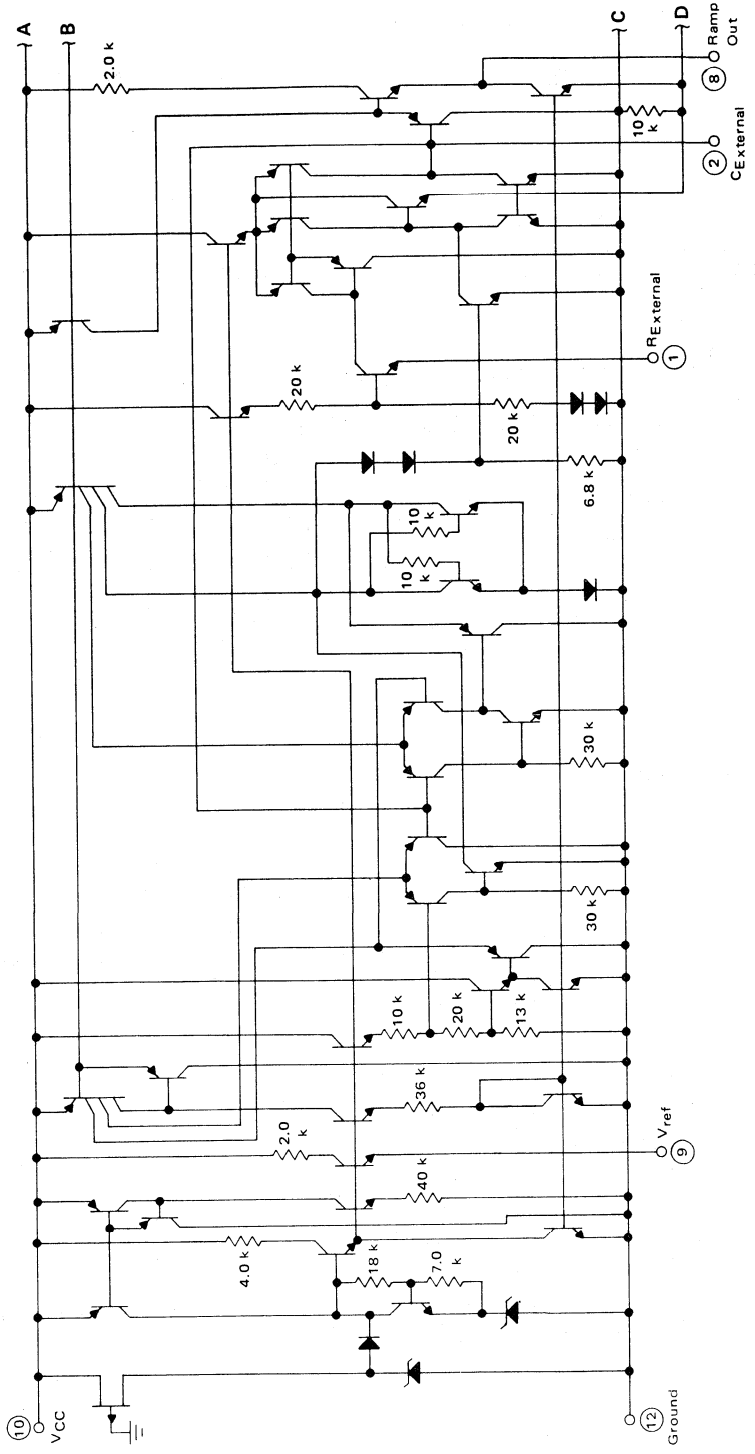
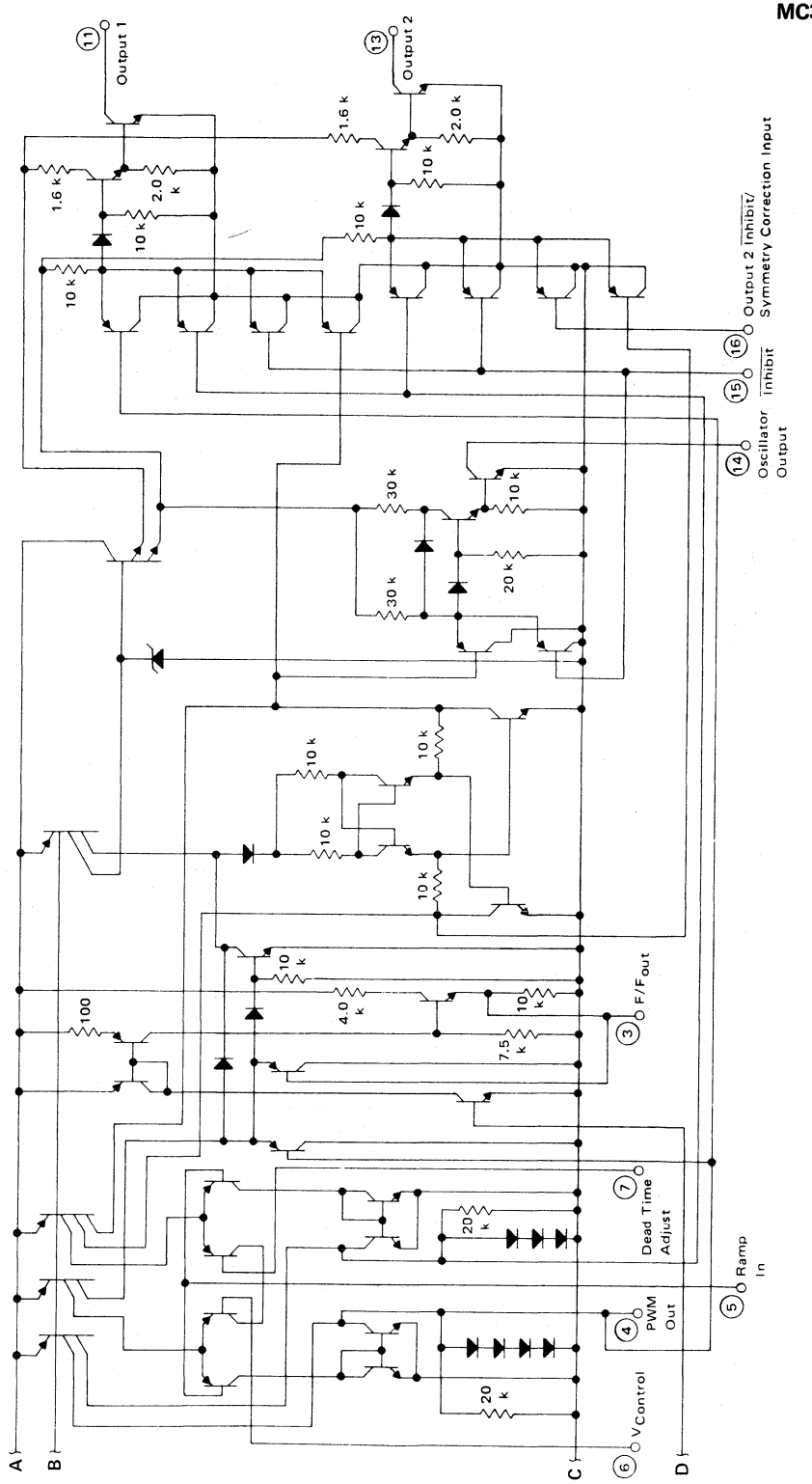


FIGURE 3 – CIRCUIT SCHEMATIC
(continued next page)



(continued) FIGURE 3 – CIRCUIT SCHEMATIC

GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS

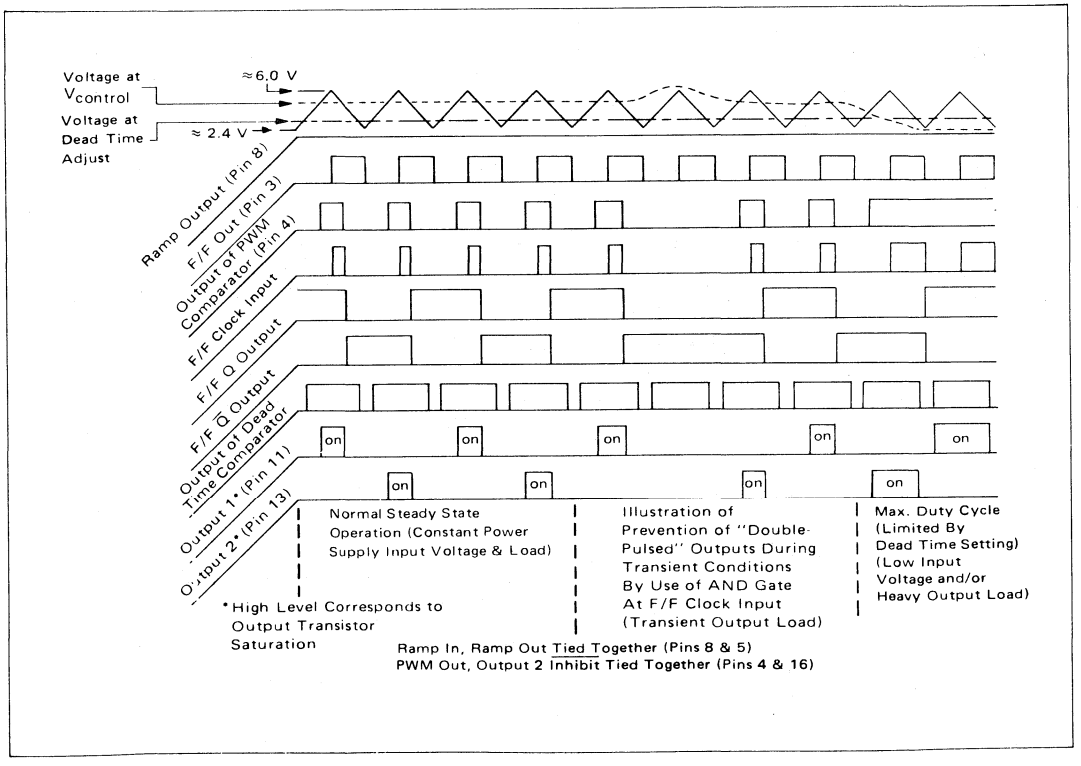


FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

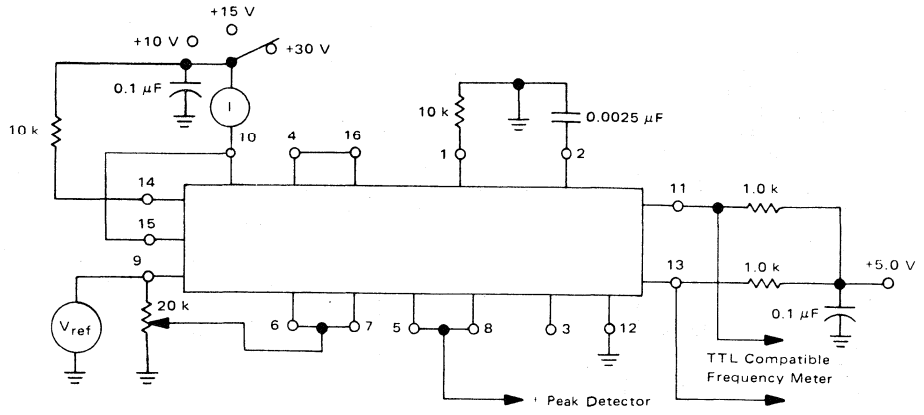


FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

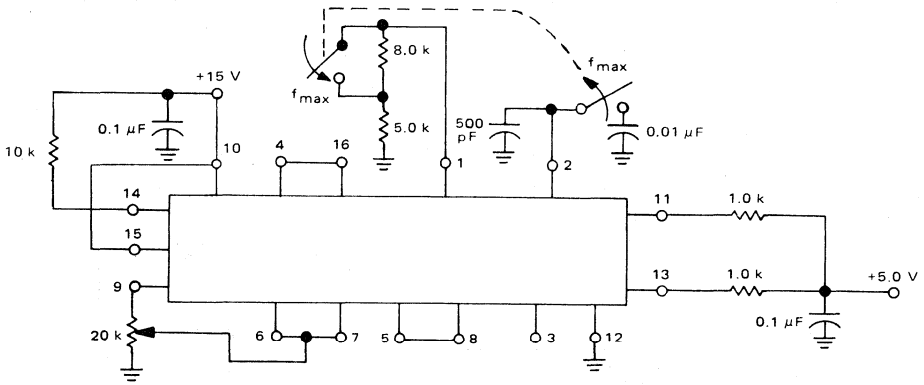
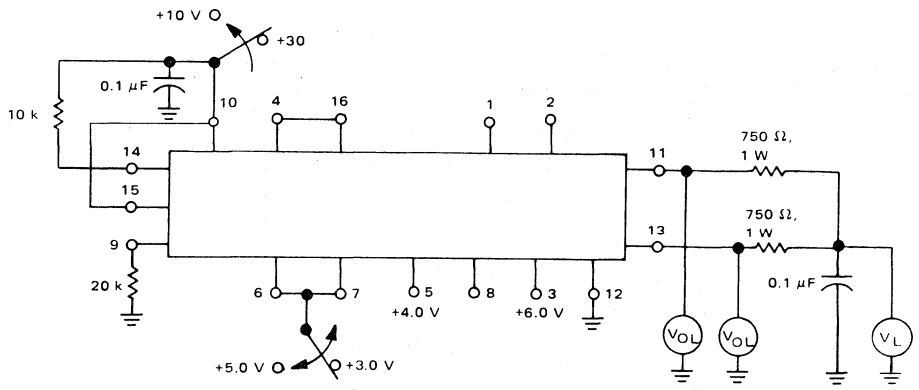
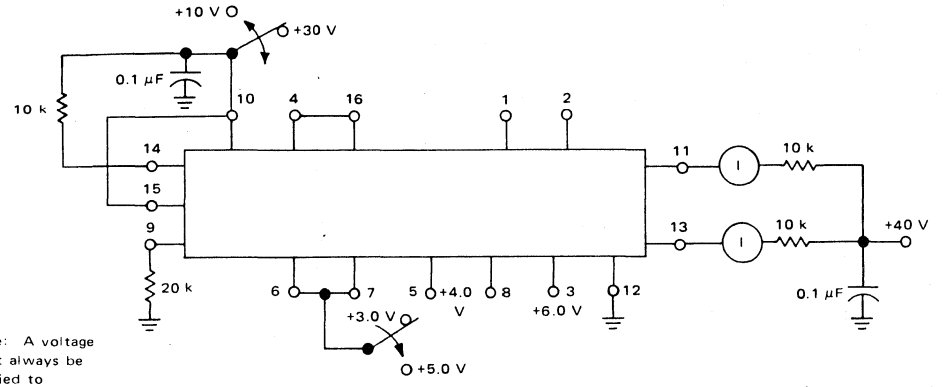


FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT



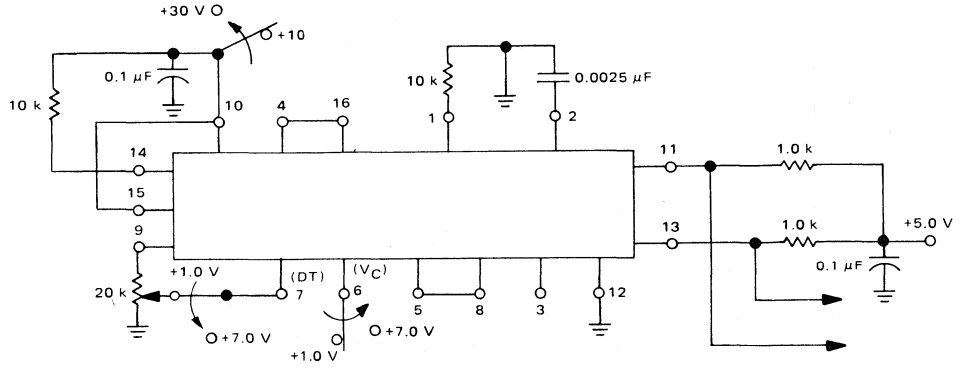
Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT



Note: A voltage must always be applied to pins 6 and 7.

FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT



TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE		TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$)	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{control}$ = 2.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)	PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50	2.0	50
2.5	46	2.5	46
3.0	40	3.0	40
3.5	33	3.5	33
4.0	26	4.0	26
4.5	18	4.5	18
5.0	11	5.0	11
5.5	4.0	5.5	4.0
6.0	0	6.0	0

	V_6	V_7	
	Volts		
100% Adjust			
Dead Time	1.0	1.0	(Pin 11 + Pin 13 = Logic "1")
Pulse Width	1.0	1.0	
0% Adjust			
Dead Time	7.0	1.0	(Pin 11)(Pin 13) = Logic "1"
Pulse Width	1.0	7.0	

NOTE: Logic "1" is TTL-Compatible V_{OH}.

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT

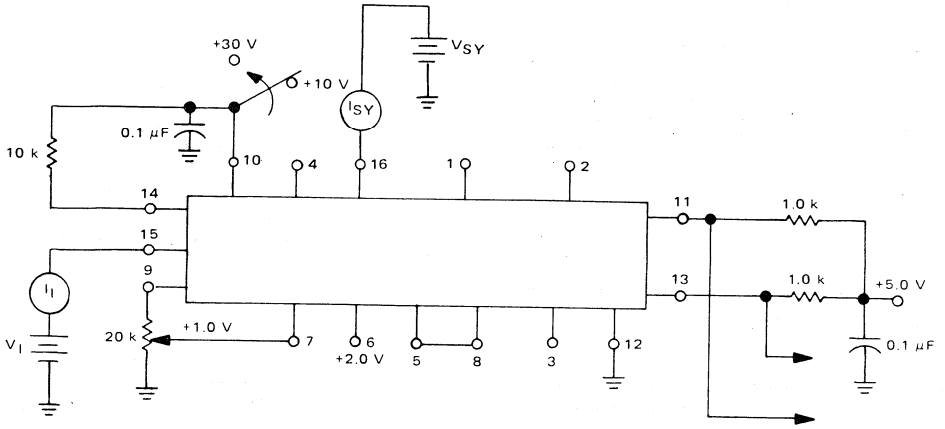


FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT

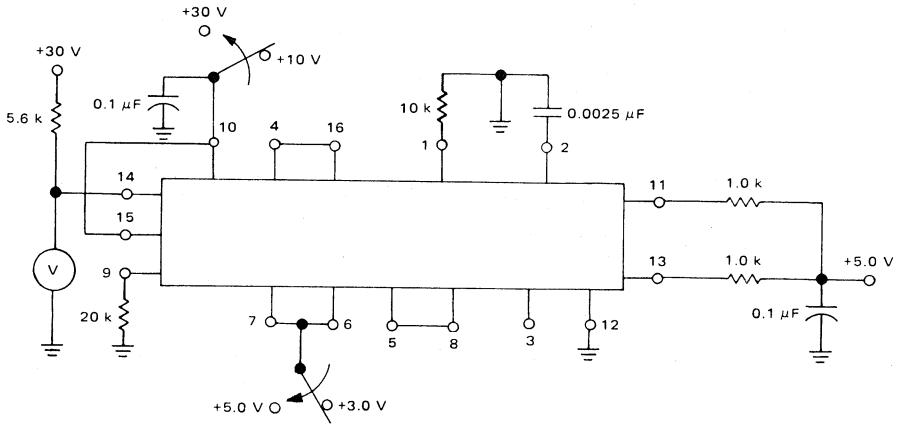


FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT

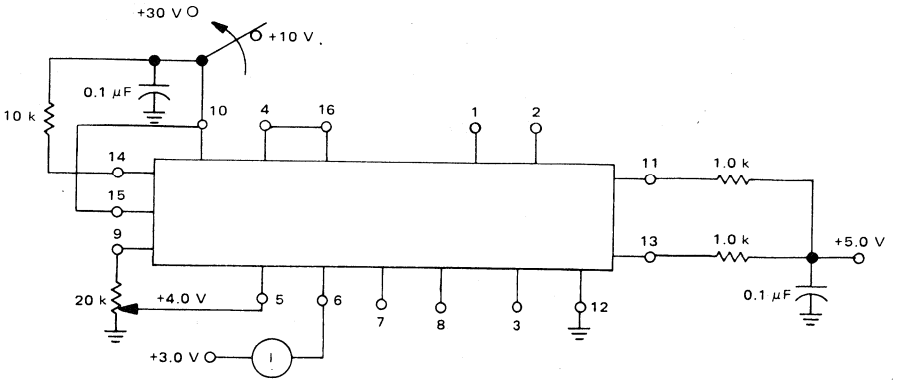


FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

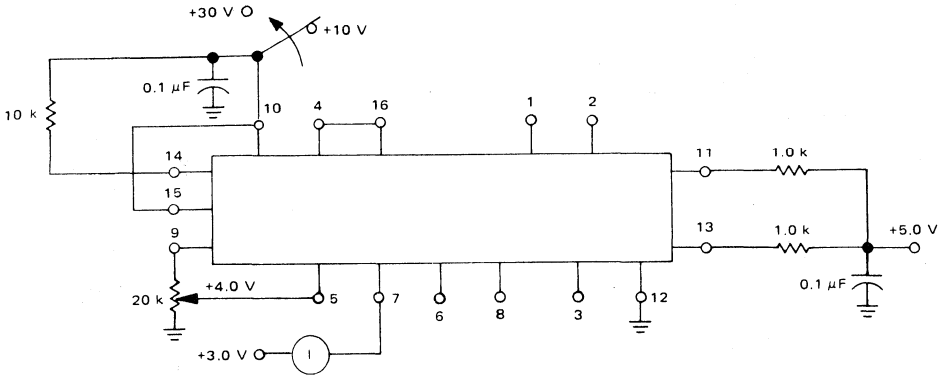


FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

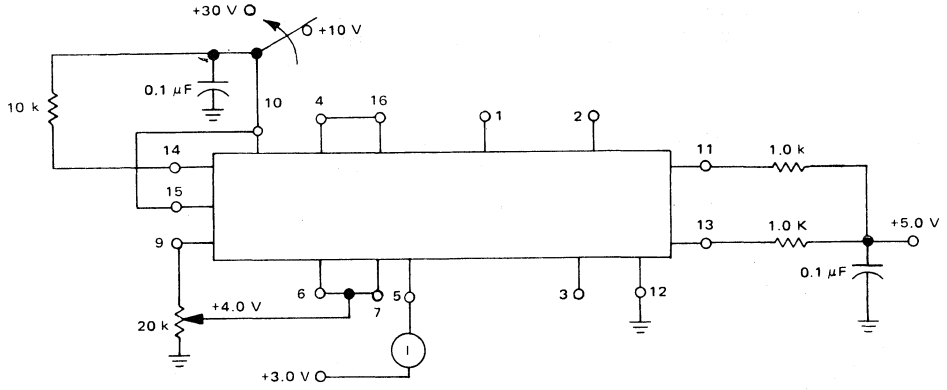
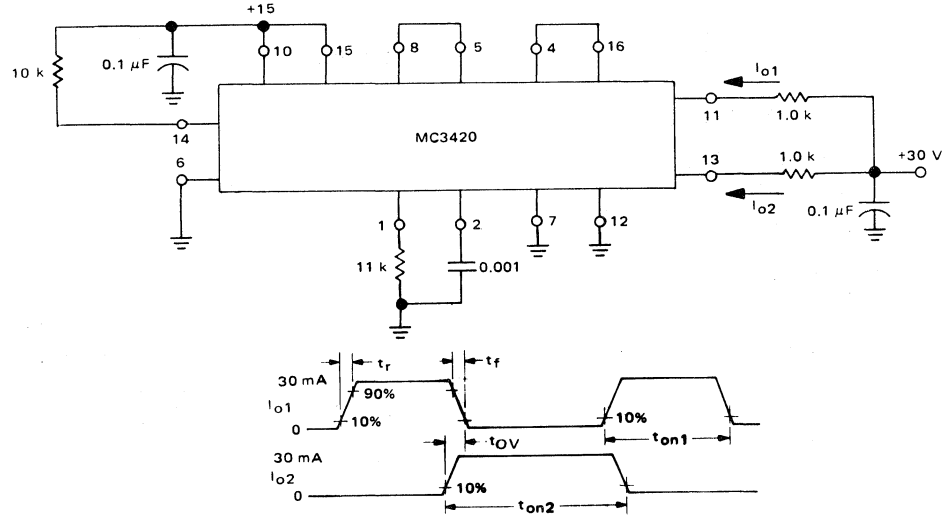


FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 16 – OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

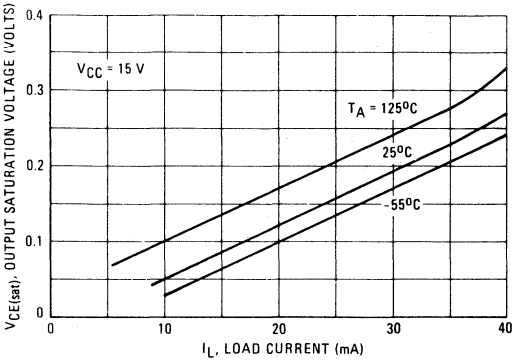


FIGURE 17 – REFERENCE VOLTAGE versus REFERENCE CURRENT

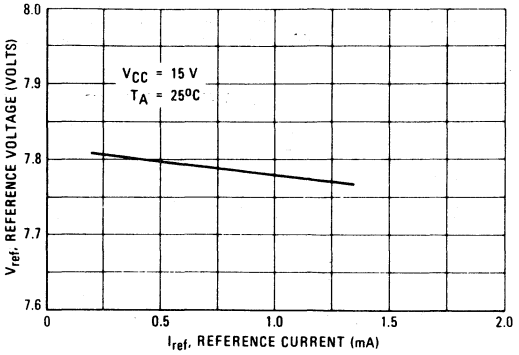


FIGURE 18 – DRAIN CURRENT versus EXTERNAL RESISTANCE

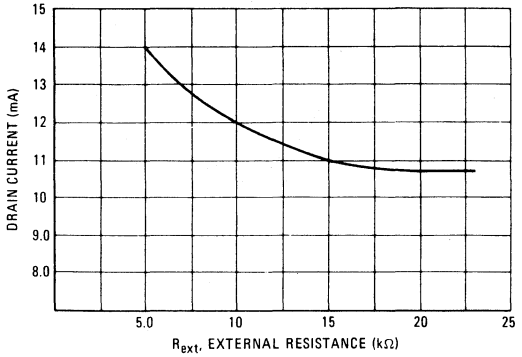


FIGURE 19 – PEAK FLIP-FLOP$_{out}$ VOLTAGE versus EXTERNAL RESISTANCE

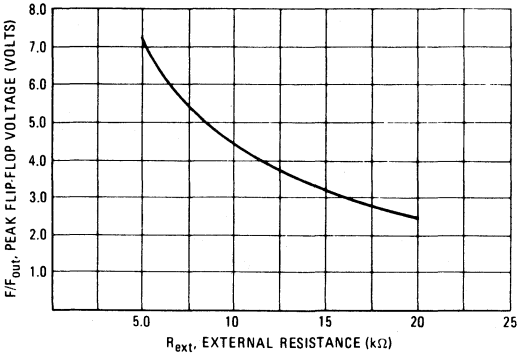


FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

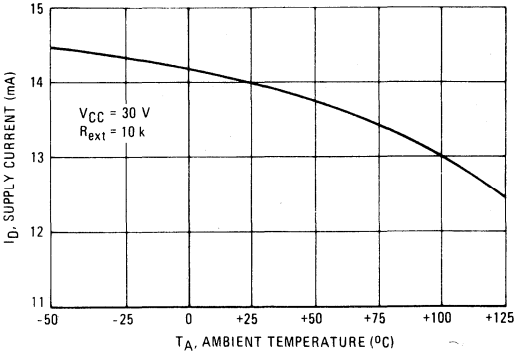
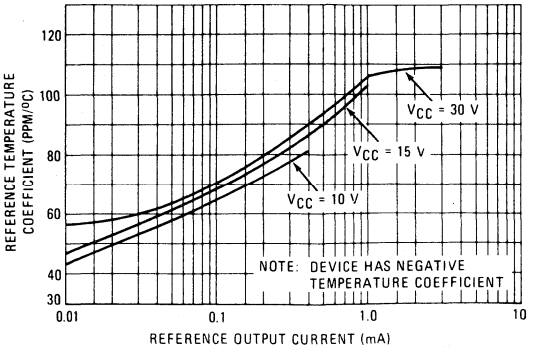


FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE COEFFICIENT versus OUTPUT CURRENT

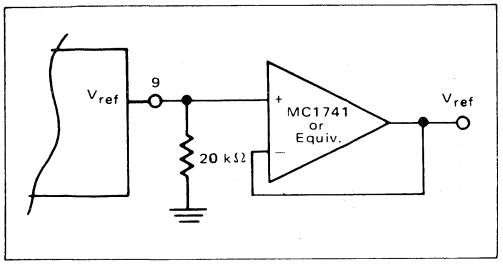


OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a 400 μA (≅20 kΩ) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22



Output Frequency

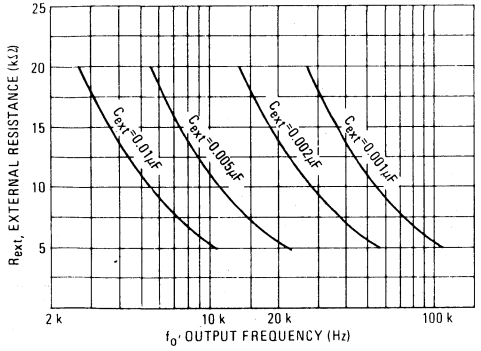
The values of R_{ext} and C_{ext} for a given output frequency, f_o, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}} \; ; \; 5.0\ k\Omega \leq R_{ext} \leq 20\ k\Omega \quad \text{(Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o.

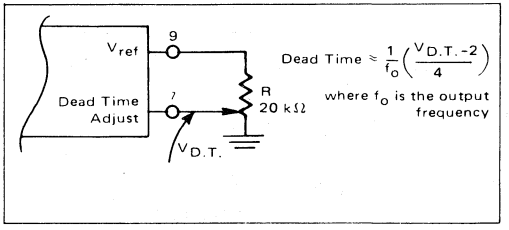
FIGURE 23



Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

FIGURE 24



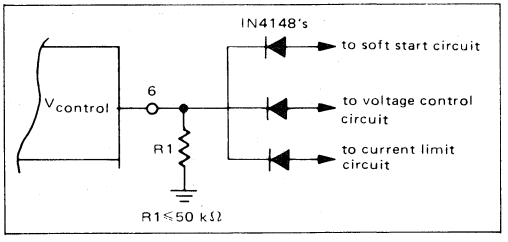
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is ≤ 50 kΩ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \cong \frac{V_{Control} - 2}{4} \times 100 \quad \text{(Eq. 2)}$$

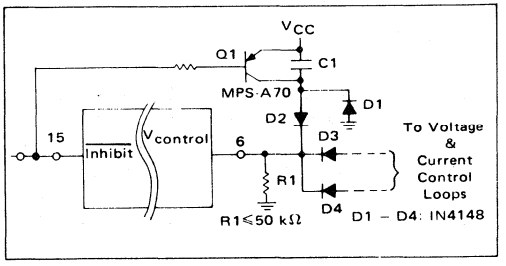
FIGURE 25



Soft Start

In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 26.

FIGURE 26



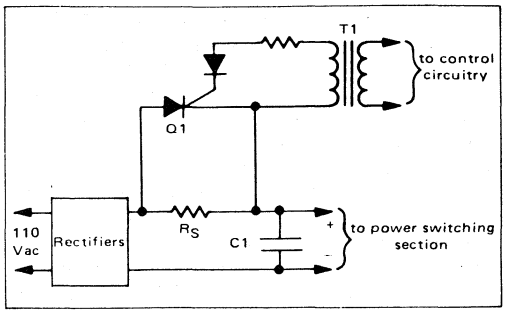
After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from V_{CC} toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power (V_{CC}) is turned off.

Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 27.

In this circuit, a series resistor, R_S, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts R_S out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary

FIGURE 27

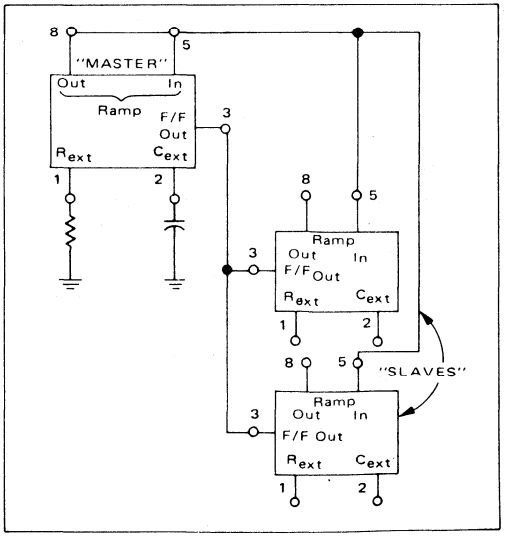


to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 28. By omitting their R_{ext} and C_{ext}, up to two MC3420s may be slaved to a master MC3420.

FIGURE 28 – SLAVING THE MC3420



15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in}, at a frequency of ≅ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, fo is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o.

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC}, Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC}; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≅ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≅ 5 μs each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

FIGURE 29 – 15 V, 2A DC-TO-DC CONVERTER

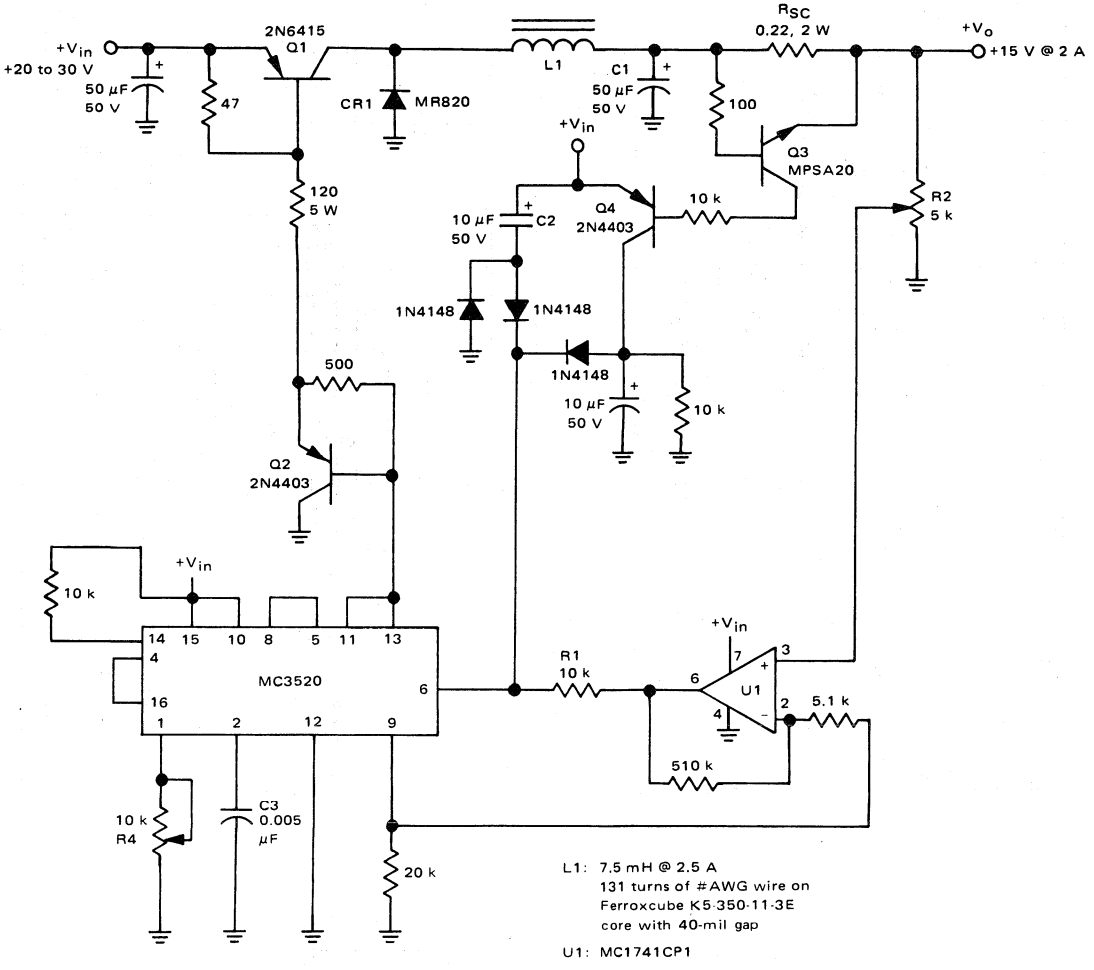
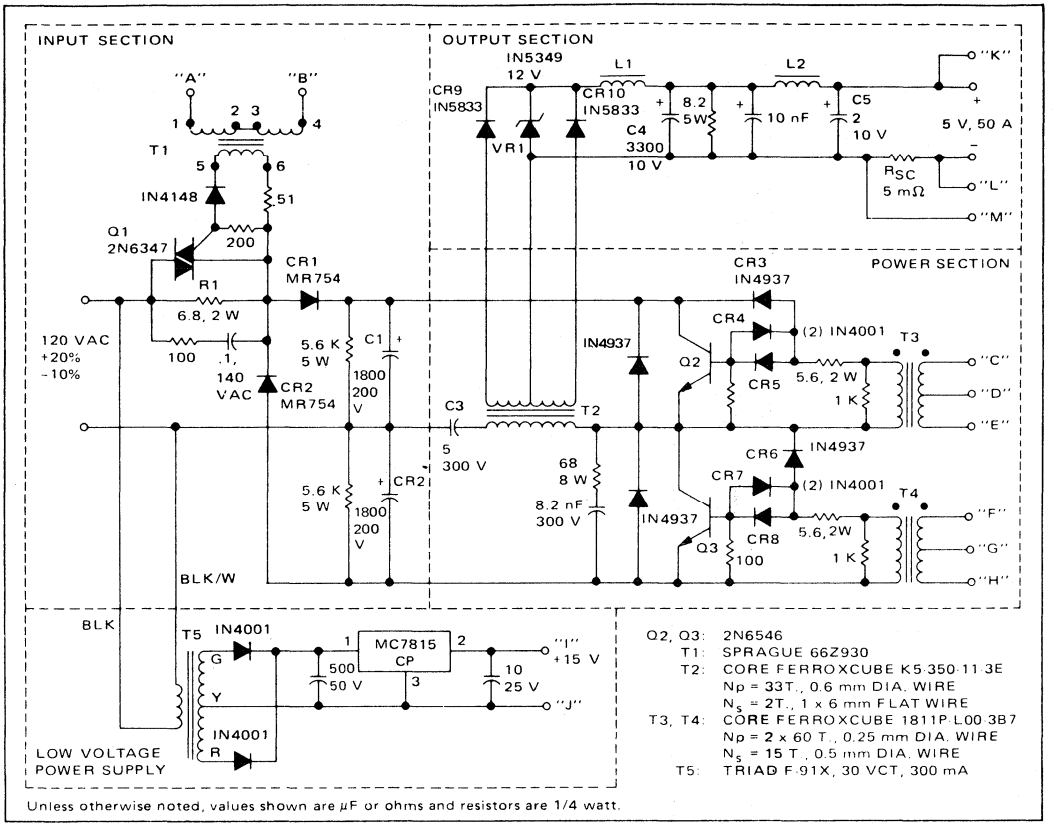


FIGURE 30a – 5 V, 50A LINE-OPERATED SUPPLY (continued on following page)

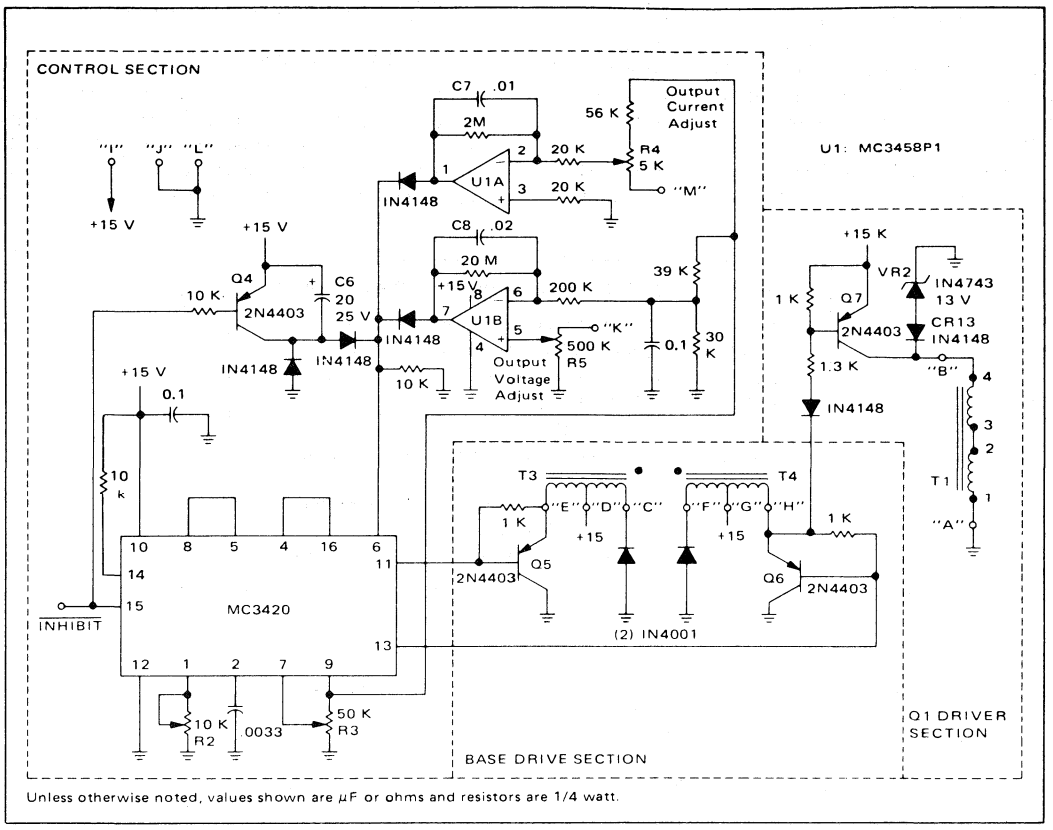


Q2, Q3: 2N6546
T1: SPRAGUE 66Z930
T2: CORE FERROXCUBE K5.350.11.3E
Np = 33T., 0.6 mm DIA. WIRE
N_S = 2T., 1 x 6 mm FLAT WIRE
T3, T4: CORE FERROXCUBE 1811P.L00.3B7
Np = 2 x 60 T., 0.25 mm DIA. WIRE
N_S = 15 T., 0.5 mm DIA. WIRE
T5: TRIAD F-91X, 30 VCT, 300 mA

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

Performance	
Line Regulation:	0.4%
Load Regulation:	0.25%
Output Ripple and Noise:	60 mV p-p
	25 mV rms
Line current surge at turn-on:	35 A max
Efficiency:	80%

FIGURE 30b



Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

Series Configuration

The single transistor series configuration is shown in Figure 1A. This configuration is usually limited to applications in which $0.2\ V_{CC} < V_o < 0.8\ V_{CC}$ and where input-output isolation is not required.

Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC}, and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors which have twice the current and half the voltage requirements as those of the push-pull configuration.

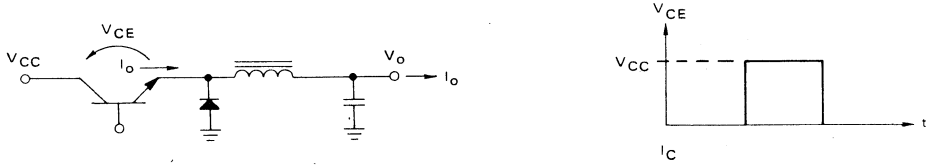
Full-Bridge Configuration

By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C:	Switching transistor collector current
V_{CE}:	Switching transistor collector-to-emitter-voltage
P_{in}:	Average input power
D.C.:	Inverter duty cycle
V_{CC}:	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX}:	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A – SERIES CONFIGURATION



TRANSISTOR REQUIREMENTS*

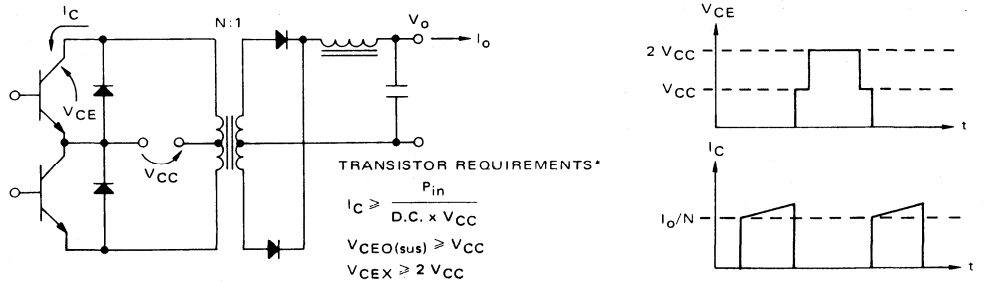
$I_C \geq I_o$

$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 2A – PUSH-PULL CONFIGURATION



TRANSISTOR REQUIREMENTS*

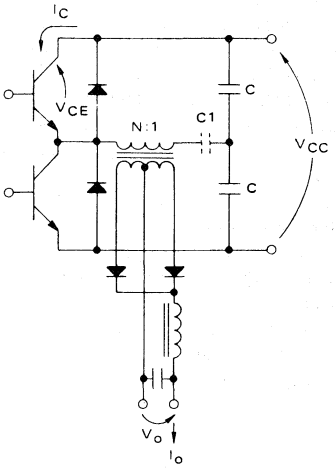
$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$

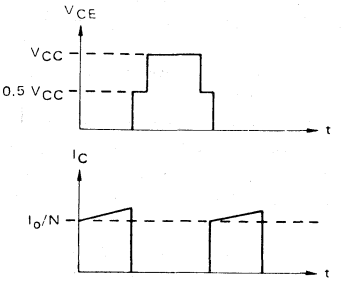
$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq 2\ V_{CC}$

*See explanation of abbreviations in text.

FIGURE 3A – HALF-BRIDGE CONFIGURATION





TRANSISTOR REQUIREMENTS*

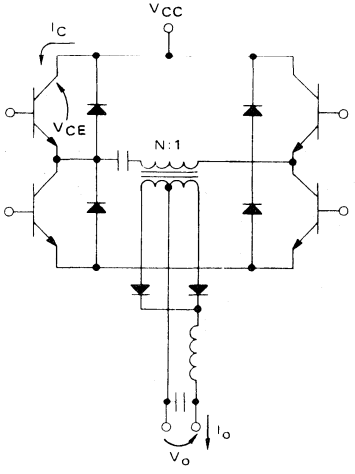
$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

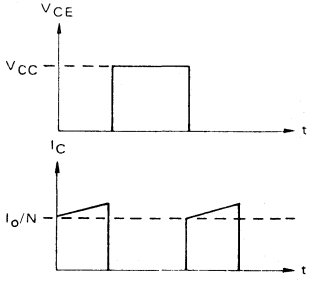
$V_{CEO(sus)} \geq V_{CC}/2$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 4A – FULL-BRIDGE CONFIGURATION





TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$V_{CEO(sus)} \geq V_{CC}$

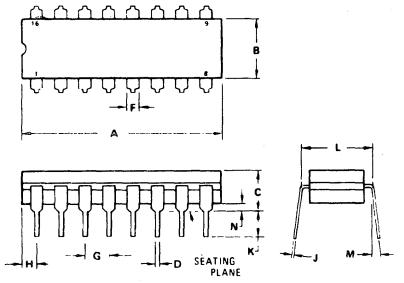
$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

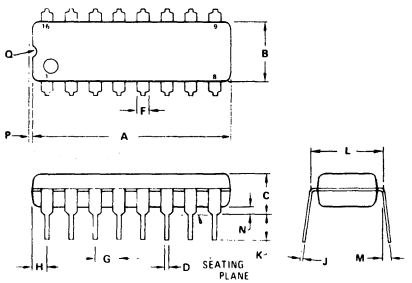
1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion,* March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion,* March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hetterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2,* October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3,* June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 620
$R_{\theta JA}$=100°C/W



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

P SUFFIX
PLASTIC PACKAGE
CASE 648
$R_{\theta JA}$=100°C/W

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geqslant I_C V_{CC}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_C = Total Sink Current

V_{CC} = Supply Voltage

Specifications and Applications Information

DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1555/MC1455 Timer

FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

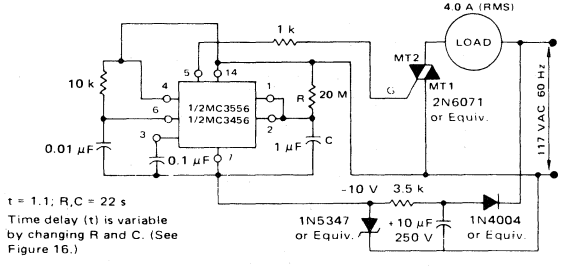
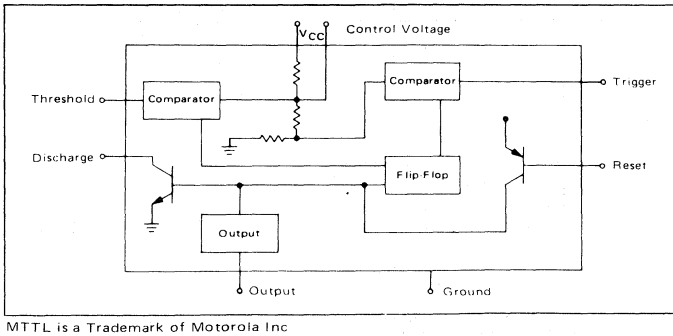


FIGURE 2 – BLOCK DIAGRAM (1/2 SHOWN)

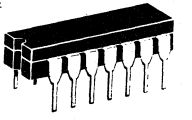


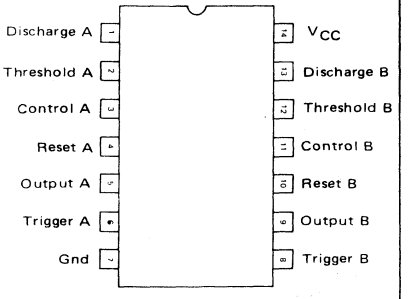
MTTL is a Trademark of Motorola Inc

DUAL TIMING CIRCUIT

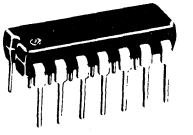
SILICON MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116





P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3456 only)



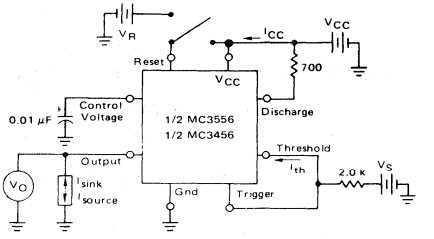
TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range MC3556	T_A	-55 to +125	°C
MC3456		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)
a. When V_S > 2/3 V_{CC}, V_O is low.
b. When V_S < 1/3 V_{CC}, V_O is high.
c. When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into discharge pin. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC3556			MC3456			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current (Per timer, double for both halfs)	I_{CC}							mA
V_{CC} = 5.0 V, R_L = ∞		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, R_L = ∞		–	10	11	–	10	14	
Low State, (Note 1)								
Timing Error (Note 2)								
Monostable Mode								
R_A = 2.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 μF		–	0.5	1.5	–	0.75	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.15	0.2	–	0.1	–	%/Volt
Astable Mode								
R_A = R_B = 2.0 kΩ to 100 kΩ								
C = 0.01 μF								
Initial Accuracy		–	1.5	–	–	2.25	–	%
Drift with Temperature		–	90	–	–	150	–	PPM/°C
Drift with Supply Voltage		–	0.15	–	–	0.3	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	μA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.03	0.1	–	0.03	0.1	μA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							V
(V_{CC} = 15 V)								
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.25	–	2.0	2.75	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Toggle Rate (Figures 17, 19)								
R_A = 3.3 kΩ, R_B = 6.8 kΩ, C = 0.003 μF	–	–	100	–	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns
Matching Characteristics Between Sections (Monostable)								
Initial Timing Accuracy		–	0.05	0.1	–	0.1	0.2	%
Timing Drift with Temperature		–	±10	–	–	±10	–	ppm/°C
Drift with Supply Voltage		–	0.1	0.2	–	0.2	0.5	%/V

NOTES: 1. Supply current when output is high is typically 2.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 megohms.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

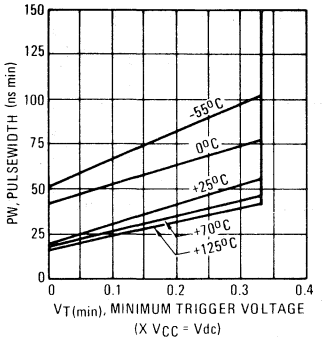


FIGURE 5 – SUPPLY CURRENT

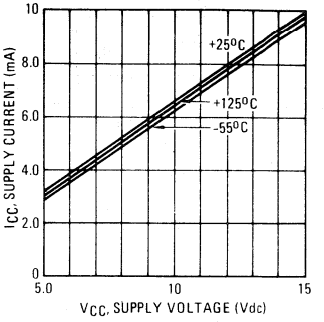


FIGURE 6 – HIGH OUTPUT VOLTAGE

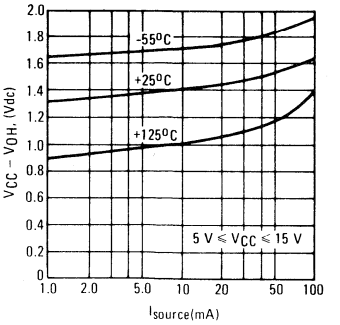


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

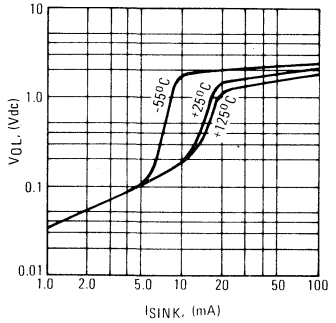


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

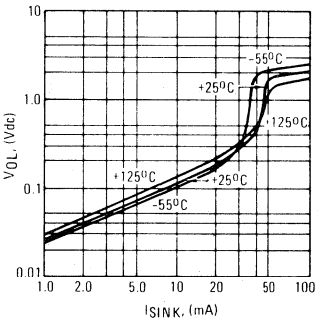


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

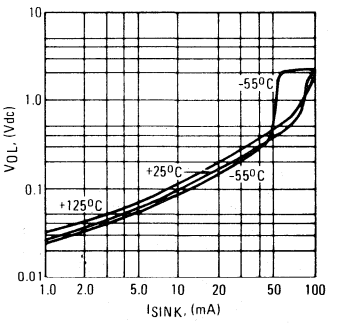


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

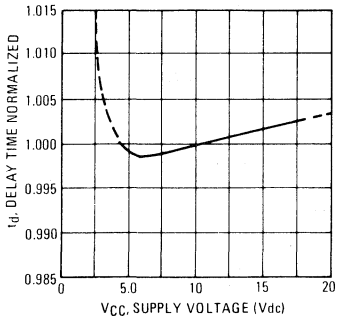


FIGURE 11 – DELAY TIME versus TEMPERATURE

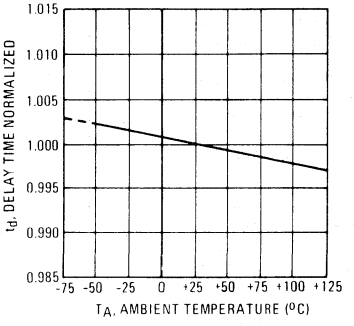
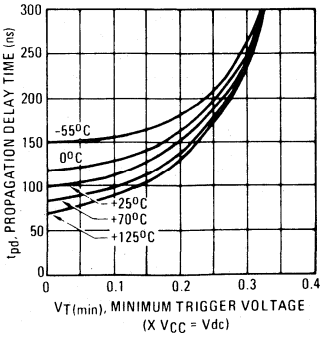


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



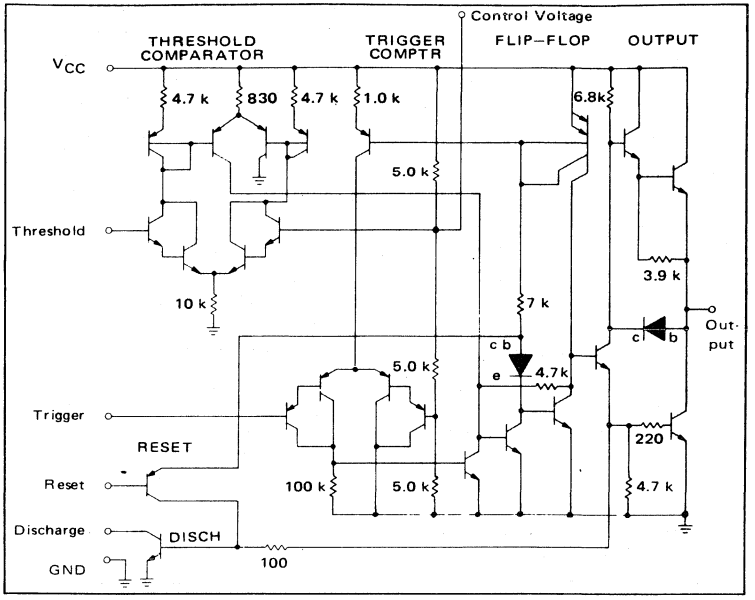


FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC

GENERAL OPERATION

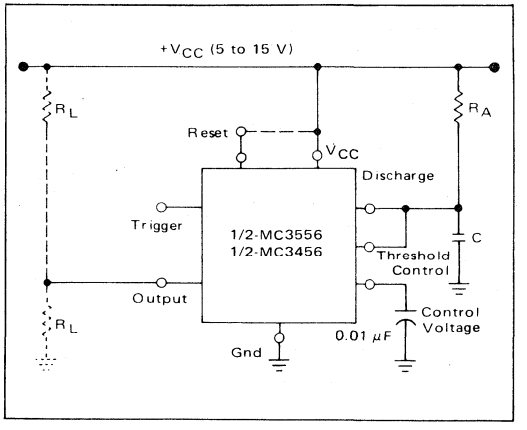
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

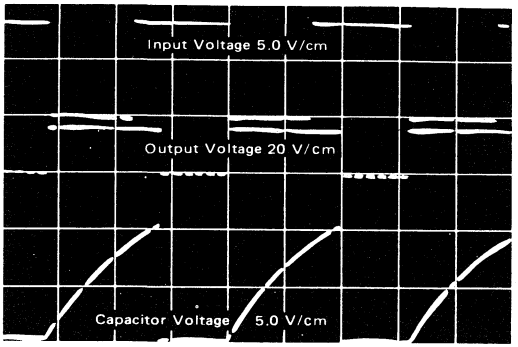
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT



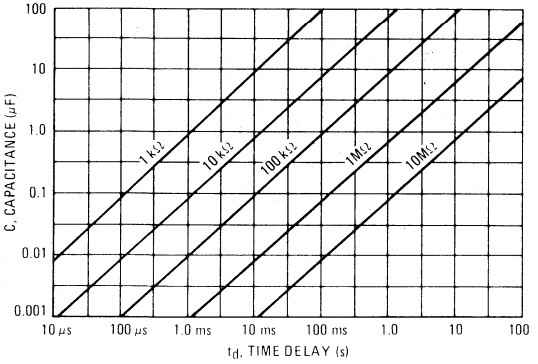
GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm
(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\,(Vdc)}{I_7\,(A)} \geq \frac{V_{CC}\,(Vdc)}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

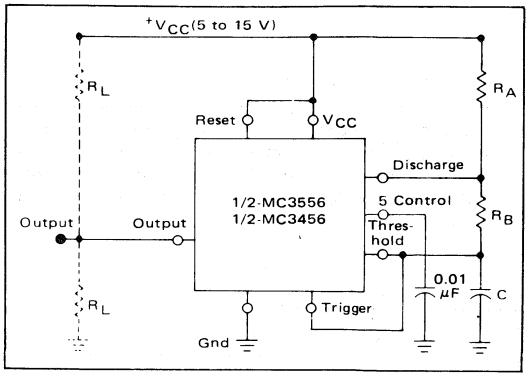
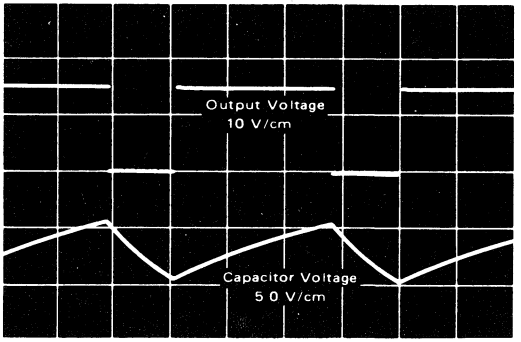
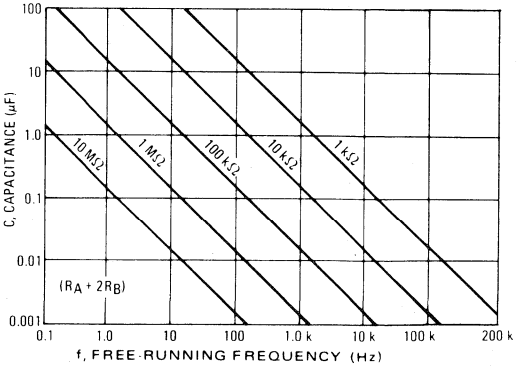


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm
(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

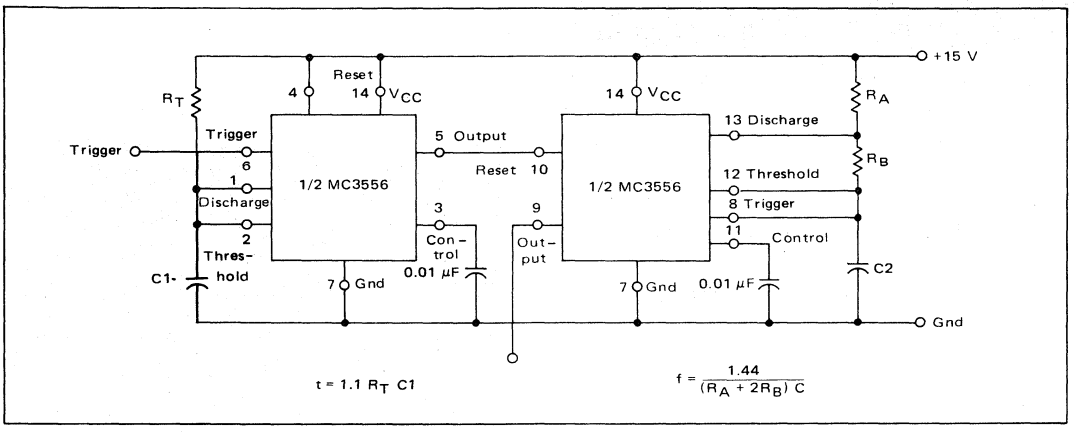
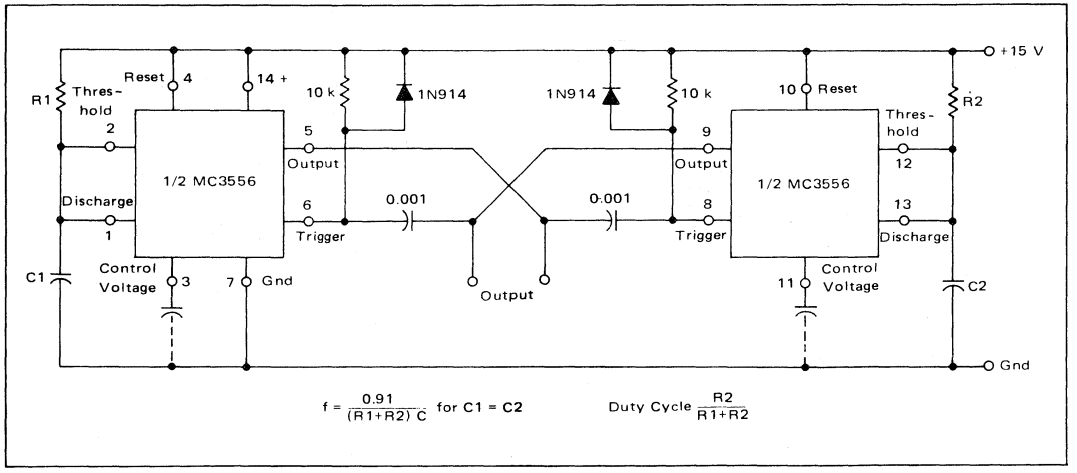


FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

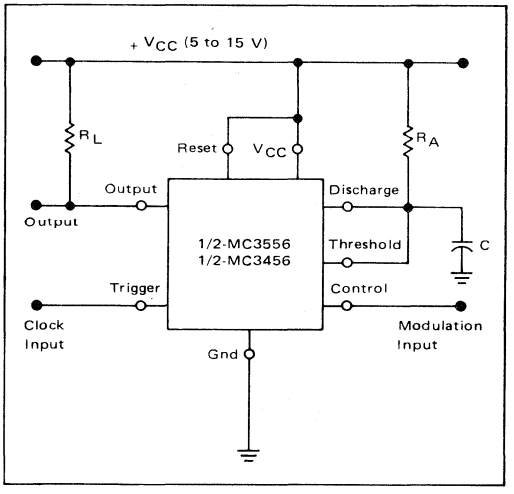
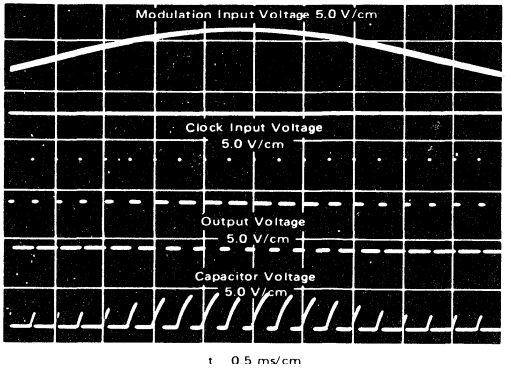


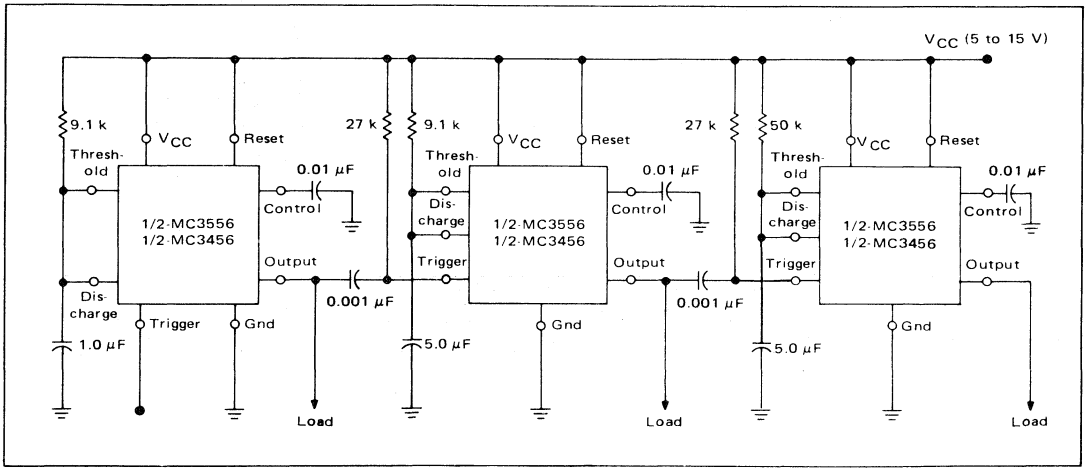
FIGURE 23 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)



Test Sequences

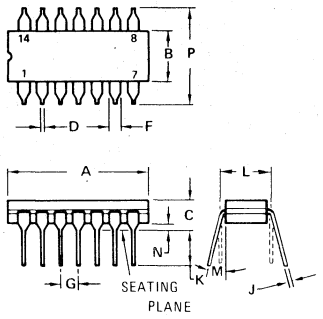
Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24



OUTLINE DIMENSIONS

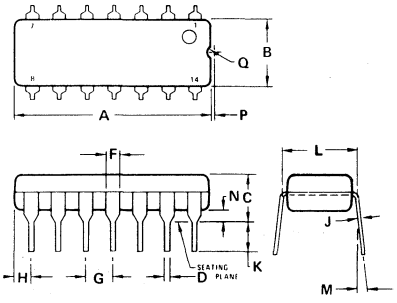
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3456 only)



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

REMOTE CONTROL RECEIVER

The MC6525 is a remote control receiver circuit in NMOS technology. The following 27 different functions are available out of the 22 channel system:

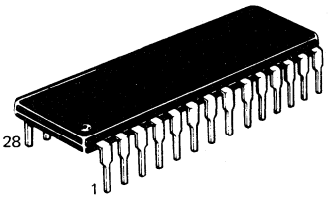
12 Programs
6 Analogue (3 controls ±)
1 Standby
2 General purpose
1 Sound killer
1 Strobe
1 Automatic sound mute
2 Separate outputs for program 8 & 12
(e.g. for dual standard switching)
1 Automatic switch-on from Standby whenever a program is selected at the transmitter.

ADDITIONAL FEATURES

- High input sensitivity (250 mVrms)
- Repetitive reading of up to 8 times the incoming time multiplex signal for good noise immunity.
- Internal UP/DOWN counter for front panel program sequencing
- Designed to be used in conjunction with the remote control transmitter MC14422

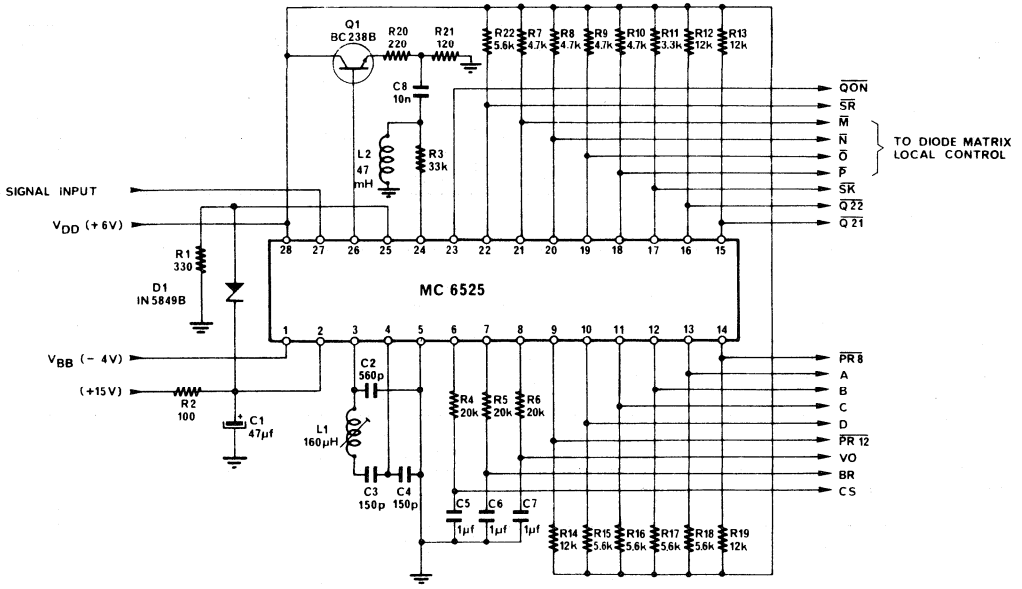
MOS
(N-CHANNEL, METAL–GATE)

REMOTE CONTROL RECEIVER



PLASTIC PACKAGE
CASE 710-01

FIGURE 1 – MC6525 TYPICAL CIRCUIT CONFIGURATION



MAXIMUM RATINGS (T_A = 25 °C)

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltages	V_{BB} V_{DD} V_{GG}	−2 to −6 −.3 to 10 −.3 to 20	Vdc Vdc Vdc
Input Voltage, all Inputs	V_{in}	0 to 15	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, V_{GG} = 13V ± 1V unless otherwise specified, T_A = 0 to 70 °C)

CHARACTERISTIC	PIN	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
DC Supply voltage	1 28 2	V_{BB} V_{DD} V_{GG}		−3.6 5.4 11	−4 6 12	−4.4 6.6 14	V
DC Supply current	1 28 2	I_{BB} I_{DD} I_{GG}				−0.5 60 20	mA
Local control $\overline{MNOP}$ Input Voltage Current	18,19 20,21	V_{IL} V_{IH} I_{IH}	 Vin = 6.6V	 4.0 		1.5 20	V uA
Band pass filter Input Voltage Current	24	V_{IL} V_{IH} I_{IH}	 Vin = 6.6V	 V_{DD}−0.6 		1.5 V_{DD} 20	V uA
Reset Input Voltage Current	25	V_{IL} V_{IH} I_{IH} I_{IL}	 Vin = 6.6V Vin = 0V	 0.8 		0.2 20 −100	V uA
Signal Input Voltage Current	27	V_{SB} I_{IH} I_{IL}	 Vin = 6.6V Vin = 0V	250 		 100 −100	mVRMS uA
Oscillator Input Current	4	I_{IH} I_{IL}	Vin = 6.6V Vin = 0 V	+.01 −.01		2 −2	mA
Binary Coded Output Current (open drain)	10,11 12,13	I_{OL} I_{OH}	V_{OL} = 0,5V V_{OH} = 6.6V	1 		 20	mA uA
Extra Output Current (open drain)	9,14 15	I_{OL} I_{OH}	V_{OL} = 0.5V V_{OH} = 6.6V	0.5 		 20	mA uA
Bistable Output Current (open drain)	16,17	I_{OL} I_{OH}	V_{OL} = 1.6V V_{OH} = 6.6V	1.6 		 10	mA uA
Strobe Output Current (open drain)	22	I_{OL} I_{OH}	V_{OL} = 0.4V V_{OH} = 14V	1.0 		 20	mA uA
Brightness & Colour Saturation Output Current (Push-Pull)	7,6	I_{OL} I_{OH}	V_{OL} = 0.5V V=V_{DD}−0.5V	0.5 −0.5			mA
Volume Output Current (Push-Pull)	8	I_{OL} I_{OH}	V_{OL}=1.6V V=V_{DD}−1.6V	1.6 −1.6			mA
ON Output Current (Push-Pull)	23	I_{OL} I_{OH}	V_{OL}=1.5V V = V_{DD} −1 V	100 −1.0			uA mA
Oscillator Output Current (Push-Pull)	3	I_{OL} I_{OH}	V_{OL} = 2.0V V=V_{DD}−1V	0.5 −10			mA uA
Band Pass Filter Output (Push-Pull)	26	I_{OL} I_{OH}	V_{OL} = 0.5V V=V_{DD}−0.5V	0.5 −0.5			mA

INPUT/OUTPUT FUNCTIONS

$\overline{QON}$ – This output distinguishes between the ON and STANDBY mode. When the front panel input ON via the matrix is low (Fig. 3 & 4) or when a program is selected via the transmitter following a previous standby instruction, output $\overline{QON}$ changes to low. When the front panel input STB changes to low or when the STANDBY instruction is given from the transmitter, $\overline{QON}$ changes to high.
When the reset voltage input V_{RE} rises from 0 volt to the threshold voltage V_{ASP} (−0.2 to −0.8 Volts) the output $\overline{QON}$ goes high. To insure that supply voltages have already reached their nominal value by this time a slight time delay is introduced by C1 and the 10 V zener D1 (refer to Fig. 1).

$\overline{MNOP}$ – Instructions performed from the front panel should be addressed via a matrix to these four inputs (see Fig. 3 & 4). Bounce protection is provided internally. Discrete pull up resistors are required on input $\overline{MNOP}$.
The program counter can be incremented or decremented in steps of 1 by applying a low on the appropriate inputs to the diode matrix PR + or PR – (see Fig. 4). The program counter has overflow & underflow capability. It is always preset to all low (program 1) if the receiver set is switched from mode OFF to ON. If the TV set is switched from STANDBY to ON, then the last operated program is selected.

$\overline{PR8}$ & $\overline{PR12}$ – These outputs change to a low during the time that program 8 (for $\overline{PR8}$) or program 12 (for $\overline{PR12}$) appear at the output ABCD. Multistandard switching capability is therefore readily available on two channels. Should it be performed for more than two channels additional external decoding circuitry is necessary.

$\overline{SK}$ – When controlling SK from the remote control transmitter using channel 20 or via the diode matrix input SK, the output $\overline{SK}$ will change alternatively to its complementary status on receipt of a command.
When the $\overline{SK}$ output is in the low mode, it is impossible to vary the volume control level VO.
If $\overline{SK}$ is in the low mode (sound killer operating) a channel change or an ON command will return it to a high.

$\overline{SR}$ – Strobe output. During all 12 program changes a pulse will appear at the output $\overline{SR}$ (fig. 5). Therefore $\overline{SR}$ can be used to defete AFC during program selection via the transmitter, via inputs PR+, PR– and during switch on, or to control on screen display device as necessary.

$\overline{Q21}$ – General purpose output. By operation of remote channel 21 or by selecting the equivalent diode matrix input, the open drain output $\overline{Q21}$ changes to low impedance as long as the command is present.

$\overline{Q22}$ – General purpose output. If the remote control receiver is switched on from standby, output $\overline{Q22}$ will change from low to high. By operating the remote control channel 22 or by selecting the equivalent diode matrix input, $\overline{Q22}$ output will change to its complementary status. This can be used for the control of ancillary equipment. (e.g. VTR, information systems and so on.)

BR – VO – CS – Brightness, Volume, Colour Saturation analogue control voltage outputs.
These voltages are obtained by integrating the output signals through a low pass filter (R4 C5, R5 C6, R6 C7 in Fig. 1).
The analogue control voltage is then proportional to the duty cycle of the outputs, with a repetition frequency of 20.3 KHz.
The D/A converter resolution has been chosen to be 60 steps Its value can be incremented or decremented in steps of 1. The analogue voltage can be varied up/down, at a speed of approximately 10 step/sec. The D/A conversion is performed with an underflow and overflow limiting circuit.
Output VO is automatically muted during channel switching when in standby mode, or when $\overline{SR}$ output is low (see timing table, fig. 5).
If the receiver is switched from the OFF mode to the ON mode or after a power interruption (reset V_{RE} rises from 0 volt to V_{ASP}) then BR & CS will be set to 50% of their value and VO to 35% (middle position).
Preset to middle position can also be performed via the diode matrix input MID or via the remote control by connecting the Q21 output to the MID key of the diode matrix via a suitable RC network.

A-B-C-D – Binary coded program number plus one outputs. They are open drain outputs requiring external discrete pull up resistors. Refer to Fig. 2 for coded program number output.

FIGURE 2 – TABLE OF INSTRUCTIONS

FUNCTION	RECEIVED FREQUENCIES FROM REMOTE CONTROL						DIODE MATRIX				PROGRAM OUTPUT CODE			
	CHANNEL	f_a	f_b	f_c	f_d	f_e	$\overline{M}$	$\overline{N}$	$\overline{O}$	$\overline{P}$	A	B	C	D
Program + ON														
1	1	0	0	0	0	1					0	0	0	0
2	2	1	0	0	0	1					1	0	0	0
3	3	0	1	0	0	1					0	1	0	0
4	4	1	1	0	0	1					1	1	0	0
5	5	0	0	1	0	1					0	0	1	0
6	6	1	0	1	0	1					1	0	1	0
7	7	0	1	1	0	1					0	1	1	0
8	8	1	1	1	0	1					1	1	1	0
9	9	0	0	0	1	1					0	0	0	1
10	10	1	0	0	1	1					1	0	0	1
11	11	0	1	0	1	1					0	1	0	1
12	12	1	1	0	1	1					1	1	0	1
Colour saturation CS –	13	0	1	0	0	0	1	0	1	1				
Colour saturation CS +	14	1	1	0	0	0	0	0	1	1				
Volume VO –	15	0	0	1	0	0	1	1	0	1				
Volume VO +	16	1	0	1	0	0	0	1	0	1				
Brightness BR –	17	0	1	1	0	0	1	0	0	1				
Brightness BR +	18	1	1	1	0	0	0	0	0	1				
Standby STB	19	0	0	0	1	0	1	1	1	0				
Sound killer SK	20	1	0	0	1	0	0	1	1	0				
General Purpose Q21	21	0	1	0	1	0	1	0	1	0				
General Purpose Q22	22	1	1	0	1	0	0	0	1	0				
Program counter PR +							1	1	0	0				
Program counter PR –							0	1	0	0				
Middle position MID							1	0	0	0				
Power ON							0	1	1	1				
*TEST							0	0	0	0				

* The code 0000 is used for device testing purposes only before shipment of MC6525 to customers.

ULTRASONIC INPUT FREQUENCIES

f_a = 34.688 KHz
f_b = 36.048 KHz
f_c = 37.519 KHz
f_d = 39.116 KHz
f_e = 42.755 KHz

FIGURE 3 – MC6525 BLOCK DIAGRAM

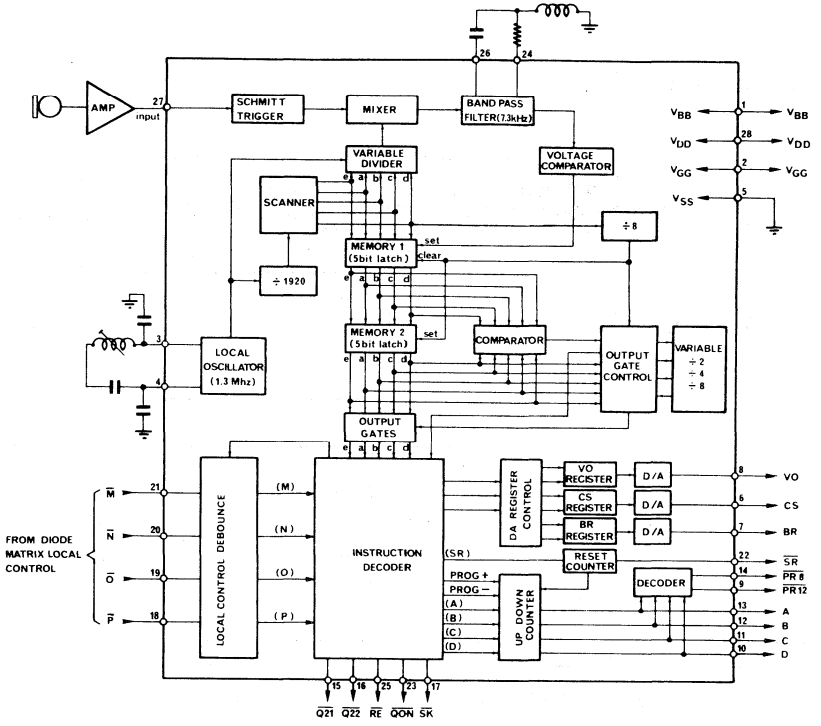
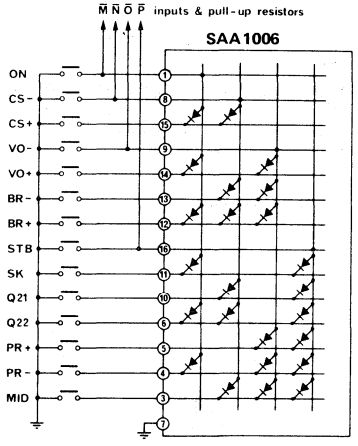


FIGURE 4 – DIODE MATRIX



This instruction encoding is performed by the Motorola IC: SAA1006.

FIGURE 5 – TIMING DIAGRAM FOR CONTROL VIA TRANSMITTER

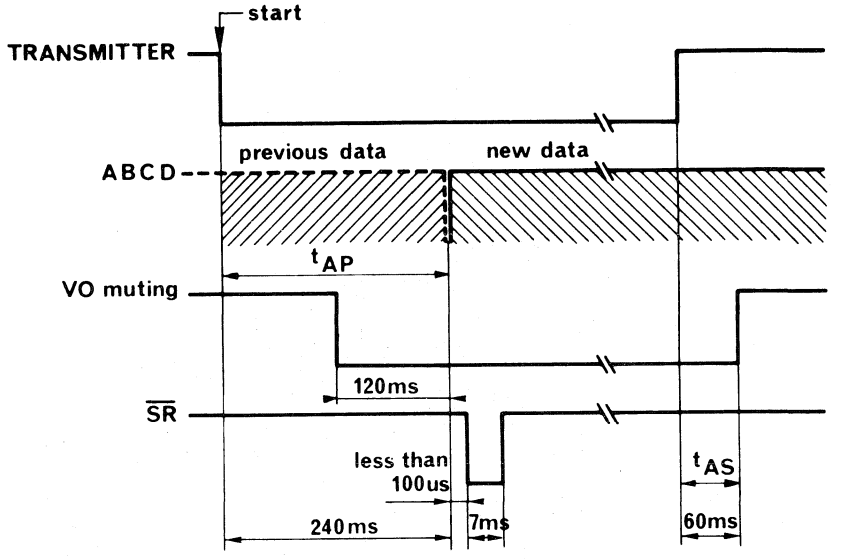
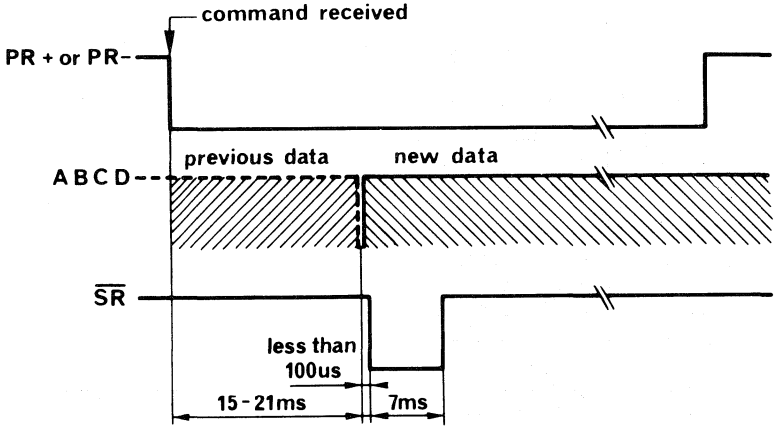
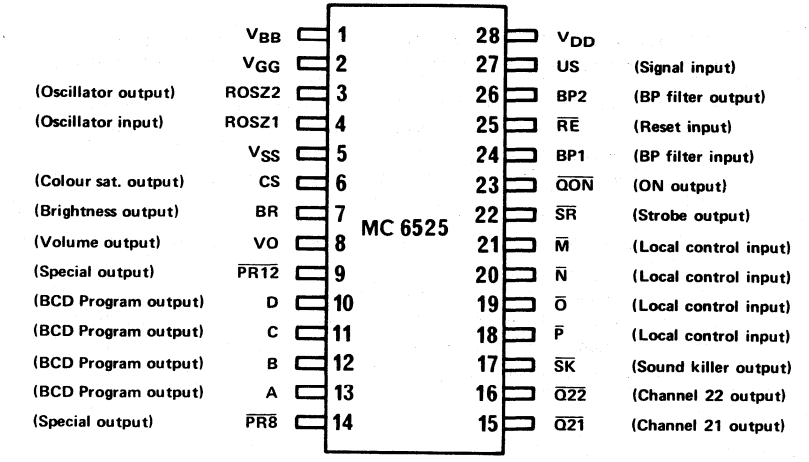


FIGURE 6 – TIMING DIAGRAM FOR CONTROL VIA DIODE MATRIX



Time required to switch "ON" or "STANDBY"	T_{AE} = 480 mS Typ.
Time required to change program	T_{AP} = 240 mS Typ.
Time required for other functions	T_{AA} = 120 mS Typ.
Delay time at the end of command	T_{AS} = 60 mS Typ.

FIGURE 7 – PIN ASSIGNMENT



EXTERNAL COMPONENT INFORMATION

L1: 160 μH, ad., Q $\geqslant$ 60, suggested supplier: TOKO-7BO-A2896HM
L2: 47 mH ± 5%, fixed, Q $\geqslant$ 100, suggested supplier: TOKO-181LY-473J
C2: 560 pF ± 10%
C3, C4: 150 pF ± 10%
C8: 10 nF ± 5%
All resistors: ± 5%

RECOMMENDED SETTING UP PROCEDURE

1. Reference oscillator and IF bandwidth

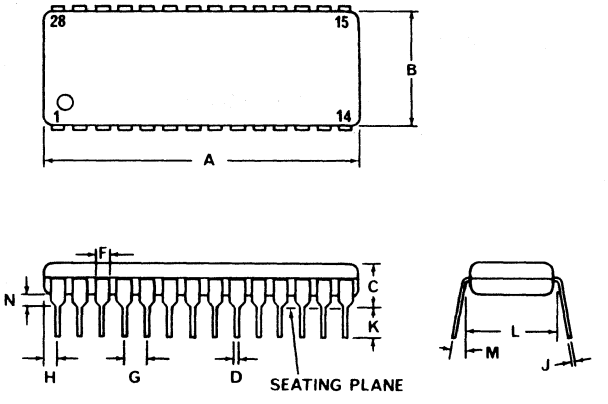
1.1. With reference to Fig. 1, connect pin 27 (Signal input) to a sine-wave oscillator set at 42755Hz (corresponding to f_e) and 5Vp/p of amplitude.

1.2. With an oscilloscope connected to pin 24 adjust L1 for maximum IF filter output. To insure the right frequency setting of the reference oscillator (approx: 1.3MHz) check the VO output pin 8 to go LOW (muted) and the $\overline{QON}$ output pin 23 to stay LOW while making this adjustment.

1.3. If desired it is now possible to check the receiver bandwidth by monitoring VO output.
Whenever channel 1 (f_e) is acquired the analogue voltage for the volume control will be muted (0 volt), therefore by varying f_e around the mean value of 42,755KHz it is possible to check the bandwidth of the receiver to be approximately ± 450Hz.

PACKAGE DIMENSIONS

PLASTIC PACKAGE
CASE 710-01



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

REMOTE CONTROL RECEIVER

The MC6526 is a remote control receiver circuit in NMOS technology. The following 46 different functions are available out of the 22 channel system:

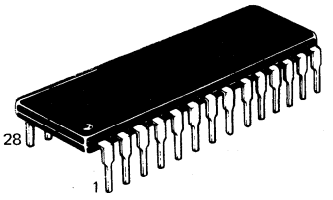
32 Programs (also 8 or 16)
6 Analogue (3 controls ±)
1 Standby
2 General purpose
1 Sound killer
1 Strobe
1 Automatic sound mute
1 Middle position mode
1 Automatic switch-on from Standby whenever a program is selected at the transmitter.

ADDITIONAL FEATURES

- High input sensitivity (250 mVrms)
- Repetitive reading of up to 8 times the incoming time multiplex signal for good noise immunity.
- Internal UP/DOWN counter for front panel program sequencing.
- Designed to be used in conjunction with the remote control transmitter MC14422

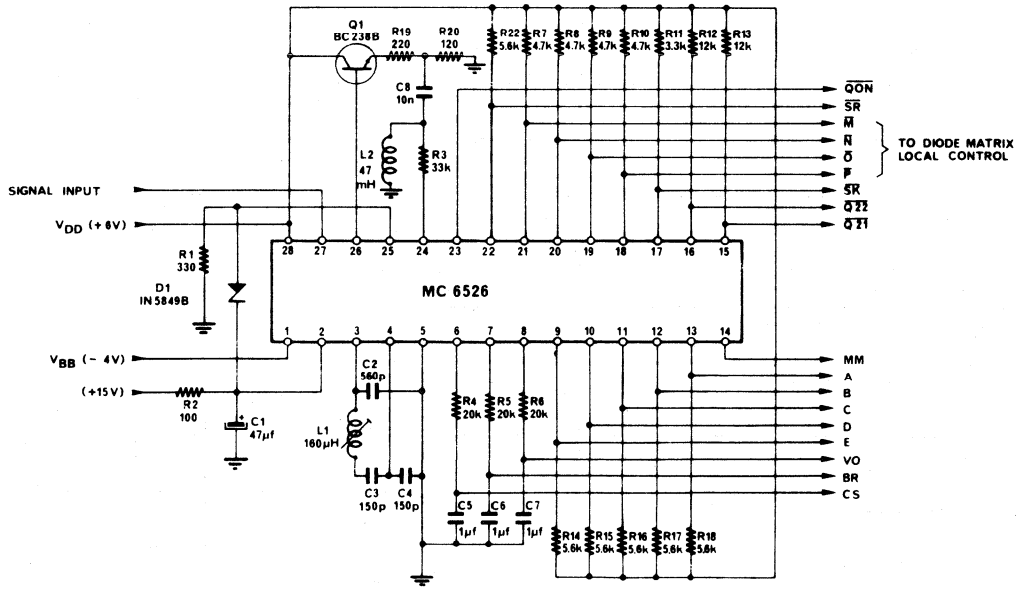
MOS
(N-CHANNEL, METAL–GATE)

REMOTE CONTROL RECEIVER



PLASTIC PACKAGE
CASE 710-01

FIGURE 1 – MC6526 TYPICAL CIRCUIT CONFIGURATION



MAXIMUM RATINGS (T_A = 25 °C)

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltages	V_{BB} V_{DD} V_{GG}	−2 to −6 −.3 to 10 −.3 to 20	Vdc Vdc Vdc
Input Voltage, all Inputs	V_{in}	0 to 15	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, V_{GG} = 13 V ± 1 V unless otherwise specified, T_A = 0 to 70 °C)

CHARACTERISTIC	PIN	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
DC Supply voltage	1 28 2	V_{BB} V_{DD} V_{GG}		−3.6 5.4 11	−4 6 12	−4.4 6.6 14	V
DC Supply current	1 28 2	I_{BB} I_{DD} I_{GG}				−0.5 60 20	mA
Local control $\overline{MNOP}$ input Voltage Current	18,19 20,21	V_{IL} V_{IH} I_{IH}	 Vin = 6.6V	 4.0 	 	1.5 20	V uA
Band pass filter Input Voltage Current	24	V_{IL} V_{IH} I_{IH}	 Vin= 6.6V	 V_{DD}−0.6 	 	1.5 V_{DD} 20	V uA
Reset Input Voltage Current	25	V_{IL} V_{IH} I_{IH} I_{IL}	 Vin = 6.6V Vin = 0V	 0.8 	 	0.2 20 −100	V uA
Signal Input Voltage Current	27	V_{SB} I_{IH} I_{IL}	 Vin = 6.6V Vin = 0V	250 	 	 100 −100	mVRMS uA
Oscillator Input Current	4	I_{IH} I_{IL}	Vin = 6.6V Vin = 0 V	+.01 −.01		2 −2	mA
Binary Coded Output Current (open drain)	9, 10, 11 12,13	I_{OL} I_{OH}	V_{OL} = 0.5V V_{OH} = 6.6V	1 	 	 20	mA uA
Extra Output Current (open drain)	15, 16	I_{OL} I_{OH}	V_{OL} = 0.5V V_{OH} = 6.6V	0.5 	 	 20	mA uA
Bistable Output Current (open drain)	17	I_{OL} I_{OH}	V_{OL} = 0,5V V_{OH} = 6.6V	0.5 	 	 10	mA uA
Strobe Output Current (open drain)	22	I_{OL} I_{OH}	V_{OL} = 0.4V V_{OH} = 14V	1.0 	 	 20	mA uA
Brightness, Colour Saturation & Volume output Current (Push-Pull)	7,6 8	I_{OL} I_{OH}	V_{OL} = 0.5V V = V_{DD} −0.5 V	0.5 −0.5	 	 	mA
Middle Position Mode Input Voltage Current	14	V_{IL} V_{IH} I_{IH}	 V_{IN}= 6.6V	 5.0 	 	0.5 20	V uA
ON Output Current (Push-Pull)	23	I_{OL} I_{OH}	V_{OL} = 1.5V V=V_{DD}−1.0V	100 −1.0	 	 	uA mA
Oscillator Output Current (Push-Pull)	3	I_{OL} I_{OH}	V_{OL} = 2.0V V=V_{DD}−2V	0.5 −10	 	 	mA uA
Band Pass Filter Output (Push-Pull)	26	I_{OL} I_{OH}	V_{OL} = 0.5V V= V_{DD}−0.5V	2.0 −2.0	 	 	mA

INPUT/OUTPUT FUNCTIONS

$\overline{QON}$ – This output distinguishes between the ON and STANDBY mode. When the front panel input ON via the matrix is low (fig. 3 & 4) or when a program is selected via the transmitter following a previous standby instruction, output $\overline{QON}$ changes to low. When the front panel input STB changes to low or when the STANDBY instruction is given from the transmitter, $\overline{QON}$ changes to high.
When the reset voltage input V_{RE} rises from 0 volt to the threshold voltage V_{ASP} (+0.2 to +0.8 Volts) the output $\overline{QON}$ goes high. To insure that supply voltages have already reached their nominal value by this time a slight time delay is introduced by C1 and the 10 V zener D1 (refer to fig. 1).

$\overline{M}$ $\overline{N}$ $\overline{O}$ $\overline{P}$ – Instructions performed from the front panel should be addressed via a matrix to these four inputs (see fig. 3 & 4). Bounce protection is provided internally. Discrete pull up resistor are required on input $\overline{MNOP}$.
The program counter can be incremented or decremented in steps of 1 by applying a low on the appropriate inputs to the diode matrix PR+ or PR– (see Fig. 4). The program counter has overflow & underflow capability. It is always preset to all low (program 1) if the receiver set is switched from mode OFF to ON. If the TV or RADIO set is switched from STANDBY to ON, then the last operated program is selected.

$\overline{Q21}$ & $\overline{Q22}$ – General purpose outputs. By operation of remote channels 21 and 22 or by selecting the equivalent diode matrix inputs, the open drain outputs $\overline{Q21}$ and $\overline{Q22}$ change to low impedance as long as the command is present. These outputs can be used to command an external UP/DOWN counter to perform a forth analogue function.

$\overline{SK}$ – When controlling $\overline{SK}$ from the remote control transmitter using channel 20 or via the diode matrix input $\overline{SK}$, the output $\overline{SK}$ will change alternatively to its complementary status on receipt of a command.
When the $\overline{SK}$ output is in the low mode, it is impossible to vary the volume control level VO.
If $\overline{SK}$ is in the low mode (sound killer operating) a channel change or an ON command will return it to a high.

$\overline{SR}$ – Strobe output. A pulse will appear at the output $\overline{SR}$ (Fig. 5) during any change at the program output code. Therefore for the 8 program applications, $\overline{SR}$ can be used to defeate AFC during program selection and switch-on, or to control on-screen display device as necessary. For 16 and 32 program, since double keying is necessary, two strobe pulses will identify the true program change. Therefore the first pulse, corresponding to the first keying can be used to kill the video and the audio signal, the second pulse will be used to bring picture and audio back in a toggle fation.

MM – Middle position mode input. When pin 14 is connected to V_{DD} (+6V) the automatic setting to middle position of the three analogue functions occurs when the receiver is switched ON from the OFF mode or after a power interruption.
When connected to ground the middle position setting is also performed whenever the MC6526 is switched ON from STANDBY.

BR - VO - CS – Brightness, Volume, Colour Saturation analogue control voltage outputs.
These voltages are obtained by integrating the output signals through a low pass filter (R4 C5, R5 C6, R6 C7 in fig. 1).
The analogue control voltage is then proportional to the duty cycle of the outputs, with a repetition frequency of 20.3 KHz.
The D/A converter resolution has been chosen to be 60 steps Its value can be incremented or decremented in steps of 1. The analogue voltage can be varied up/down, at a speed of approximately 10 step/sec. The D/A conversion is performed with an underflow and overflow limiting circuit.
Output VO is automatically muted during channel switching when in standby mode, or when SR output is low (see timing table, fig. 5).
If the receiver is switched from the OFF mode to the ON mode or after a power interruption (reset V_{RE} rises from 0 volt to V_{ASP}) then BR & CS will be set to 50% of their value and VO to 35% (middle position).
Preset to middle position can also be performed via the diode matrix input MID or via the remote control by connecting the Q21 output to the MID key of the diode matrix via a suitable RC network.

A-B-C-D-E–Binary coded program number plus one outputs. They are open drain outputs requiring external discrete pull up resistors. Refer to Fig. 2 for coded program number output.

NOTE that for an 8 program receiver outputs A, B, C will be used, for 16 program A, B, C, D and for 32 programs A, B, C, D, E.

FIGURE 2 – TABLE OF INSTRUCTIONS

FUNCTION	RECEIVED FREQUENCIES FROM REMOTE CONTROL						DIODE MATRIX				PROGRAM OUTPUT CODE				
	CHANNEL	f_a	f_b	f_c	f_d	f_e	M	N	O	P	A	B	C	D	E
1	1	0	0	0	0	1					0	0	0	X	X
2	2	1	0	0	0	1					1	0	0	X	X
3	3	0	1	0	0	1					0	1	0	X	X
4	4	1	1	0	0	1					1	1	0	X	X
5	5	0	0	1	0	1					0	0	1	X	X
6	6	1	0	1	0	1					1	0	1	X	X
7	7	0	1	1	0	1					0	1	1	X	X
8	8	1	1	1	0	1					1	1	1	X	X
W	9	0	0	0	1	1					X	X	X	0	0
X	10	1	0	0	1	1					X	X	X	1	0
Y	11	0	1	0	1	1					X	X	X	0	1
Z	12	1	1	0	1	1					X	X	X	1	1
Colour saturation CS–	13	0	1	0	0	0	1	0	1	1					
Colour saturation CS+	14	1	1	0	0	0	0	0	1	1					
Volume VO–	15	0	0	1	0	0	1	1	0	1					
Volume VO+	16	1	0	1	0	0	0	1	0	1					
Brightness BR–	17	0	1	1	0	0	1	0	0	1					
Brightness BR+	18	1	1	1	0	0	0	0	0	1					
Standby STB	19	0	0	0	1	0	1	1	1	0					
Sound killer SK	20	1	0	0	1	0	0	1	1	0					
General Purpose Q21	21	0	1	0	1	0	1	0	1	0					
General Purpose Q22	22	1	1	0	1	0	0	0	1	0					
Program counter PR+							1	1	0	0					
Program counter PR–							0	1	0	0					
Middle position MID							1	0	0	0					
Power ON							0	1	1	1					
* TEST							0	0	0	0					

X: no change

* The code 0000 is used fos device testing purposes only before shipment.

ULTRASONIC INPUT FREQUENCIES

f_a = 34.688 KHz
f_b = 36.048 KHz
f_c = 37.519 KHz
f_d = 39.116 KHz
f_e = 42.755 KHz

FIGURE 3 – MC6526 BLOCK DIAGRAM

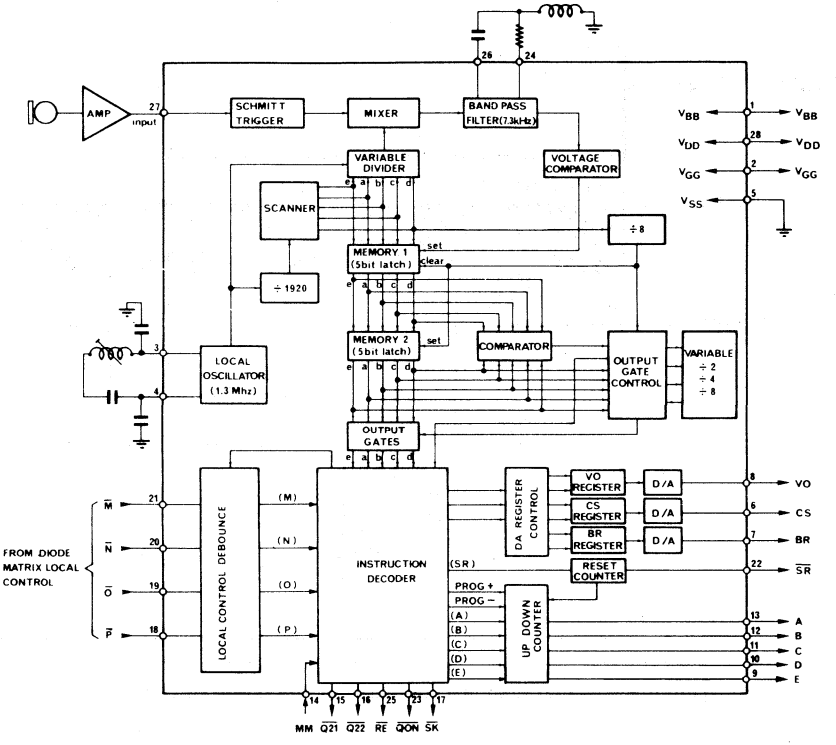
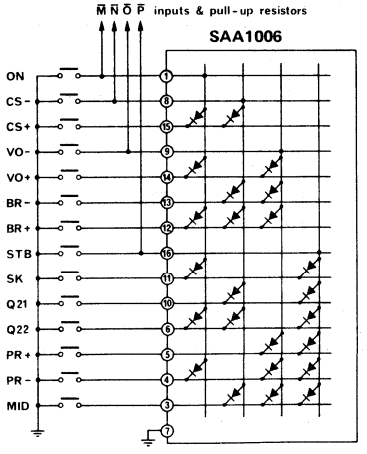


FIGURE 4 – DIODE MATRIX



This instruction encoding is performed by the Motorola IC: SAA1006.

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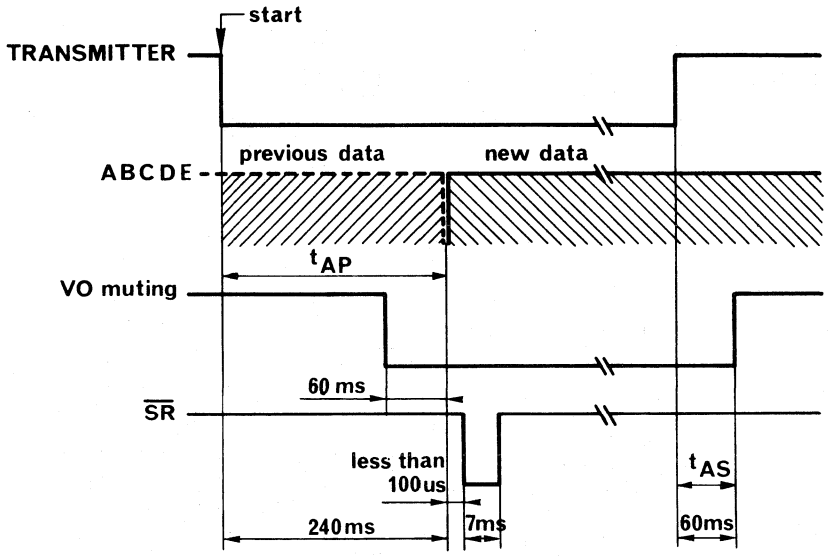
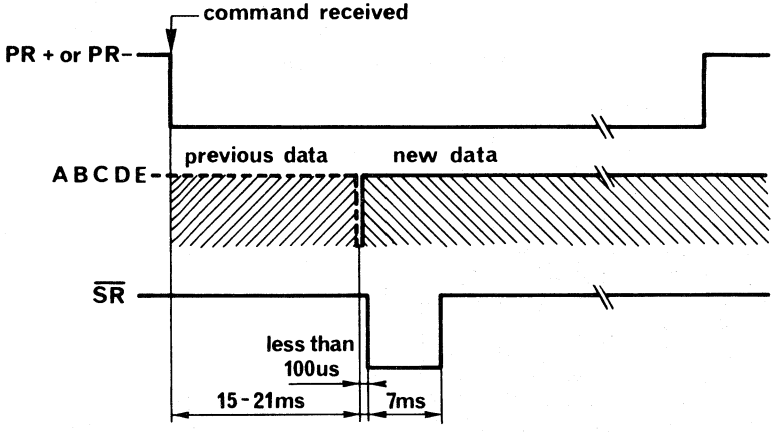
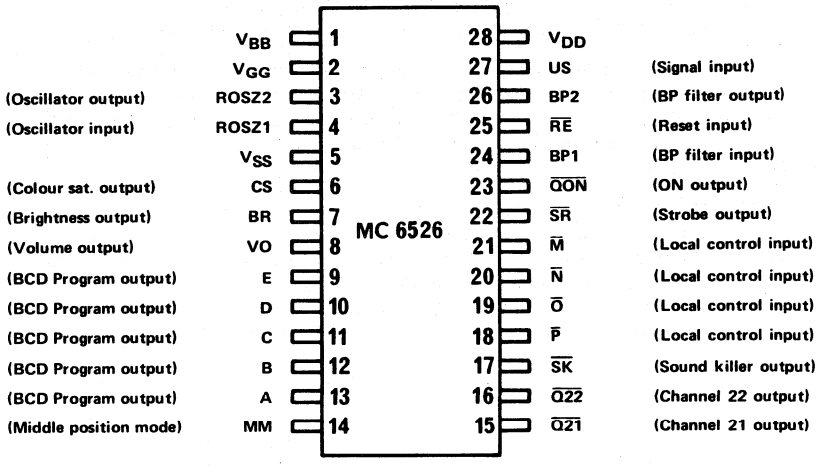


FIGURE 6 – TIMING DIAGRAM FOR CONTROL VIA DIODE MATRIX



Time required to switch "ON" or "STANDBY"	T_{AE} = 480 mS Typ
Time required to change program and to operate channels 20, 21, 22	T_{AP} = 240 mS Typ
Time required to operate analogue outputs	T_{AA} = 120 mS Typ
Delay time at the end of command	T_{AS} = 60 mS Typ

FIGURE 7 – PIN ASSIGNMENT



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C2: 560 pF ± 10%
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C8: 10 nF ± 5%
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RECOMMENDED SETTING UP PROCEDURE

1. Reference oscillator and IF bandwidth

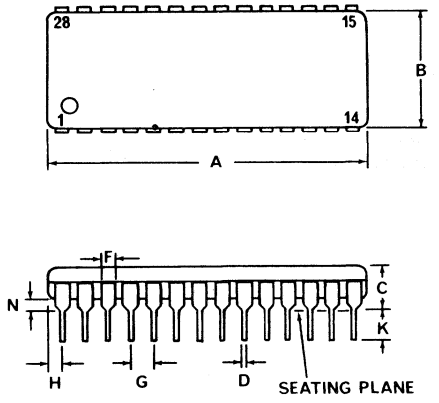
1.1. With reference to Fig. 1, connect pin 27 (Signal input) to a sine-wave oscillator set at 42755Hz (corresponding to f_e) and 5Vp/p of amplitude.

1.2. With an oscilloscope connected to pin 24 adjust L1 for maximum IF filter output. To insure the right frequency setting of the reference oscillator (approx: 1.3MHz) check the VO output pin 8 to go LOW (muted) and the $\overline{QON}$ output pin 23 to stay LOW while making this adjustment.

1.3. If desired it is now possible to check the receiver bandwidth by monitoring VO output.
Whenever channel 1 (f_e) is acquired the analogue voltage for the volume control will be muted (0 volt), therefore by varying f_e around the mean value of 42,755KHz it is possible to check the bandwidth of the receiver to be approximately ± 450Hz.

PACKAGE DIMENSIONS

PLASTIC PACKAGE
CASE 710-01



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

REMOTE CONTROL RECEIVER

The MC6529 is a remote control receiver circuit for infrared applications. The following functions are available out of the 26 channel system:

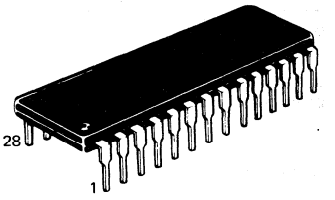
- 12 or 16 Programs
- 6 Analogue (3 controls ±)
- 1 Standby
- 2 General purpose
- 1 Sound killer
- 1 Strobe
- 1 Automatic sound mute
- 1 Decoded VR output
- 1 Automatic switch-on from Standby whenever a program is selected at the transmitter.
- 1 Pin option for 12 or 16 program operation.

ADDITIONAL FEATURES

- High input sensitivity (250 mVrms)
- Can be used for 8 programs only
- Internal UP/DOWN counter for front panel program sequencing
- Designed to be used in conjunction with the remote control transmitter MC14422P for 12 programs or MC14424P for 12 and 16 programs.

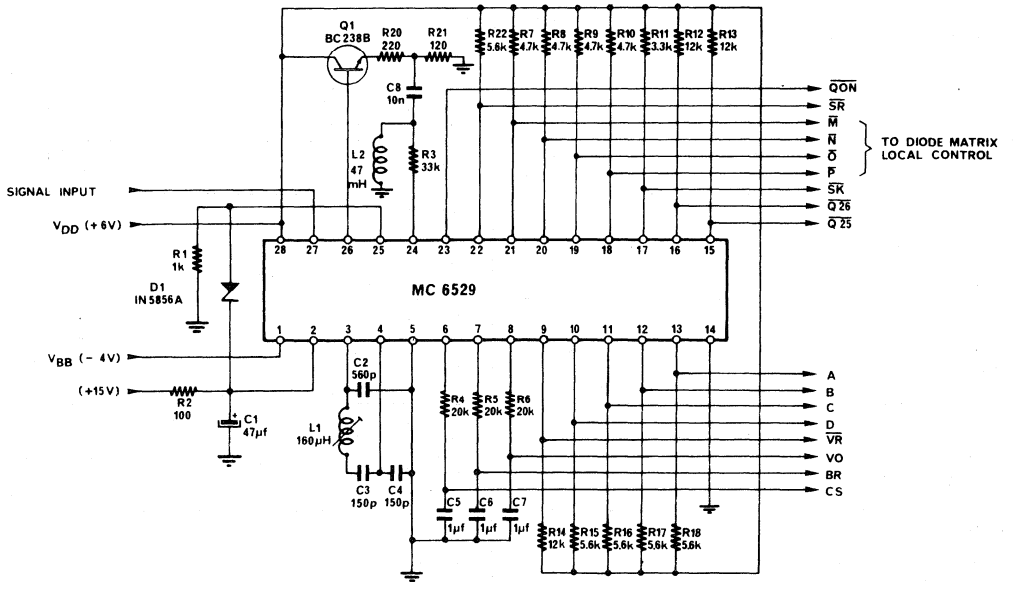
MOS
(N-CHANNEL, METAL–GATE)

REMOTE CONTROL RECEIVER



PLASTIC PACKAGE
CASE 710-01

FIGURE 1 – MC6529 TYPICAL CIRCUIT CONFIGURATION (16 PROGRAMS)



MAXIMUM RATINGS (T_A = 25 °C)

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltages	V_{BB} V_{DD} V_{GG}	−2 to −6 −.3 to 10 −.3 to 20	Vdc Vdc Vdc
Input Voltage, all Inputs	V_{in}	0 to 15	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, V_{GG} = 13 V ± 1 V unless otherwise specified, T_A = 0 to 70 °C)

CHARACTERISTIC	PIN	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
DC Supply voltage	1 28 2	V_{BB} V_{DD} V_{GG}		−3.6 5.4 11	−4 6 12	−4.4 6.6 14	V
DC Supply current	1 28 2	I_{BB} I_{DD} I_{GG}				−0.5 60 20	mA
Local control $\overline{MNOP}$ Input Voltage Current	18,19 20,21	V_{IL} V_{IH} I_{IH}	 Vin = 6.6 V	 4.0 		1.5 20	V µA
Band pass filter Input Voltage Current	24	V_{IL} V_{IH} I_{IH}	 Vin = 6.6 V	 V_{DD}−0.6 		1.5 V_{DD} 20	V µA
Reset Input Voltage Current	25	V_{IL} V_{IH} I_{IH} I_{IL}	 Vin = 6.6 V Vin = 0 V	 0.8 		0.2 20 −100	V µA
Signal Input Voltage Current	27	V_{SB} I_{IH} I_{IL}	 Vin = 6.6 V Vin = 0 V	250 		 100 −100	mVRMS µA
12/16 Program Input Option Voltage Current	14	V_{IL} V_{IH} I_{IH}	 Vin = 6.6 V	 4.0 		1.5 20	V µA
Oscillator Input Current	4	I_{IH} I_{IL}	Vin = 6.6 V Vin = 0 V	+.01 −.01		2 −2	mA
Binary Coded Output Current (open drain)	10,11 12,13	I_{OL} I_{OH}	V_{OL} = 0.5 V V_{OH} = 6.6 V	1 		 20	mA µA
Extra Output Current (open drain)	9,15	I_{OL} I_{OH}	V_{OL} = 0.5 V V_{OH} = 6.6 V	0.5 		 20	mA µA
Bistable Output Current (open drain)	16,17	I_{OL} I_{OH}	V_{OL} = 1.6 V V_{OH} = 6.6 V	1.6 		 10	mA µA
Strobe Output Current (open drain)	22	I_{OL} I_{OH}	V_{OL} = 0.4 V V_{OH} = 14 V	1.0 		 20	mA µA
Brightness & Colour Saturation Output Current (Push-Pull)	7,6	I_{OL} I_{OH}	V_{OL} = 0.5 V V = V_{DD} − 0.5 V	0.5 −0.5			mA
Volume Output Current (Push-Pull)	8	I_{OL} I_{OH}	V_{OL} = 1.6 V V = V_{DD} − 1.6 V	1.6 −1.6			mA
ON Output Current (Push-Pull)	23	I_{OL} I_{OH}	V_{OL} = 1.5 V V = V_{DD} − 1 V	100 −1.0			µA mA
Oscillator Output Current (Push-Pull)	3	I_{OL} I_{OH}	V_{OL} = 2.0 V V = V_{DD} − 1 V	0.5 −10			mA µA
Band Pass Filter Output (Push-Pull)	26	I_{OL} I_{OH}	V_{OL} = 0.5 V V = V_{DD} − 0.5 V	2.0 −2.0			mA

INPUT/OUTPUT FUNCTIONS

$\overline{QON}$ – This output distinguishes between the ON and STANDBY mode. When the front input ON via the matrix is low (Fig. 3 & 4) or when a program is selected via the transmitter following a previous standby instruction, output $\overline{QON}$ changes to low. When the front panel input STB changes to low or when the STANDBY instruction is given from the transmitter, $\overline{QON}$ changes to high.
When the reset voltage input V_{RE} rises from 0 volt to the threshold voltage V_{ASP} (+0.2 to +0.8 Volts) the output $\overline{QON}$ goes high. To insure that supply voltages have already reached their nominal value by this time a slight time delay is introduced by C1 and the 10 V zener D1 (refer to Fig. 1).

$\overline{MNOP}$ – Instructions performed from the front panel should be addressed via a matrix to these four inputs (see Fig. 3 & 4). Bounce protection is provided internally. Discrete pull up resistors are required on input $\overline{MNOP}$.
The program counter can be incremented or decremented in steps of 1 by applying a low on the appropriate inputs to the diode matrix PR + or PR – (see Fig. 4). The program counter has overflow & underflow capability. It is always preset to all low (program 1) if the receiver set is switched from mode OFF to ON. If the TV set is switched from STANDBY to ON, then the last operated program is selected and preset to middle position of BR, CS and V0 is performed.

$\overline{VR}$ – This output changes to low depending on the state of outputs A, B, C, D and as well input OPT (pin 14) as follows:
a) $\overline{VR} = \overline{ABCD}$ for OPT = high (12 program)
b) $\overline{VR} = \overline{ABCD}$ for OPT = low (16 program).

$\overline{SK}$ – When controlling $\overline{SK}$ from the remote control transmitter using channel 20 or via the diode matrix input $\overline{SK}$, the output $\overline{SK}$ will change alternatively to its complementary status on receipt of a command.
When the $\overline{SK}$ output is in the low mode, it is impossible to vary the volume control level V0.
If $\overline{SK}$ is in the low mode (sound killer operating) a channel change or an ON command will return it to a high.

$\overline{SR}$ – Strobe output. During all TV program changes a pulse will appear at the output $\overline{SR}$ (fig. 5). Therefore $\overline{SR}$ can be used to defete AFC during program selection via the transmitter, via inputs PR+, PR– and during switch on, or to control on screen display device as necessary.

OPT – Option Input. When OPT is high, the 12 program operation mode is selected. When OPT is low, the 16 program operation mode is selected.

$\overline{Q25}$ – General purpose output. By operation of remote channel 25 or by selecting the equivalent diode matrix input, the open drain output $\overline{Q25}$ changes to low impedance as long as the command is present.

$\overline{Q26}$ – General purpose output. If the remote control receiver is switched on from standby, output $\overline{Q26}$ will change from low to high. By operating the remote control channel 26 or by selecting the equivalent diode matrix input, $\overline{Q26}$ output will change to its complementary status. This can be used for the control of ancillary equipment. (e.g. VTR, information systems and so on.)

BR – VO – CS – Brightness, Volume, Colour Saturation analogue control voltage outputs.
These voltages are obtained by integrating the output signals through a low pass filter (R4 C5, R5 C6, R6 C7 in Fig. 1).
The analogue control voltage is then proportional to the duty cycle of the outputs, with a repetition frequency of 20.3 KHz.
The D/A converter resolution has been chosen to be 60 steps its value can be incremented or decremented in steps of 1. The analogue voltage can be varied up/down, at a speed of approximately 10 step/sec. The D/A conversion is performed with an underflow and overflow limiting circuit.
Output VO is automatically muted during channel switching when in standby mode, or when $\overline{SR}$ output is low (see timing table, fig. 5).
If the receiver is switched from the OFF mode to the ON mode or after a power interruption (reset V_{RE} rises from 0 volt to V_{ASP}) then BR & CS will be set to 50% of their value and VO to 35% (middle position).
Preset to middle position can also be performed via the diode matrix input MID or ON or via the remote control by connecting the Q25 output to the ON key of the diode matrix.

A-B-C-D – Binary coded program number minus one outputs. They are open drain outputs requiring external discrete pull up resistors. Refer to Fig. 2 for coded program number output.

FIGURE 2 – TABLE OF INSTRUCTIONS

FUNCTION	RECEIVED FREQUENCIES FROM REMOTE CONTROL						DIODE MATRIX				PROGRAM OUTPUT CODE			
	CHANNEL	f_a	f_b	f_c	f_d	f_e	M	N	O	P	A	B	C	D
Program + ON														
1	1	0	0	0	0	1					0	0	0	0
2	2	1	0	0	0	1					1	0	0	0
3	3	0	1	0	0	1					0	1	0	0
4	4	1	1	0	0	1					1	1	0	0
5	5	0	0	1	0	1					0	0	1	0
6	6	1	0	1	0	1					1	0	1	0
7	7	0	1	1	0	1					0	1	1	0
8	8	1	1	1	0	1					1	1	1	0
9	9	0	0	0	1	1					0	0	0	1
10	10	1	0	0	1	1					1	0	0	1
11	11	0	1	0	1	1					0	1	0	1
12	12	1	1	0	1	1					1	1	0	1
13	13	0	0	1	1	1					0	0	1	1
14	14	1	0	1	1	1					1	0	1	1
15	15	0	1	1	1	1					0	1	1	1
16	16	1	1	1	1	1					1	1	1	1
Colour saturation CS –	17	0	1	0	0	0	1	0	1	1				
Colour saturation CS +	18	1	1	0	0	0	0	0	1	1				
Volume VO –	19	0	0	1	0	0	1	1	0	1				
Volume VO +	20	1	0	1	0	0	0	1	0	1				
Brightness BR –	21	0	1	1	0	0	1	0	0	1				
Brightness BR +	22	1	1	1	0	0	0	0	0	1				
Standby STB	23	0	0	0	1	0	1	1	1	0				
Sound killer SK	24	1	0	0	1	0	0	1	1	0				
General Purpose Q25	25	0	1	0	1	0	1	0	1	0				
General Purpose Q26	26	1	1	0	1	0	0	0	1	0				
Program counter PR +							1	1	0	0				
Program counter PR –							0	1	0	0				
Middle position MID							1	0	0	0				
Power ON & MID							0	1	1	1				
TEST*							0	0	0	0				

* The code 0000 is used for device testing purposes only before shipment of MC6529 to customers.

ULTRASONIC INPUT FREQUENCIES

f_a = 34.688 KHz
f_b = 36.048 KHz
f_c = 37.519 KHz
f_d = 39.116 KHz
f_e = 42.755 KHz

FIGURE 3 – MC6529 BLOCK DIAGRAM

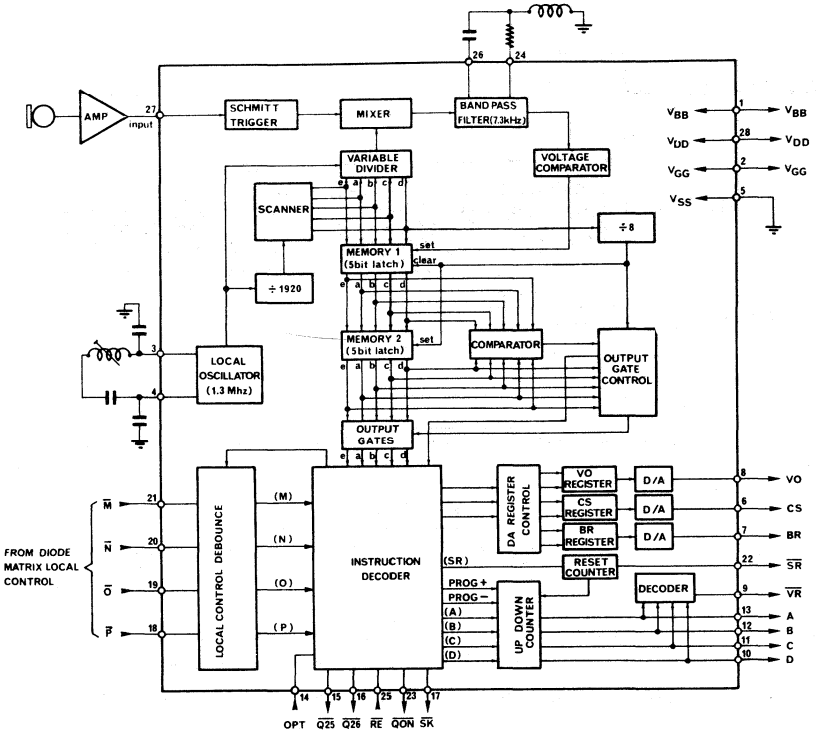
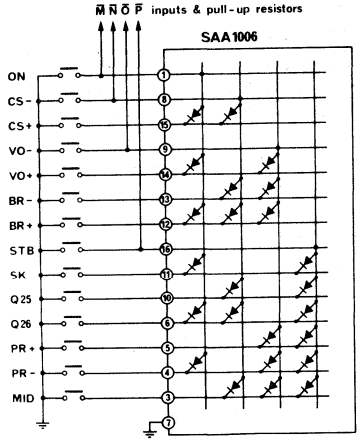


FIGURE 4 – DIODE MATRIX



This instruction encoding is performed by the Motorola IC: SAA1006.

FIGURE 5 – TIMING DIAGRAM FOR CONTROL VIA TRANSMITTER

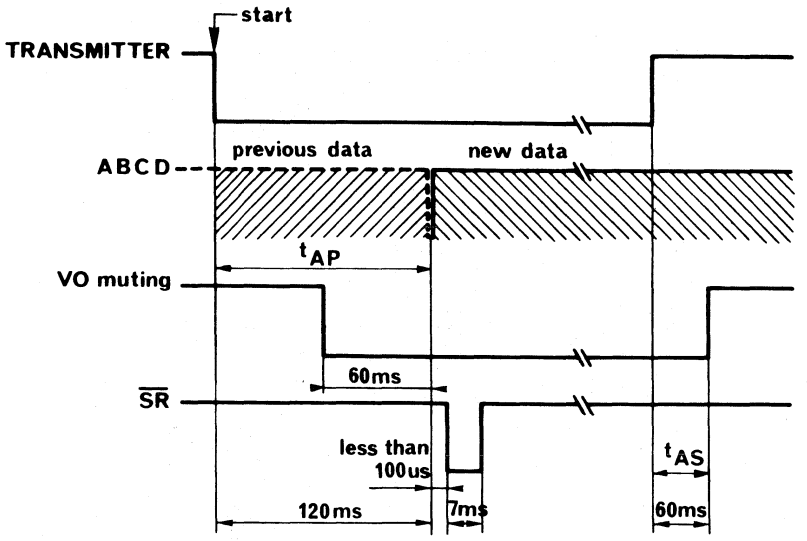
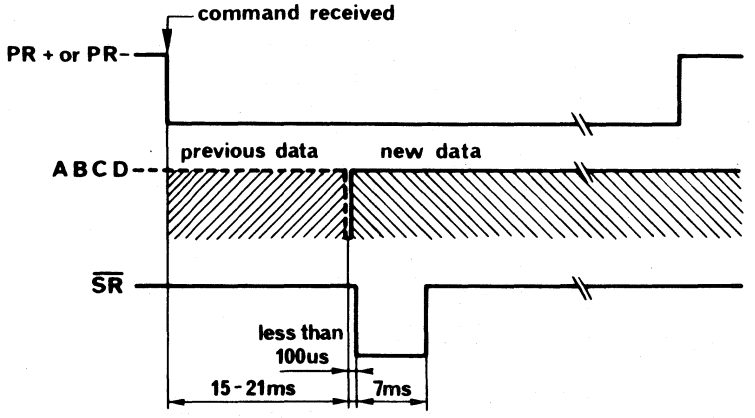
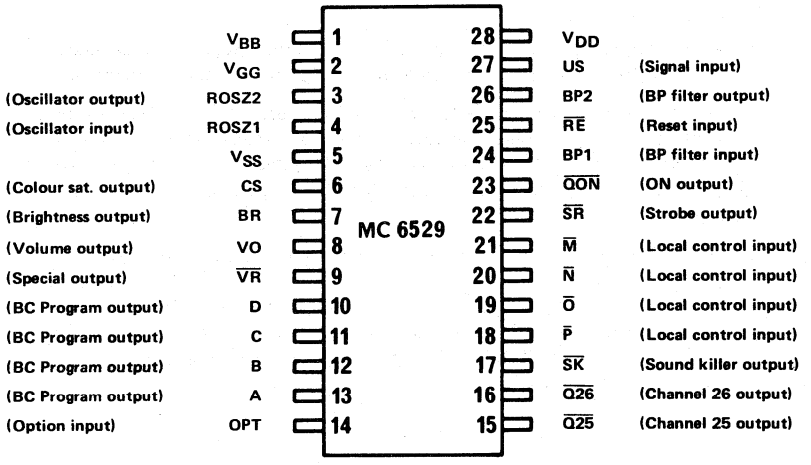


FIGURE 6 – TIMING DIAGRAM FOR CONTROL VIA DIODE MATRIX



Time required to switch "ON" or "STANDBY"	T_{AE} = 120 mS Typ.
Time required to change program	T_{AP} = 120 mS Typ.
Time required for other functions	T_{AA} = 120 mS Typ.
Delay time at the end of command	T_{AS} = 60 mS Typ.

FIGURE 7 – PIN ASSIGNMENT



EXTERNAL COMPONENT INFORMATION

L1: 160 μH, ad., Q $\geqslant$ 60, suggested supplier: TOKO-7BO-A2896HM
L2: 47 mH ± 5%, fixed, Q $\geqslant$ 100, suggested supplier: TOKO-181LY-473J
C2: 560 pF ± 10%
C3, C4: 150 pF ± 10%
C8: 10 nF ± 5%
All resistors: ± 5%

RECOMMENDED SETTING UP PROCEDURE

1. Reference oscillator and IF bandwidth

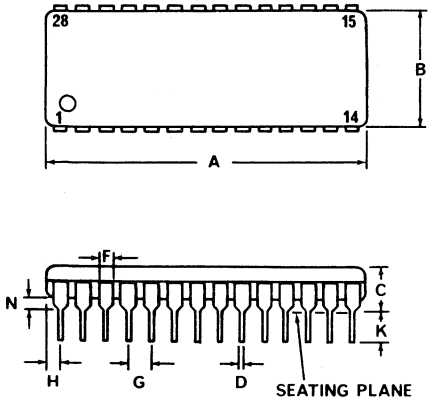
1.1. With reference to Fig. 1, connect pin 27 (Signal input) to a sine-wave oscillator set at 42755Hz (corresponding to f_e) and 5Vp/p of amplitude.

1.2. With an oscilloscope connected to pin 24 adjust L1 for maximum IF filter output. To insure the right frequency setting of the reference oscillator (approx: 1.3MHz) check the VO output pin 8 to go LOW (muted) and the $\overline{QON}$ output pin 23 to stay LOW while making this adjustment.

1.3. If desired it is now possible to check the receiver bandwidth by monitoring VO output.
Whenever channel 1 (f_e) is acquired the analogue voltage for the volume control will be muted (0 volt), therefore by varying f_e around the mean value of 42,755KHz it is possible to check the bandwidth of the receiver to be approximately ± 450Hz.

PACKAGE DIMENSIONS

PLASTIC PACKAGE
CASE 710-01



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE)

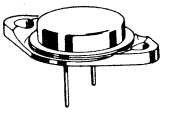
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

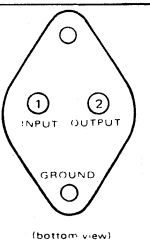
MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation – making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A-02 and Case 11 (TO-220AB and Hermetic TO-3)

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS





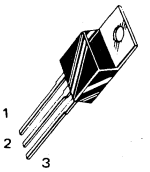
K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

(bottom view)

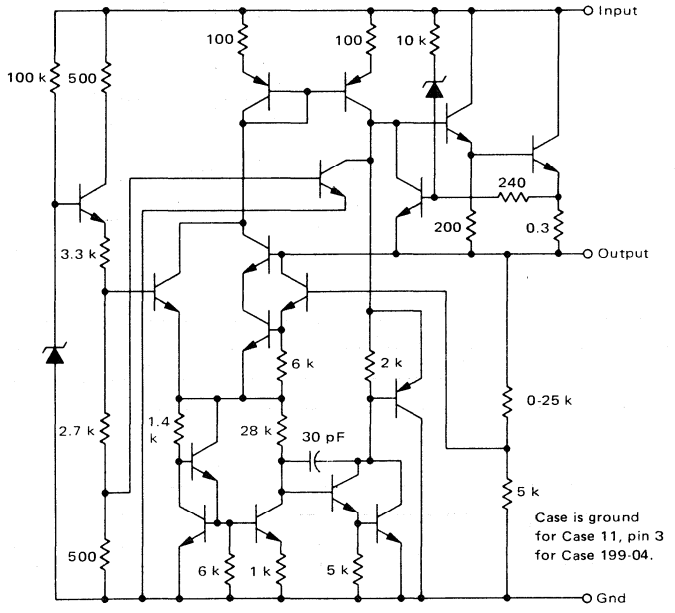
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
(TO-220AB)

Pin 1. Input
2. Ground
3. Output

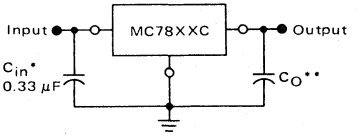


SCHEMATIC DIAGRAM



Case is ground for Case 11, pin 3 for Case 199-04.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC78XXCK	T_J = 0° C to +150° C	Metal Power
MC78XXCT	T_J = 0° C to +150° C	Plastic Power

MC7800C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +95°C (See Figure 1) Thermal Resistance, Junction to Case Metal Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +65°C (See Figure 2) Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC} P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 Internally Limited 15.4 65 Internally Limited 200 5.0 Internally Limited 22.5 45 Internally Limited 182 5.5	 Watts mW/°C °C/W Watts mW/°C °C/W Watts mW/°C °C/W Watts mW/°C °C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC7805C ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc (T_J = +25°C, I_O = 500 mA) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{in}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	4.75	–	5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	V_{in} V_O	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	750	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	 –	 -1.0	 –	mV/°C

MC7806C ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	9.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	43	120	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage	V_O				Vdc
(8.0 Vdc ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		5.7	–	6.3	
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential	V_{in} V_O				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	35	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	550	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$		–	–1.0	–	

MC7808C ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	12	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	50	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage	V_O				Vdc
(10.5 Vdc ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		7.6	–	8.4	
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential	V_{in}-V_O				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	40	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	450	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$		–	–1.0	–	

MC7812C ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
14.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	13	120	
16 Vdc ≤ V_{in} ≤ 22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
14.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	55	240	
16 Vdc ≤ V_{in} ≤ 22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage	V_O				Vdc
(14.5 Vdc ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		11.4	–	12.6	
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
14.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	350	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
(I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$)		–	-1.0	–	

MC7815C ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	14	150	
20 Vdc ≤ V_{in} ≤ 26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	57	300	
20 Vdc ≤ V_{in} ≤ 26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage	V_O				Vdc
(17.5 Vdc ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		14.25	–	15.75	
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change	ΔI_B				mA
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	230	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$		–	-1.0	–	

MC7818C ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	25	180	
24 Vdc ≤ V_{in} ≤ 30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	90	360	
24 Vdc ≤ V_{in} ≤ 30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage	V_O				Vdc
(21 Vdc ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		17.1	–	18.9	
Quiescent Current (T_J = +25°C)	I_B	–	4.5	8.0	mA
Quiescent Current Change	ΔI_B				mA
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	110	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	200	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$		–	-1.0	–	

MC7824C ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	31	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	118	480	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage	V_O				Vdc
(27 Vdc ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		22.8	–	25.2	
Quiescent Current (T_J = +25°C)	I_B	–	4.6	8.0	mA
Quiescent Current Change	ΔI_B				mA
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$	–	2.0	–	Vdc
(I_O = 1.0 A, T_J = +25°C)					
Output Resistance (I_O = 500 mA)	R_O	–	150	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	150	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, $0^oC \le T_A \le +125^oC$		–	-1.0	–	

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 313)

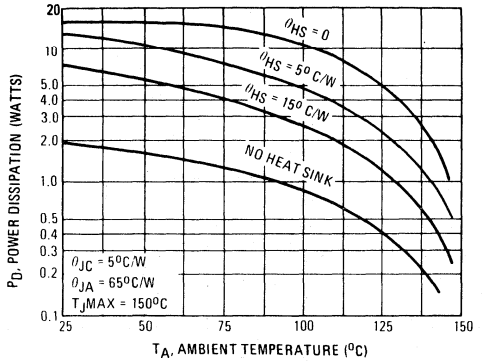


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 11)

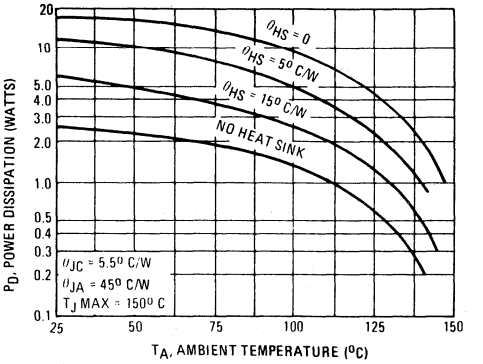


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE

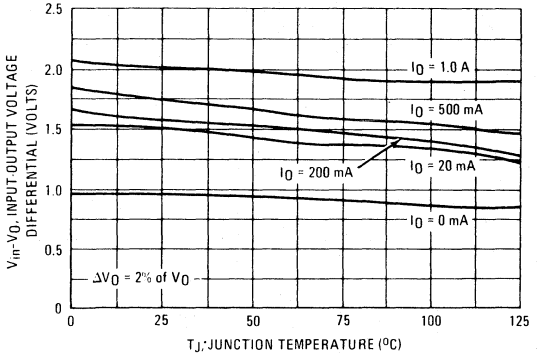


FIGURE 4 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

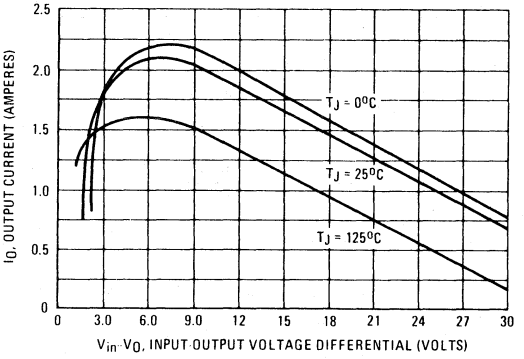


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

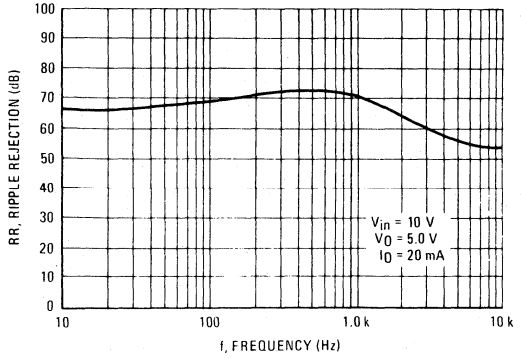
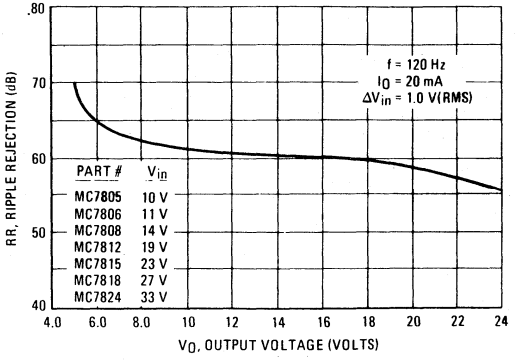


FIGURE 6 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

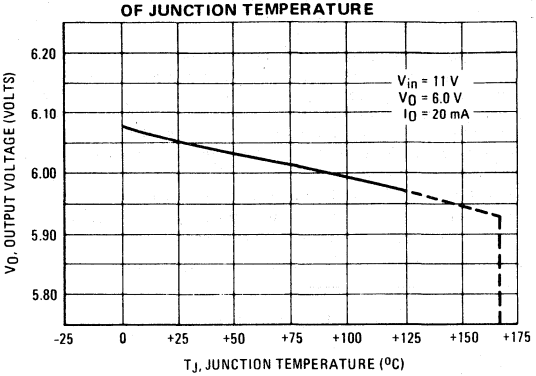


FIGURE 8 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

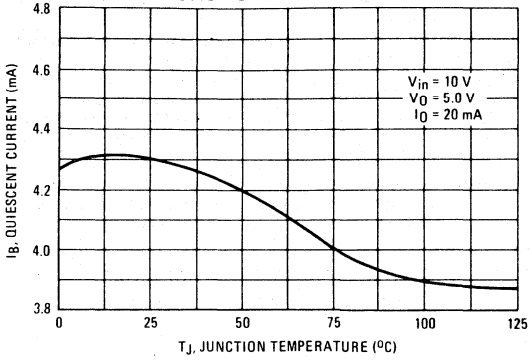
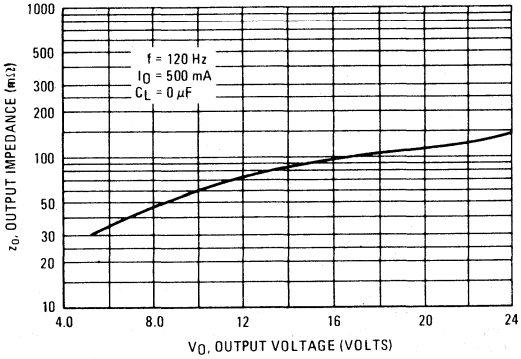


FIGURE 9 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

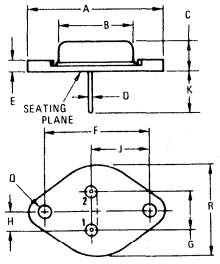
Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

OUTLINE DIMENSIONS

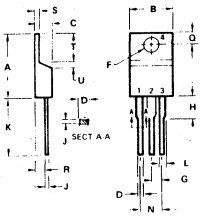
$R_{\theta JA}$ = 45°C/W (Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Weight ≈ 5.9 grams
Pins 1 and 2 electrically isolated from case
Case is third electrical connection.
Leads are gold-plated copper-cored Kovar*
*Trademark of Westinghouse Electric Corporation
Ground connected to case.
Metal Package
CASE 11-01
K SUFFIX

$R_{\theta JA}$ = 65° C/W (Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

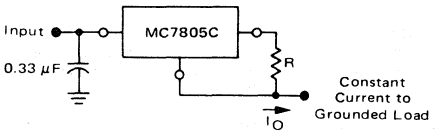
APPLICATIONS INFORMATION

Design Considerations

The MC7800C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 10 – CURRENT REGULATOR



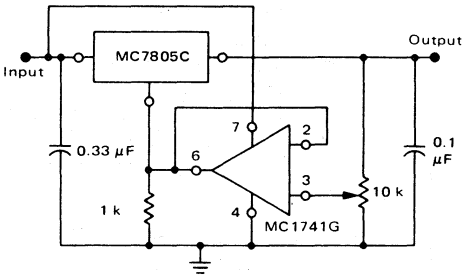
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

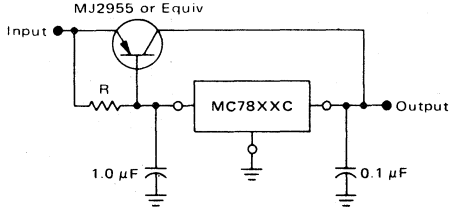
FIGURE 11 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

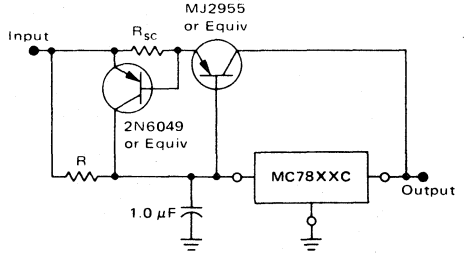
FIGURE 12 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 13 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 12 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc} and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08C			MC78L08AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
10.5 Vdc ≤ V_I ≤ 23 Vdc		–	20	200	–	20	175	
11 Vdc ≤ V_I ≤ 23 Vdc		–	12	150	–	12	125	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	80	–	15	80	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	6.0	40	–	8.0	40	
Output Voltage	V_O							Vdc
(10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		7.2	–	8.8	7.6	–	8.4	
(V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)		7.2	–	8.8	7.6	–	8.4	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	–	60	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	20	–	–	20	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	36	55	–	37	57	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L12C			MC78L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.1	12	12.9	11.5	12	12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		10.8	–	13.2	11.4	–	12.6	
(V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)		10.8	–	13.2	11.4	–	12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.2	6.5	–	4.2	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L15C			MC78L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	13.8	15	16.2	14.4	15	15.6	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	130	300	–	130	300	
20 Vdc ≤ V_I ≤ 30 Vdc		–	110	250	–	110	250	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	25	150	–	25	150	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	12	75	–	12	75	
Output Voltage	V_O							Vdc
(17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		13.5	–	16.5	14.25	–	15.75	
(V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)		13.5	–	16.5	14.25	–	15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.4	6.5	–	4.4	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(20 Vdc ≤ V_I ≤ 30 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L18C			MC78L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	16.6	18	19.4	17.3	18	18.7	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
21.4 Vdc ≤ V_I ≤ 33 Vdc		–	32	325				
20.7 Vdc ≤ V_I ≤ 33 Vdc					–	45	325	
22 Vdc ≤ V_I ≤ 33 Vdc		–	27	275				
21 Vdc ≤ V_I ≤ 33 Vdc					–	35	275	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	30	170	–	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	15	85	–	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		16.2	–	17.8				
(20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					17.1	–	18.9	
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)		16.2	–	17.8				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					17.1	–	18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)		–	–	1.5				
(21 Vdc ≤ V_I = 33 Vdc)					–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	35	350	–	–	–	
28 Vdc ≤ V_I ≤ 38 Vdc		–	30	300	–	50	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	60	350	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					22.8	–	25.2	
(28 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)					22.8	–	25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	30	43	–	31	45	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

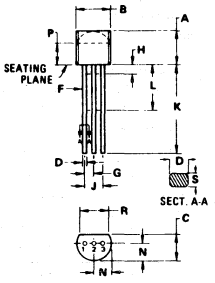
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

OUTLINE DIMENSIONS

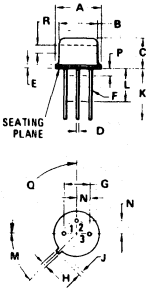


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

P SUFFIX
CASE 29
TO-92

$R_{\theta JA}$ = 200°C/W



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

G SUFFIX
CASE 79
TO-39

$R_{\theta JA}$ = 150°C/W
$R_{\theta JC}$ = 40°C/W

MC78L00C, AC Series

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

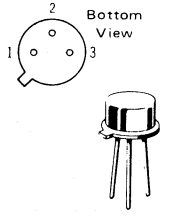
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

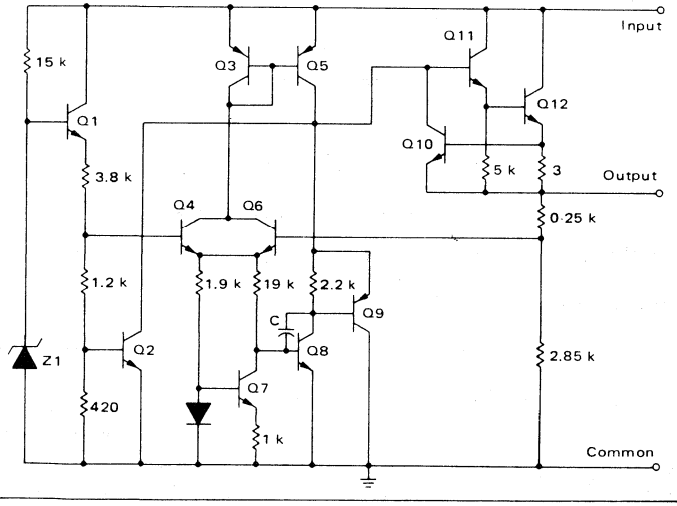
PIN 1. INPUT
2. OUTPUT
3. GROUND



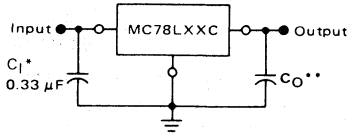
G SUFFIX
CASE 79
TO-39

Pin 1. Input
2. Output
3. Ground

REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

Device No. ·10%	Device No. ·5%	Nominal Voltage
–	MC78L02AC	2.6
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

ORDERING INFORMATION		
Device	Temperature Range	Package
MC78LXXACG	T_J = 0°C to +150°C	Metal Can
MC78LXXACP	T_J = 0°C to +150°C	Plastic Transistor
MC78LXXCG	T_J = 0°C to +150°C	Metal Can
MC78LXXCP	T_J = 0°C to +150°C	Plastic Transistor
XX indicates nominal voltage		

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V) (12 V – 18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L02AC ELECTRICAL CHARACTERISTICS (V_I = 9.0 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C ≤ T_J ≤ +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L02AC Min	MC78L02AC Typ	MC78L02AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	2.5	2.6	2.7	Vdc
Input Regulation (T_J = +25°C) 4.75 Vdc ≤ V_I ≤ 20 Vdc 5.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 40 30	 100 75	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 10 4.0	 50 25	mV
Output Voltage (4.75 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (4.75 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 2.45 2.45	 – –	 2.75 2.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_B	 – –	 3.6 –	 6.0 5.5	mA
Input Bias Current Change (5.0 Vdc ≤ V_{in} ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_B	 – –	 – –	 2.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	30	–	μV
Ripple Rejection (f = 120 Hz, 6.0 V ≤ V_{in} ≤ 16 V, T_J = 25°C)	RR	43	51	–	dB
Input-Output Voltage Differential (T_J = 25°C)	V_I/V_O	–	1.7	–	Vdc

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C ≤ T_J ≤ +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05C Min	MC78L05C Typ	MC78L05C Max	MC78L05AC Min	MC78L05AC Typ	MC78L05AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 200 150	 – –	 55 45	 150 100	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	 – –	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.5 4.5	 – –	 5.5 5.5	 4.75 4.75	 – –	 5.25 5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	 – –	 3.8 –	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

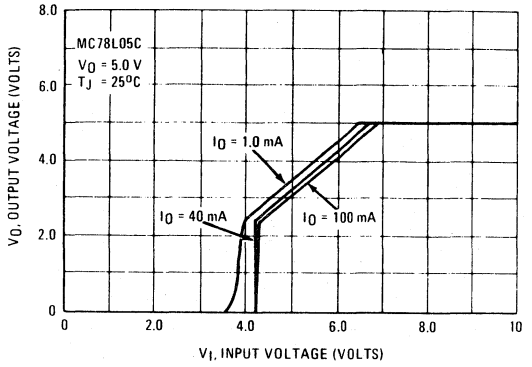


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

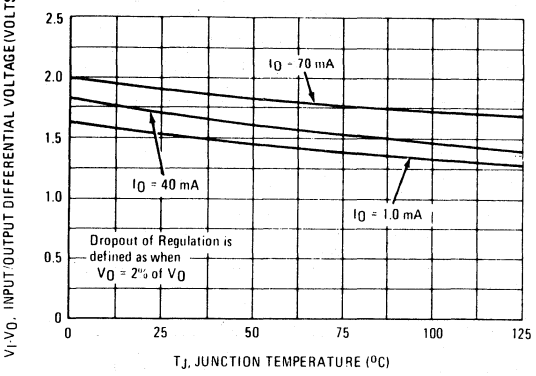


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

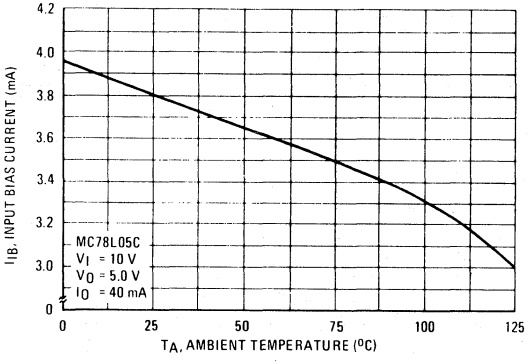


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

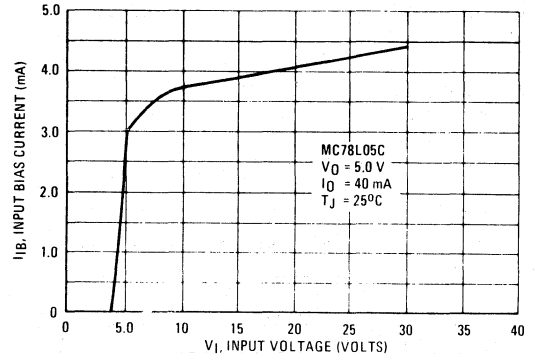


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

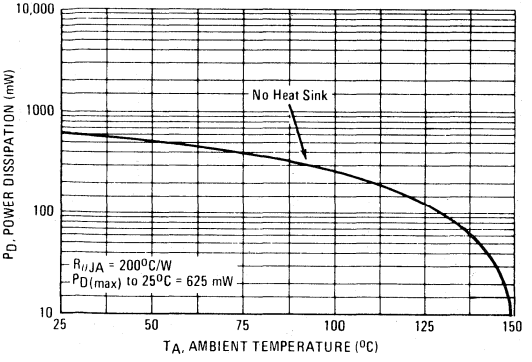
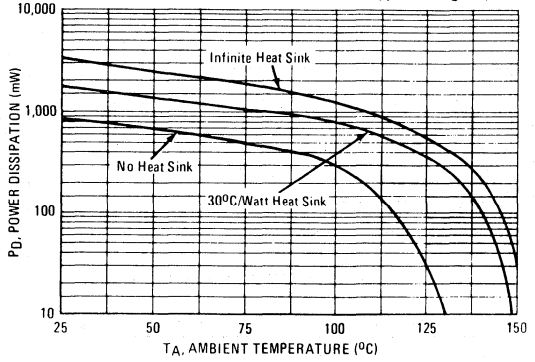


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



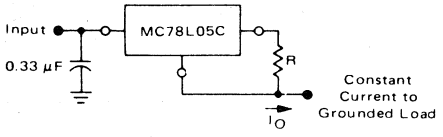
APPLICATIONS INFORMATION

Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

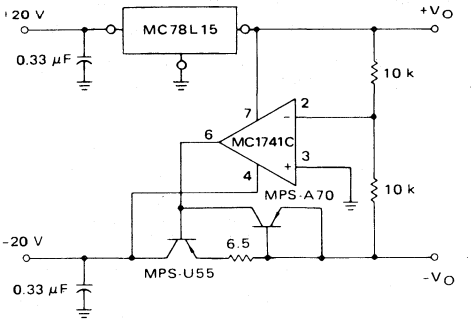
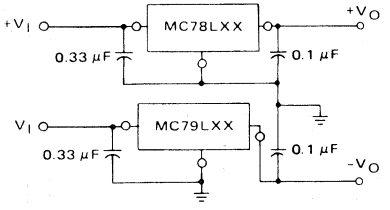


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



MC78M00C Series

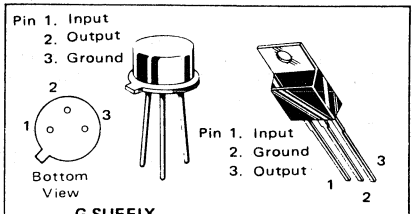
MC78M00C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only half the output current. Like the MC7800C devices, the MC78M00C three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A-02 and Case 79 (TO-220AB and Hermetic TO-39)

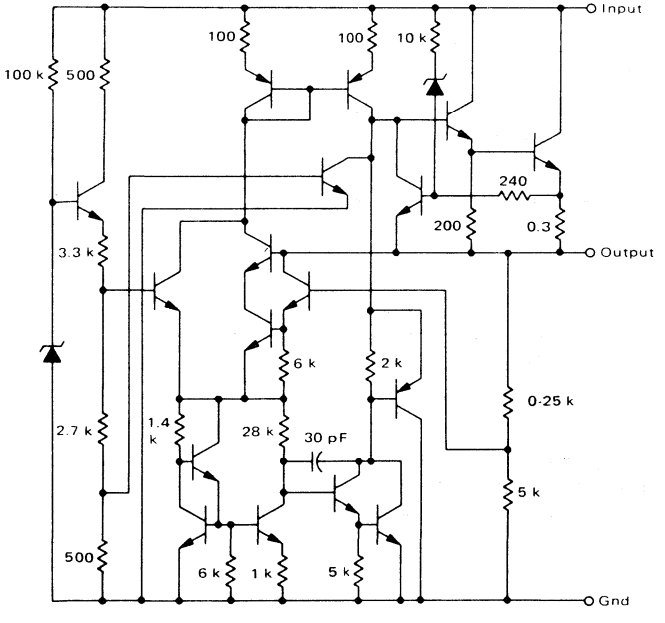
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



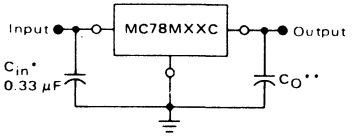
G SUFFIX
METAL PACKAGE
CASE 79
TO-39
(Case connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
(TO-220AB)

REPRESENTATIVE SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC78MXXCG	T_J = 0° C to +150° C	Metal Can
MC78MXXCT	T_J = 0° C to +150° C	Plastic Power
XX indicates nominal voltage		

TYPE NO./VOLTAGE

MC78M05C	5.0 Volts
MC78M06C	6.0 Volts
MC78M08C	8.0 Volts
MC78M12C	12 Volts
MC78M15C	15 Volts
MC78M18C	18 Volts
MC78M20C	20 Volts
MC78M24C	24 Volts

MC78M00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation)			
Plastic Package			
T_A = 25°C	P_D	Internally Limited	
Derate above T_A = 25°C	θ_{JA}	70	°C/W
T_C = 25°C	P_D	Internally Limited	
Derate above T_C = 110°C	θ_{JC}	5.0	°C/W
Metal Package			
T_A = 25°C	P_D	Internally Limited	
Derate above T_A = 25°C	θ_{JA}	185	°C/W
T_C = 25°C	P_D	Internally Limited	
Derate above T_C = 85°C	θ_{JC}	25	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}		
Plastic Package		-65 to +150	°C
Metal Package		-65 to +150	°C

MC78M05C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C)					
(7.0 Vdc $\leq V_I \leq$ 25 Vdc)		–	3.0	100	
(8.0 Vdc $\leq V_I \leq$ 25 Vdc)		–	1.0	50	
Load Regulation	Reg_{load}				mV
(T_J = +25°C, 5.0 mA $\leq I_O \leq$ 500 mA)		–	20	100	
(T_J = +25°C, 5.0 mA $\leq I_O \leq$ 200 mA)		–	10	50	
Output Voltage (7.0 Vdc $\leq V_I \leq$ 25 Vdc, 5.0 mA $\leq I_O \leq$ 200 mA)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(8.0 Vdc $\leq V_I \leq$ 25 Vdc)		–	–	0.8	
(5.0 mA $\leq I_O \leq$ 200 mA)		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leq f \leq$ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 8.0 V $\leq V_I \leq$ 18 V)	RR	–	80	–	dB
(I_O = 300 mA, f = 120 Hz, 8.0 $\leq V_I \leq$ 18 V, T_J = 25°C)		–	80	–	
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	300	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M06C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C) (8.0 Vdc ≤ V_I ≤ 25 Vdc) (9.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 5.0 1.5	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	5.7	–	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	270	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-0.5	–	mV/°C
Peak Output Current (T_J = 25°C) (T_J = 25°C)	I_O	–	700	–	mA

MC78M08C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C) (10.5 Vdc ≤ V_I ≤ 25 Vdc) (11 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 6.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	7.6	–	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	250	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M12C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 200 mA, $0^oC < T_J < +125^oC$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C) (14.5 Vdc ≤ V_I ≤ 30 Vdc) (16 Vdc ≤ V_I ≤ 22 Vdc)	Reg_{line}	 – –	 8.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M15C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 200 mA, $0^oC < T_J < +125^oC$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C) (17.5 Vdc ≤ V_I ≤ 30 Vdc) (20 Vdc ≤ V_I ≤ 30 Vdc)	Reg_{line}	 – –	 10 3.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 150 75	mV
Output Voltage 17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (18.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M18C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C) (21 Vdc ≤ V_I ≤ 33 Vdc) (24 Vdc ≤ V_I ≤ 33 Vdc)	Reg_{line}	 – –	 10 40	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	17.1	–	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	100	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M20C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 200 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C) (23 Vdc ≤ V_I ≤ 35 Vdc) (24 Vdc ≤ V_I ≤ 35 Vdc)	Reg_{line}	 – –	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	19	–	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.9	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	80	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.1	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M24C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C) (27 Vdc ≤ V_I ≤ 38 Vdc) (28 Vdc ≤ V_I ≤ 38 Vdc)	Reg_{line}	 – –	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	22.8	–	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	5.0	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V < V_I < 38 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$(Typ) = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

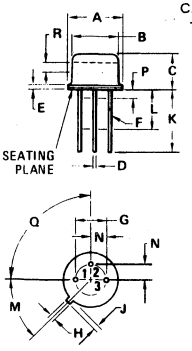
Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

OUTLINE DIMENSIONS

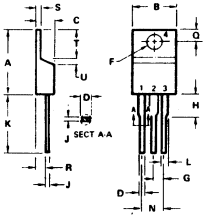
G SUFFIX
METAL PACKAGE
CASE 79
TO-39



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
(TO-220AB)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

TYPICAL PERFORMANCE CURVES

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220AB (CASE 221A-02)

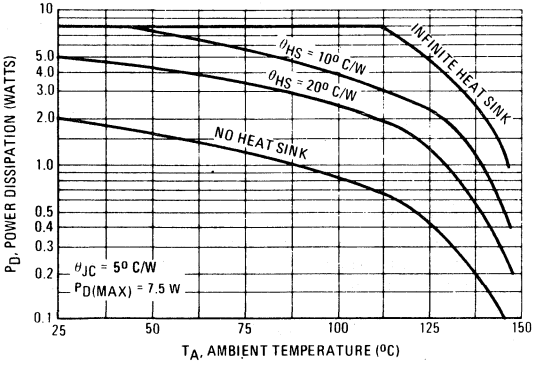


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-39 (CASE 79)

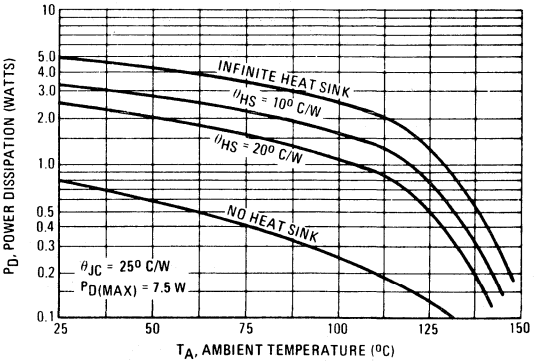


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

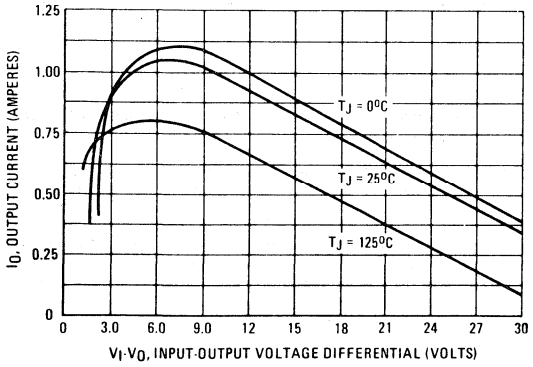
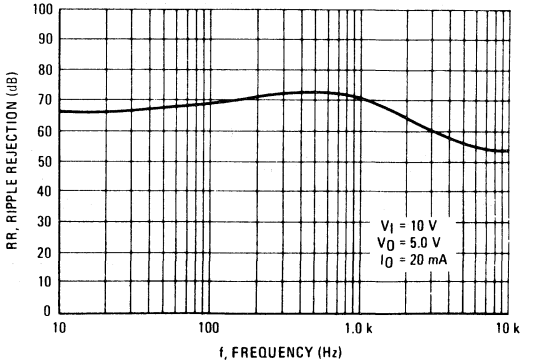


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



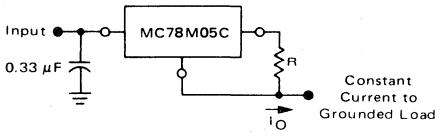
APPLICATIONS INFORMATION

Design Considerations

The MC78M00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 – CURRENT REGULATOR



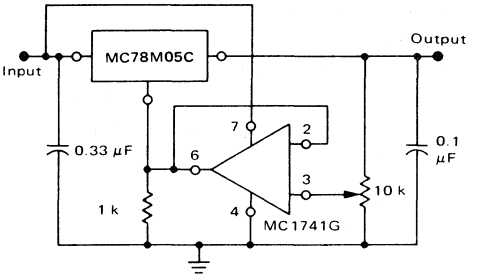
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

I_Q = 1.5 mA over line and load changes

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

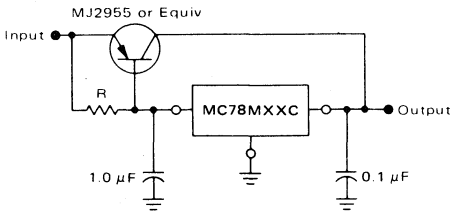
FIGURE 6 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geqslant 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

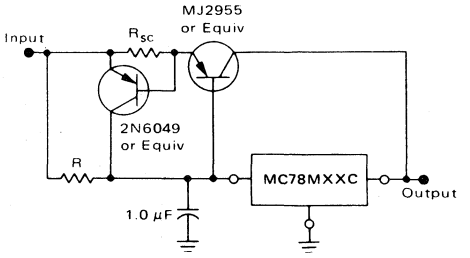
FIGURE 7 – CURRENT BOOST REGULATOR



XX – 2 digits of type number indicating voltage.

The MC78M00C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 8 – SHORT-CIRCUIT PROTECTION



XX – 2 digits of type number indicating voltage

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

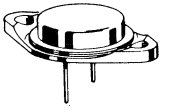
MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

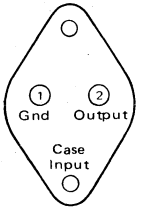
Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A-02 and Case 11 (TO-220AB and Hermetic TO-3)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

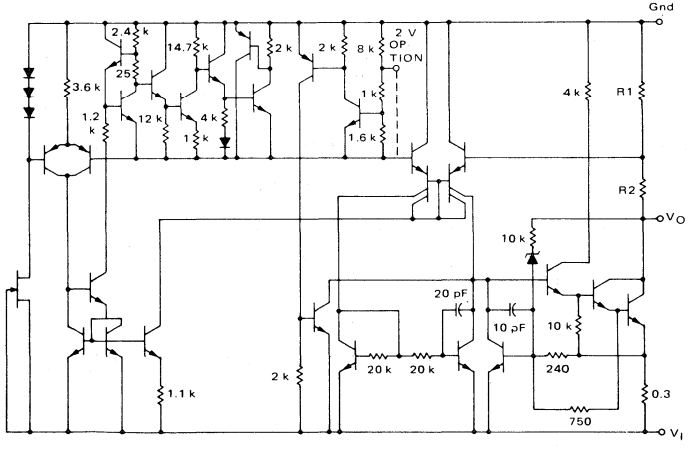


(bottom view)

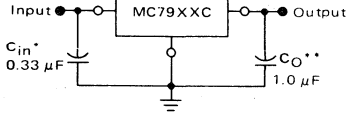
T SUFFIX
PLASTIC PACKAGE
CASE 221A-02

Pin 1. Ground
2. Input
3. Output

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C – 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	T_J = 0° C to +150° C	Metal Power
MD79XXCT	T_J = 0° C to +150° C	Plastic Power
XX indicates nominal voltage		

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MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_I	−35 −40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C (See Figure 1) Metal Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +65°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	 Internally Limited 15.4 Internally Limited 200 Internally Limited 22.2 Internally Limited 182	 Watts mW/°C Watts mW/°C Watts mW/°C Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient – Plastic Package – Metal Package	$R_{\theta JA}$	65 45	°C/W
Thermal Resistance, Junction to Case – Plastic Package – Metal Package	$R_{\theta JC}$	5.0 5.5	°C/W

MC7902C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 – – – –	 8.0 4.0 18 8.0	 20 10 40 20	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 70 20	 120 60	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-1.90	–	-2.10	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	7.0	50	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	35	100	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage	V_O	-4.75	–	-5.25	Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	8.0	52	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	37	105	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	8.5	52	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	12	105	
250 mA ≤ I_O ≤ 750 mA		–	4.5	52	
Output Voltage	V_O	-4.94	–	-5.46	Vdc
-7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	42	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	9.0	60	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	43	120	
-9.0 Vdc ≥ V_I ≥ -13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage	V_O	-5.7	–	-6.3	Vdc
-8.0 Vdc ≥ V_I ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-8.0 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	12	80	
-11 Vdc ≥ V_I ≥ -17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	50	160	
-11 Vdc ≥ V_I ≥ -17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage	V_O	-7.6	–	-8.4	Vdc
-10.5 Vdc ≥ V_I ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-10.5 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	13	120	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	55	240	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage	V_O	-11.4	–	-12.6	Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	14	150	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	57	300	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage	V_O	-14.25	–	-15.75	Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	25	180	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	90	360	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage	V_O	-17.1	–	-18.9	Vdc
-21 Vdc ≥ V_I ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	31	240	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	118	480	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage	V_O	-22.8	–	-25.2	Vdc
-27 Vdc ≥ V_I ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

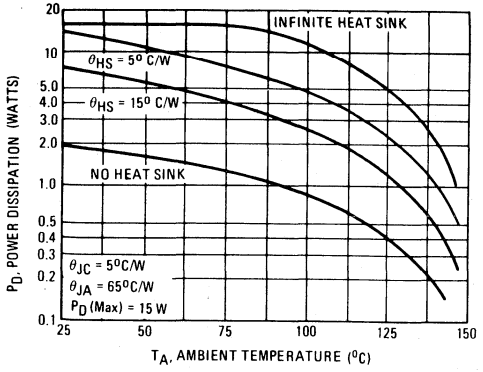


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

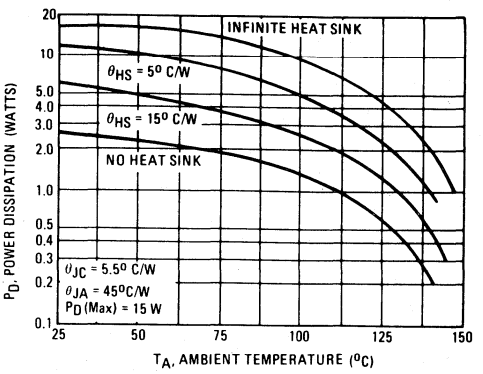


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

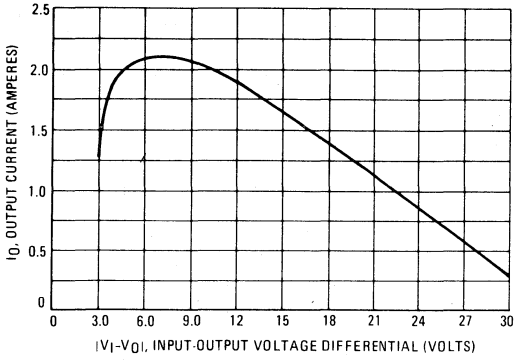


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

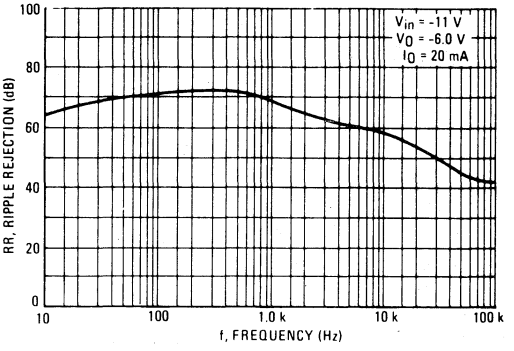


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

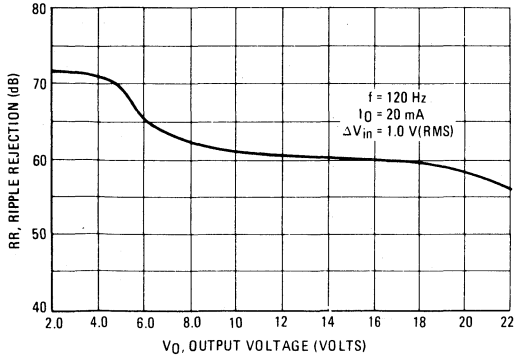
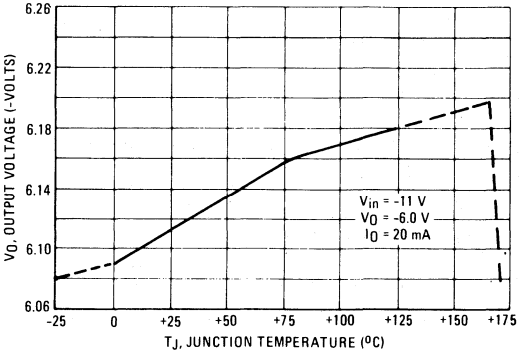
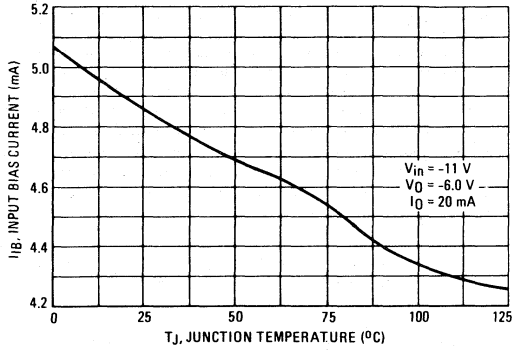


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

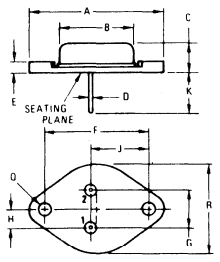
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

OUTLINE DIMENSIONS



LEAD CONFIGURATION
PIN 1. GND
2. OUTPUT
CASE: INPUT

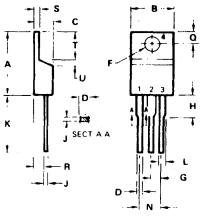
NOTE
1. DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A		39.37		1.550
B		21.08		0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		3.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R		26.67		1.050

Weight – 5.9 grams

$R_{\theta JA}$ = 45°C/W (Typ)

Leads are gold plated copper cored Kovar*
*Trademark of Westinghouse Electric Corporation
Ground connected to case
Metal Package
CASE 11-01
K SUFFIX



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

$R_{\theta JA}$ = 65°C/W (Typ)

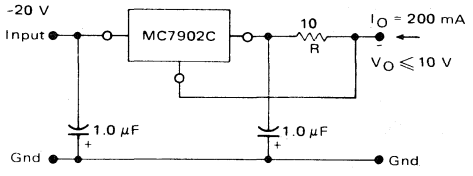
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

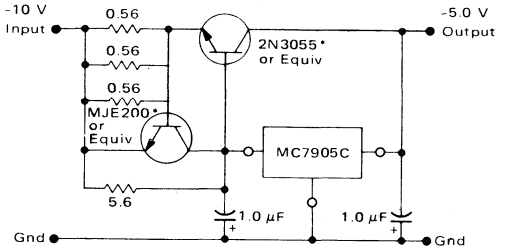


The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

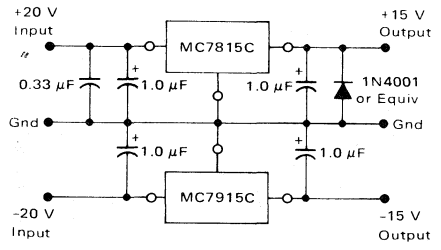
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS 10 or equivalent.

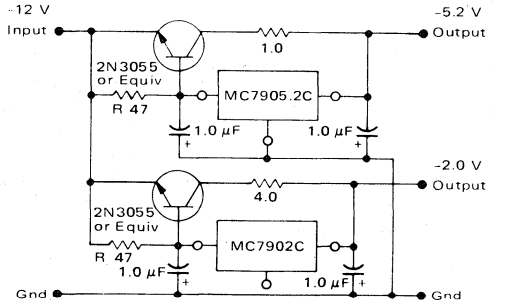
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

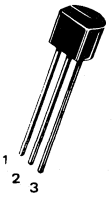
The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

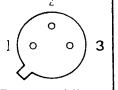
P SUFFIX
CASE 29
TO-92



Pin 1. Ground
2. Input
3. Output

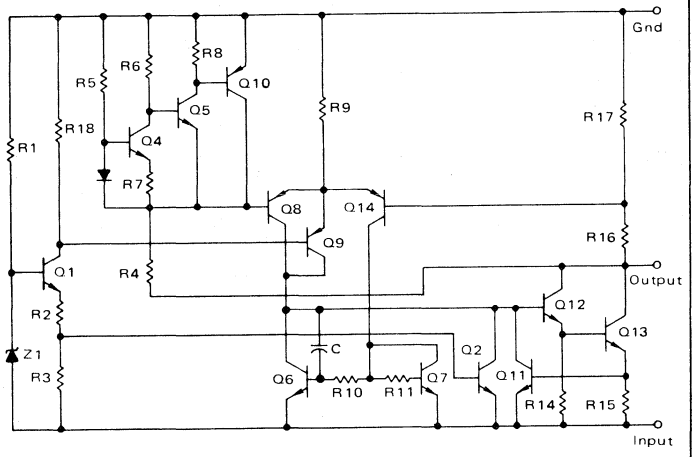
G SUFFIX
CASE 79
TO-39

Pin 1. Ground
2. Output
3. Input

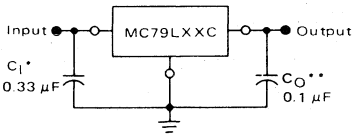


Bottom View

REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L03C	MC79L03AC	−3.0
MC79L05C	MC79L05AC	−5.0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

ORDERING INFORMATION		
Device	Temperature Range	Package
MC79LXXACG	T_J = 0°C to +150°C	Metal Can
MC79LXXACP	T_J = 0°C to +150°C	Plastic Power
MC79LXXCG	T_J = 0°C to +150°C	Metal Can
MC79LXXCP	T_J = 0°C to +150°C	Plastic Power
XX indicates nominal voltage		

MC79L00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Input Voltage	(-3,-5 V)	V_I	-30	Vdc
	(-12,-15,-18 V)		-35	
	(-24 V)		-40	
Storage Temperature Range		T_{stg}	-65 to +150	°C
Junction Temperature Range		T_J	0 to +150	°C

MC79L03C, AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L03C			MC79L03AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-2.76	-3.00	-3.24	-2.88	-3.0	-3.12	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-7.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	80	–	–	60	
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	60	–	–	40	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	72	–	–	72	
1.0 mA ≤ I_O ≤ 40 mA		–	–	36	–	–	36	
Output Voltage	V_O							Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-2.7	–	-3.3	-2.85	–	-3.15	
V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-2.7	–	-3.3	-2.85	–	-3.15	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	-1.5	–	–	-1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	-0.2	–	–	-0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	30	–	–	30	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	10	–	–	10	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ -18 Vdc, f = 120 Hz, T_J = 25°C)	RR	44	51	–	45	51	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-7.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	200	–	–	150	
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	150	–	–	100	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	60	–	–	60	
1.0 mA ≤ I_O ≤ 40 mA		–	–	30	–	–	30	
Output Voltage	V_O							Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-4.5	–	-5.5	-4.75	–	-5.25	
V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-4.5	–	-5.5	-4.75	–	-5.25	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 kHz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-14.5 Vdc ≥ V_I ≥ -27 Vdc		–	–	250	–	–	250	
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	200	–	–	200	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	100	–	–	100	
1.0 mA ≤ I_O ≤ 40 mA		–	–	50	–	–	50	
Output Voltage	V_O							Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-10.8	–	-13.2	-11.4	–	-12.6	
V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-10.8	–	-13.2	-11.4	–	-12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	300	–	–	300	
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	250	–	–	250	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	150	–	–	150	
1.0 mA ≤ I_O ≤ 40 mA		–	–	75	–	–	75	
Output Voltage	V_O							Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-13.5	–	-16.5	-14.25	–	-15.75	
V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-13.5	–	-16.5	-14.25	–	-15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	–	1.7	–	–	1.7	–	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-20.7 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	325	
-21.4 Vdc ≥ V_I ≥ -33 Vdc		–	–	325	–	–	–	
-22 Vdc ≥ V_I ≥ -33 Vdc		–	–	275	–	–	–	
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	275	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	170	–	–	170	
1.0 mA ≤ I_O ≤ 40 mA		–	–	85	–	–	85	
Output Voltage	V_O							Vdc
-20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-17.1	–	-18.9	
-21.4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-16.2	–	-19.8	–	–	–	
V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-16.2	–	-19.8	-17.1	–	-18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	1.5	
-27 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.5	–	–	–	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	–	1.7	–	–	1.7	–	Vdc

MC79L24C, AC ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-27 Vdc ≥ V_I ≥ -38 V		–	–	–	–	–	350	
-27.5 Vdc ≥ V_I ≥ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ≥ V_I ≥ -38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-22.8	–	-25.2	
-28 Vdc ≥ V_I ≥ -38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-21.4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (-29 ≤ V_I ≤ -35 Vdc, f = 120 Hz, T_J = 25°C)	RR	30	43	–	31	47	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

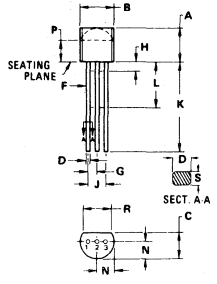
T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

OUTLINE DIMENSIONS

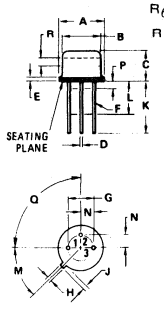
PLASTIC PACKAGE
CASE 29
TO-92
$R_{\theta JA}$ = 200°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply

METAL PACKAGE
CASE 79
TO-39
$R_{\theta JA}$ = 150°C/W
$R_{\theta JC}$ = 40°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

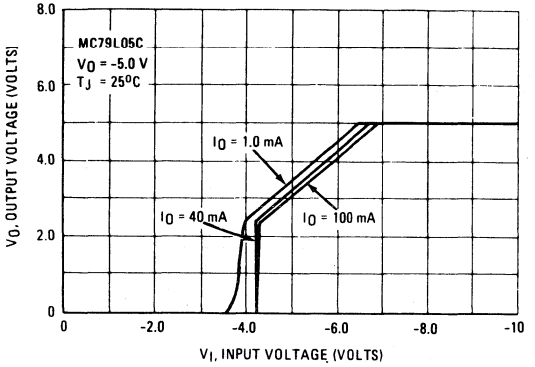


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

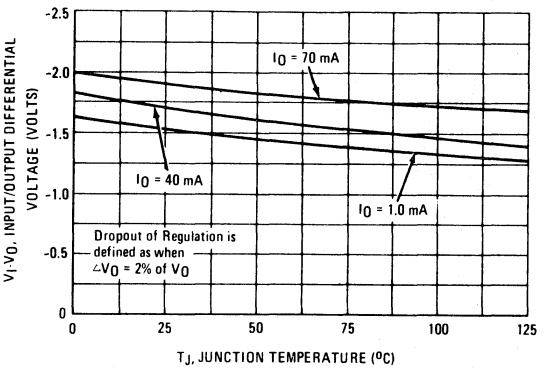


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

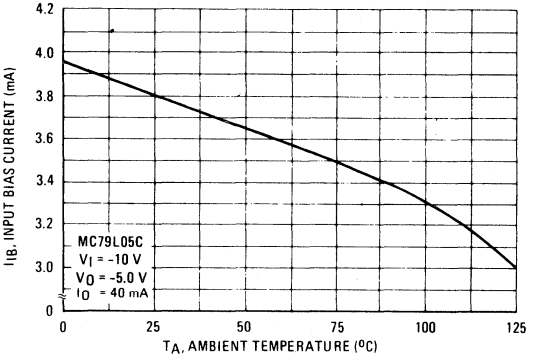


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

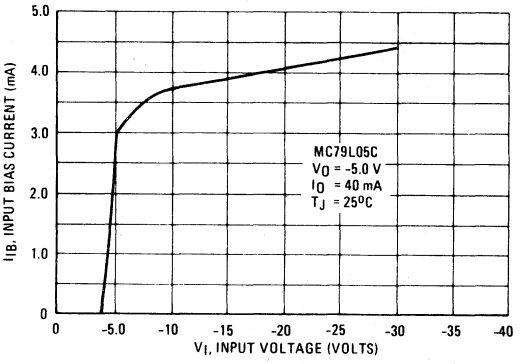


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

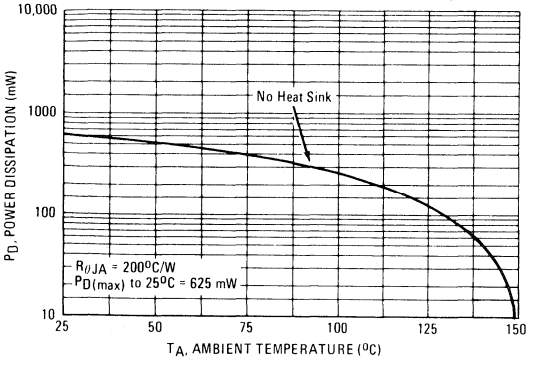
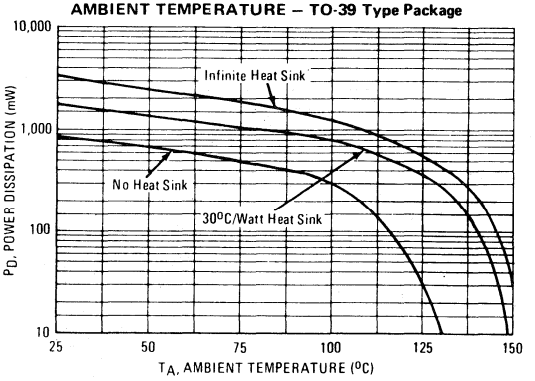


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



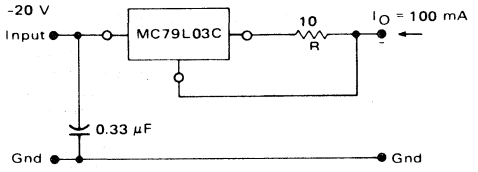
APPLICATIONS INFORMATION

Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR

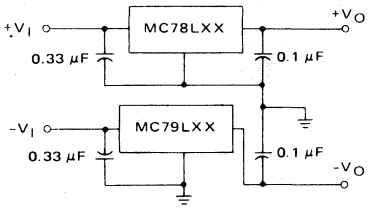


The MC79L03, -3.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{3\ V}{R} + I_B$$

The quiescent current for this regulator is typically 3.8 mA. The -3.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

FIGURE 8 – POSITIVE AND NEGATIVE REGULATOR



QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066 consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

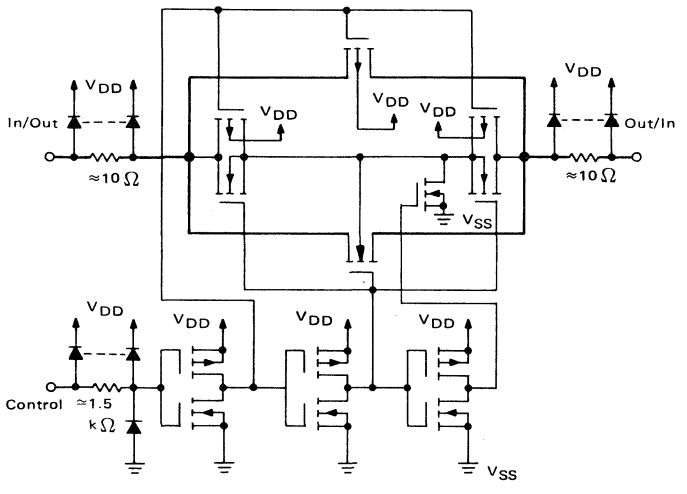
The MC14066 is designed to be pin-for-pin compatible with the MC14016, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio — 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches —50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS} (at 15V)
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



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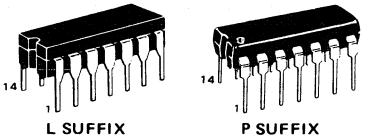
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER

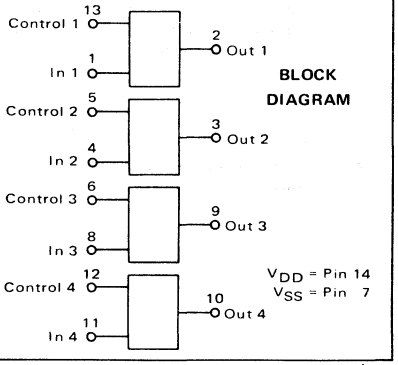


L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

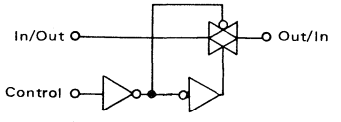
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



BLOCK DIAGRAM

LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0	OFF
1	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Input Current (AL Device) Control	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device) Control	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control Input		–	–	–	–	5.0	–	–	–	
Switch Inputs		10	–	–	–	8.0	–	–	–	
Output Capacitance	C_{out}	10	–	–	–	8.0	–	–	–	pF
Feedthrough Capacitance	C_{in-out}	10	–	–	–	0.5	–	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_Q	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
ON Resistance (AL Device)	R_{ON}	5.0	–	800	–	250	1050	–	1300	Ω
		10	–	400	–	120	500	–	550	
		15	–	220	–	80	280	–	320	
ON Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
		10	–	450	–	120	500	–	520	
		15	–	250	–	80	280	–	300	
ΔON Resistance Between Any Two of Four Switches	ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	–	–	
Input/Output Leakage Current Switch OFF (AL Device)	–	15	–	±100	–	±0.01	±100	–	±1000	nAdc
Input/Output Leakage Current Switch OFF (CL/CP Device)	–	15	–	±300	–	±0.01	±300	–	±1000	nAdc

*The formulas given are for the typical characteristics only.
T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Times	V_{SS} = 0 Vdc						
Input to Output (R_L = 10 kΩ)		t_{PLH},t_{PHL}					ns
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns			5.0	20	30	45	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns			10	10	15	30	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns			15	7.0	10	20	
Control to Output (R_L = 300 Ω)							
Output "1" to High Impedance		$t_{"1"H}$	5.0	35	50	100	ns
			10	30	45	90	
			15	25	38	75	
Output "0" to High Impedance		$t_{"0"H}$	5.0	30	45	90	ns
			10	25	38	75	
			15	20	30	60	
High Impedance to Output "1"		$t_{H"1"}$	5.0	60	90	180	ns
			10	20	30	60	
			15	15	22	45	
High Impedance to Output "0"		$t_{H"0"}$	5.0	60	90	180	ns
			10	16	25	50	
			15	14	20	40	
Sine Wave Distortion (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	V_{SS} = -5 Vdc	–	5.0	0.1	–	–	%
Frequency Response (Switch ON) (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -3 dB)	V_{SS} = -5 Vdc	–	5.0	65	–	–	MHz
Feedthrough Attenuation (Switch OFF) (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -50 dB)	V_{SS} = -5 Vdc	–	5.0	1.0	–	–	MHz
Crosstalk Between Any Two Switches (R_L = 1 kΩ, $20 \log_{10}\frac{V_{out(B)}}{V_{in(A)}}$ = -50 dB, (Switch A ON, Switch B OFF)	V_{SS} = -5 Vdc	–	5.0	8.0	–	–	MHz
Crosstalk, Control Input to Signal Output	V_{SS} = -5 Vdc	–	5.0	50	–	–	mV
Maximum Control Input Frequency ($20 \log_{10}\frac{V_{out}}{V_{in}}$ = -6 dB)	V_{SS} = 0 Vdc	–	5.0	6.0	–	–	MHz
			10	8.0	–	–	
			15	8.5	–	–	

*The formulas given are for the typical characteristics only.
T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

TEST CIRCUITS

FIGURE 1 – NOISE IMMUNITY

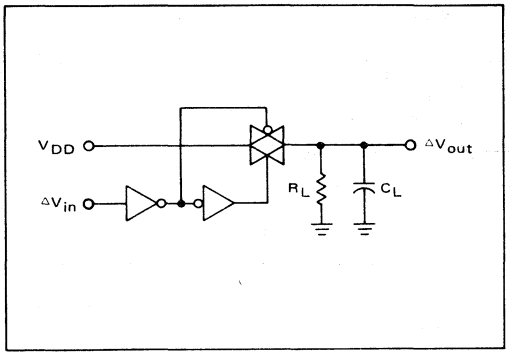


FIGURE 2 – PROPAGATION DELAY TIME, CONTROL TO OUTPUT

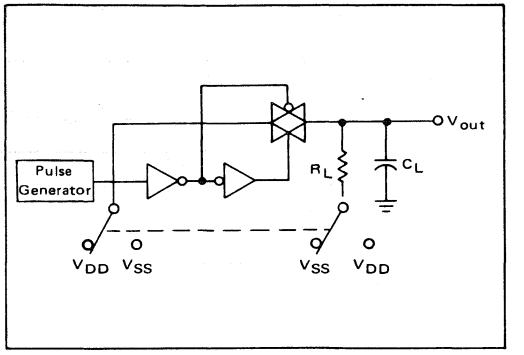


FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

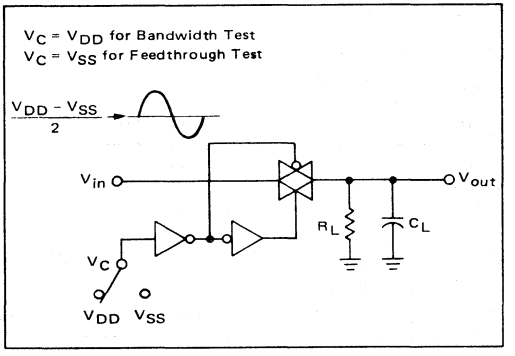


FIGURE 4 – CROSSTALK BETWEEN ANY TWO SWITCHES

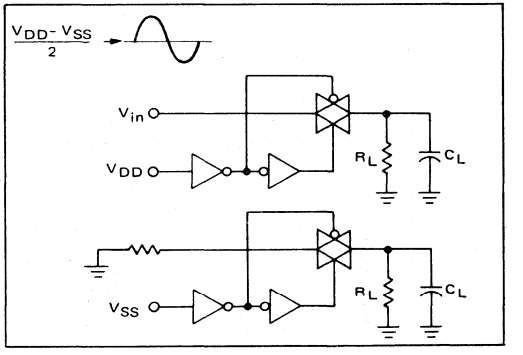


FIGURE 5 – FEEDTHROUGH, CONTROL TO OUTPUT

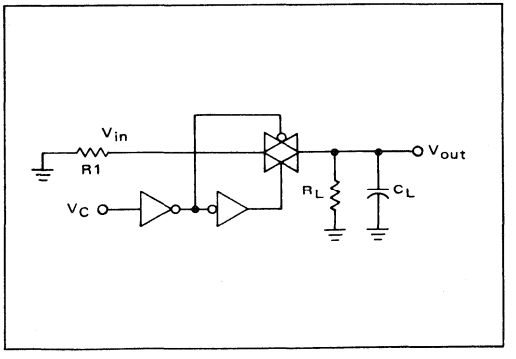


FIGURE 6 – MAXIMUM CONTROL FREQUENCY

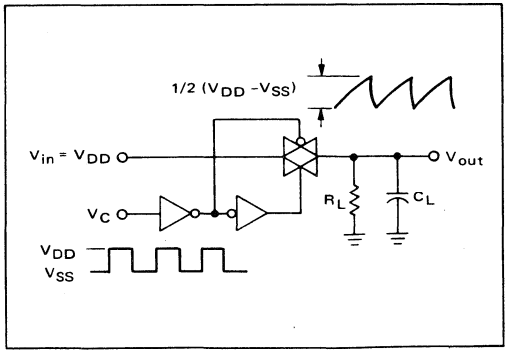
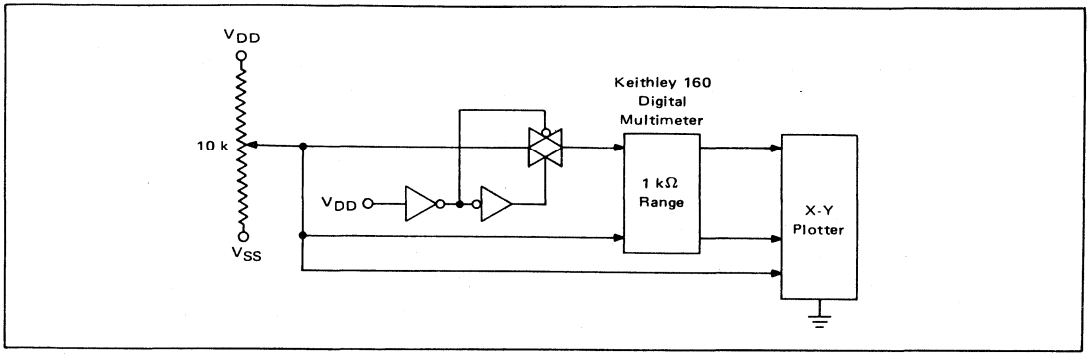


FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V

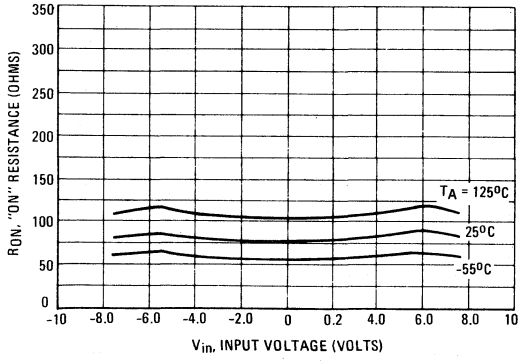


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V

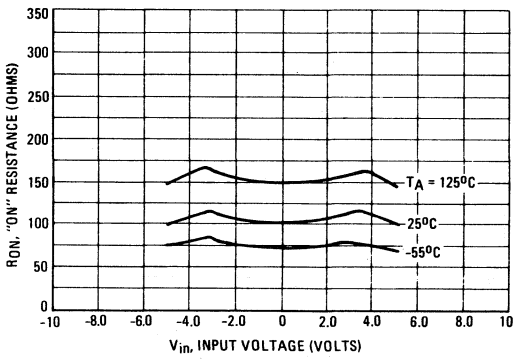


FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

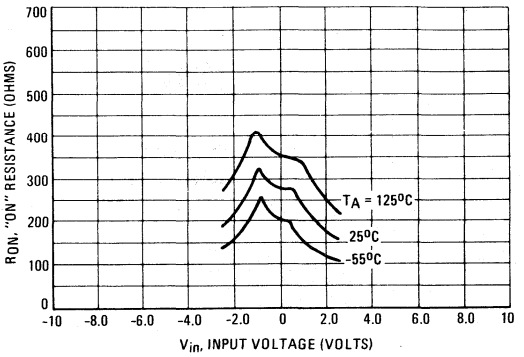
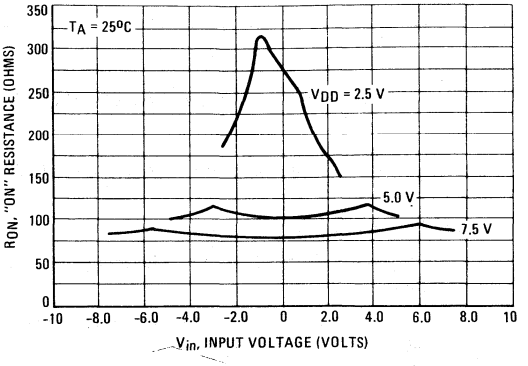


FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}



MC14422P

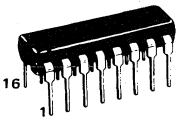
REMOTE CONTROL TRANSMITTER

The MC14422 is a remote control transmitter circuit in CMOS technology.

- 22 Ultrasonic channel capability.
- Transmission of information is achieved by time multiplexing 5 ultrasonic frequencies.
- The chosen frequency band is free from line frequency harmonics generated in television receivers.
- Suitable for application with ultrasonic or infrared transducers.
- Low external component count.
- Low power consumption.
- Designed to be used in conjunction with the remote control receiver integrated circuits MC6525, MC6526, MC6527, MC6529.

CMOS

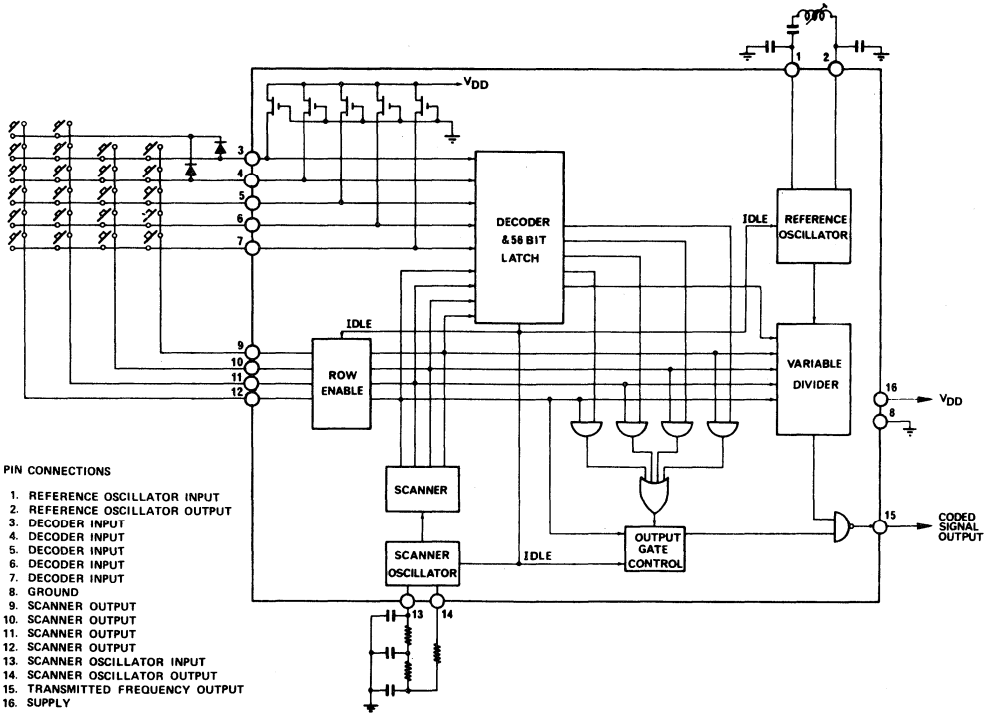
REMOTE CONTROL TRANSMITTER



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

FIGURE 1 – BLOCK DIAGRAM & PIN ASSIGNEMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+10 to − 0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +55	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Voltage	16	5		8	Vdc
Supply Current Idle (V_{DD} = 8 V) Operating (V_{DD} = 8 V)	16		5.0	100 10	μA mA
Transmitted Frequency Output Drive Current Source V_{OH} = 4 V, V_{DD} = 5 V Sink V_{OL} = 1 V, V_{DD} = 5 V	15	 −0.4 0.2			 mA mA
Scanner Output Drive Current Source V_{OH} = 4 V, V_{DD} = 5 V Sink V_{OL} = 1 V, V_{DD} = 5 V	9, 10, 11, 12	 −50 50			 μA μA
Scanner Oscillator Input Current Source V_{IL} = 0 V, V_{DD} = 8 V Sink V_{IH} = 8 V, V_{DD} = 8 V	13			 1.0 1.0	 μA μA
Scanner Oscillator Output Drive Current Source V_{OH} = 4 V, V_{DD} = 5 V Sink V_{OL} = 1 V, V_{DD} = 5 V	14	 −0.1 0.1			 mA mA
Reference Oscillator Input Current Source V_{IL} = 0 V, V_{DD} = 8 V Sink V_{IH} = 8 V, V_{DD} = 8 V	1	 −4.0 4.0		 −400 400	 μA μA
Reference Oscillator Output Drive Current Source V_{OH} = 4 V, V_{DD} = 5 V Sink V_{OL} = 1 V, V_{DD} = 5 V	2	 −0.3 0.3			 mA mA
Reference Oscillator Frequency V_{DD} = 5 V	2	 0.1		 1.0	 MHz
Decoder Input Current Source V_{IH} = 7 V, V_{DD} = 8 V Sink V_{IL} = 1 V, V_{DD} = 5 V	3, 4, 5, 6, 7	 −1.0		 −25	 μA μA

CIRCUIT OPERATION

Referring to the timing diagram (Fig. 2) it can be seen that until a matrix switch is depressed, pins 3, 4, 5, 6, 7 (decoder inputs) are high, all scanner outputs, pins 9, 10, 11 and 12 are low and both the scanner and reference oscillators are off. This is referred to as the "idle" mode. This mode reduces current consumption to a minimum. The decoder section however, remains in continuous operation so that a switch matrix command can be recognised.
When a switch is depressed, the decoder (see Fig. 1) will set the 5 latches in accordance with the correct code. At the same time a latch is triggered which activates the idle line and turns on the reference oscillator, the scanner oscillator, the row enable, and the output gate control.
When the switch is operated just prior to time period t_1 the following happens:

- The scanner outputs become active and take up their respective code corresponding to t_1 when the next negative going edge of the scanner oscillator occurs.
- The reference oscillator is activated.
- The output gate control idle input is enabled.

NOTE: No output can occur at pin 15 until the negative going edge of the pin 12 scanner signal has occurred at the end of t_4.

In the timing example the matrix connection of pin 4 to 11 has been selected. Referring to the frequency code table (Fig. 3) it can be seen that the code for 4-11 is f_a transmitted in time slot t_2 and f_b transmitted in time slot t_3. After the negative going edge of the pin 12 scanner pulse has enabled the output gate control, an output cycle can begin. Therefore, in this case no output occurs in the time slot t_1, f_a and f_b are transmitted in time slots t_2 and t_3 recpectively and again no output occurs during t_4. The code is repeated continuously at pin 15 until the matrix switch is released. At this point the circuit completes the scan cycle and the trailing edge of the pin 12 scanner signal returns the circuit to its "idle" position.
The transmitted frequencies are generated by dividing a reference oscillator frequency by a variable divider circuit which is controlled by the decoder outputs.

FIGURE 2 – TIMING DIAGRAM

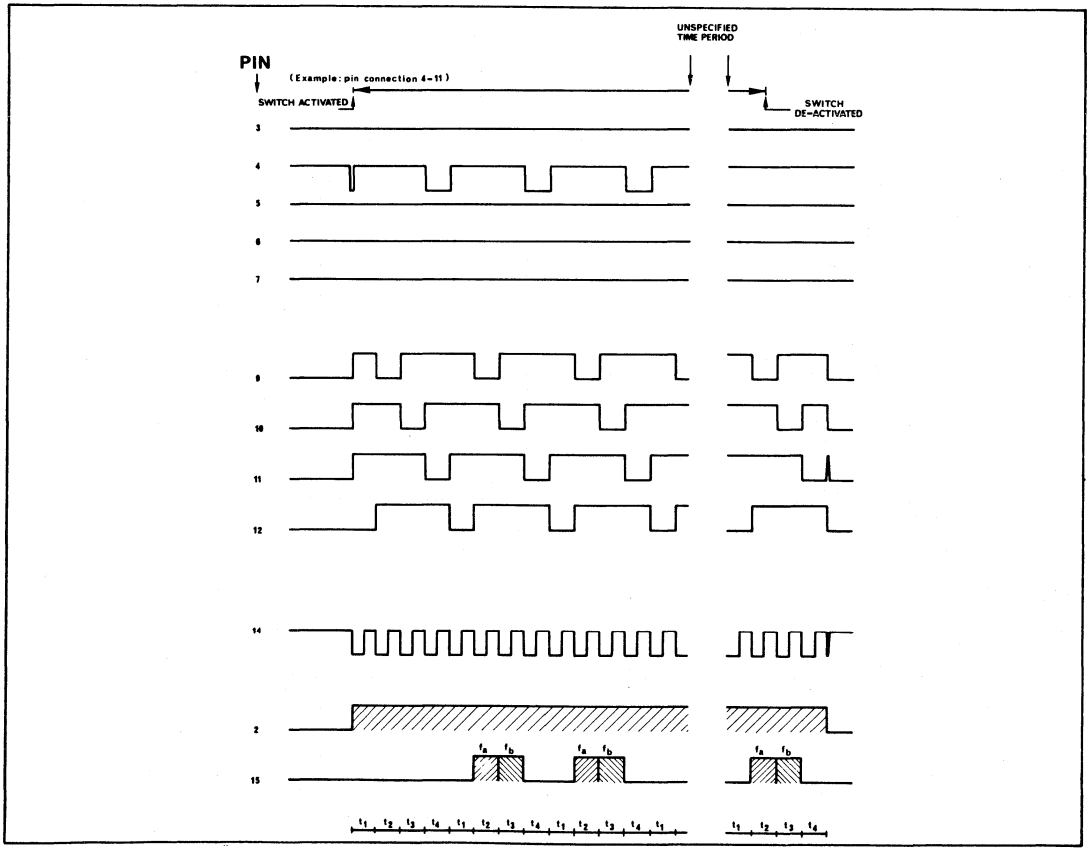


FIGURE 3 – TRANSMITTED FREQUENCY CODE

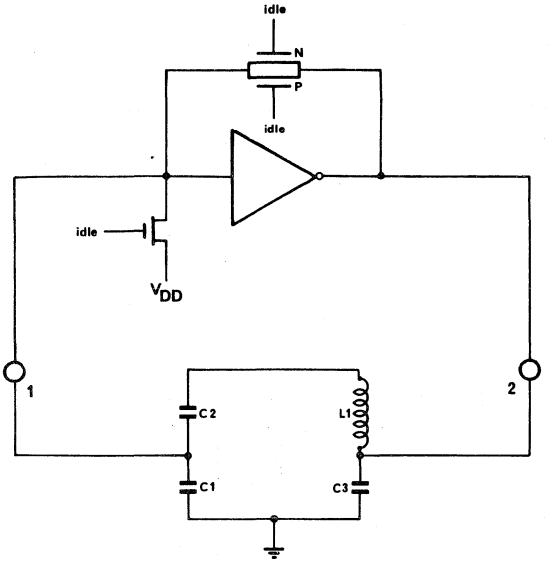
Channel Number	Matrix connections		Transmitted frequencies			
	Pin	to Pin	t_1	t_2	t_3	t_4
1	7	12	f_e			
2	7	9	f_e	f_a		
3	7	10	f_e		f_b	
4	7	11	f_e	f_a	f_b	
5	6	12	f_e			f_c
6	6	9	f_e	f_a		f_c
7	6	10	f_e		f_b	f_c
8	6	11	f_e	f_a	f_b	f_c
9	5	12	f_e			f_d
10	5	9	f_e	f_a		f_d
11	5	10	f_e		f_b	f_d
12	5	11	f_e	f_a	f_b	f_d
13	4	12			f_b	
14	4	11		f_a	f_b	
15	3	9				f_c
16	3	10		f_a		f_c
17	4	9			f_b	f_c
18	4	10		f_a	f_b	f_c
19	3	12				f_d
20	3	11		f_a		f_d
21	3 & 4	12			f_b	f_d
22	3 & 4	11		f_a	f_b	f_d

FIGURE 4 – OUTPUT FREQUENCIES

Frequencies	Output frequency	Division ratio
f_a	34.688 KHz	$\frac{f_2}{26.5}$
f_b	36.048 KHz	$\frac{f_2}{25.5}$
f_c	37.519 KHz	$\frac{f_2}{24.5}$
f_d	39.116 KHz	$\frac{f_2}{23.5}$
f_e	42.755 KHz	$\frac{f_2}{21.5}$

f_2 = 919.222 KHz reference frequency.

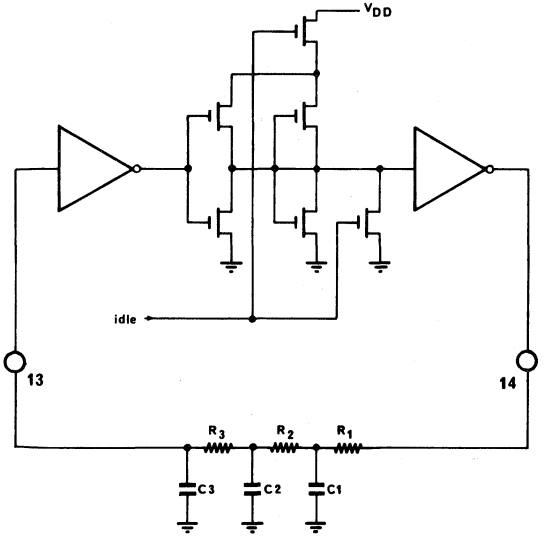
FIGURE 5 – REFERENCE OSCILLATOR, EXTERNAL COMPONENTS



Recommended values for $f_2 \cong 919$ KHz

C1 = 820 pF
C2 = 180 pF
C3 = 820 pF
L1 = 160 μH, Q $\geqslant$ 60.

FIGURE 6 – SCANNER OSCILLATOR, EXTERNAL COMPONENTS



The scanner oscillator frequency can be calculated using the following formula:

$$f_{14} = \frac{\sqrt{3}}{2\pi\ RC}$$

Recommended values for f_{14} = 100 Hz:

R1 = 47 K	C1 = 69 nF
R2 = 100 K	C2 = 33 nF
R3 = 180 K	C3 = 15 nF

FIGURE 7 – ULTRASONIC REMOTE CONTROL TRANSMITTER TYPICAL CIRCUIT DIAGRAM

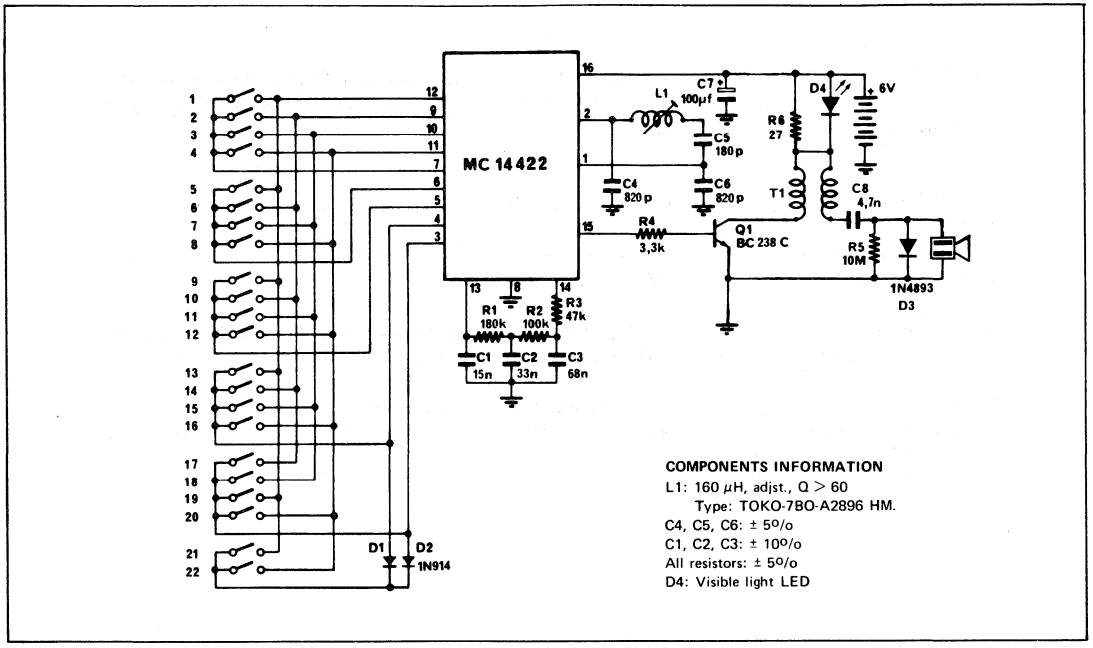
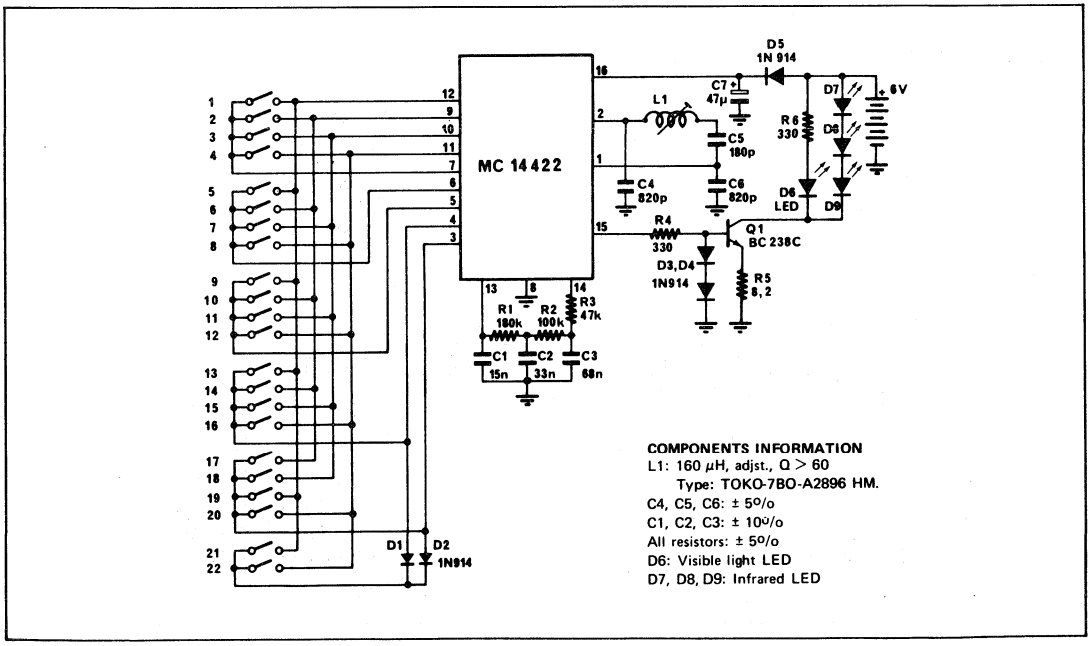


FIGURE 8 – INFRARED REMOTE CONTROL TRANSMITTER TYPICAL CIRCUIT DIAGRAM



APPLICATION INFORMATION

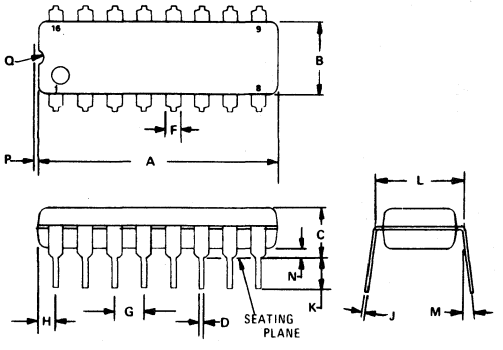
KEYBOARD LAYOUT – Due to the high impedance of the CMOS MC14422 decoder inputs, it is recommended to minimise cross coupling between the switch matrix connections by providing for generous ground plane whenever possible.

ADJUSTMENT PROCEDURE – L1 to be adjusted for a reference oscillator frequency at pin 2 of 919222 Hz.
However, since the scanner oscillator can be stopped for continuous wave output, the following production oriented procedure is recommended:

1 – A special test jig is required capable of grounding pin 13 as soon as an output on pin 15 is detected. By doing so the transmitter scanner oscillator can be stopped on the desired output frequency f_e.

2 – Connect the above test jig to pin 13 and 15, plus a frequency counter also to pin 15.
Press the switch corresponding to channel 1 and adjust L1 to read f_e = 42755 Hz. All other ultrasonic frequencies will be automatically calibrated.

PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

PLASTIC PACKAGE
Case 648

ADVANCE INFORMATION

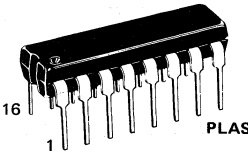
CMOS

REMOTE CONTROL TRANSMITTER

REMOTE CONTROL TRANSMITTER

The MC14424 is a remote control transmitter circuit in CMOS high performance technology.

- 31 channel capability
- Transmission of information is achieved by time multiplexing 5 modulation frequencies
- The chosen frequency band is free from line frequency harmonics generated in television receivers
- Suitable for application with ultrasonic or infrared transducers
- Extremely low external component count
- Low power consumption
- Designed to be used in conjunction with the remote control receiver integrated circuits MC6525, MC6526, MC6527, MC6529.



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

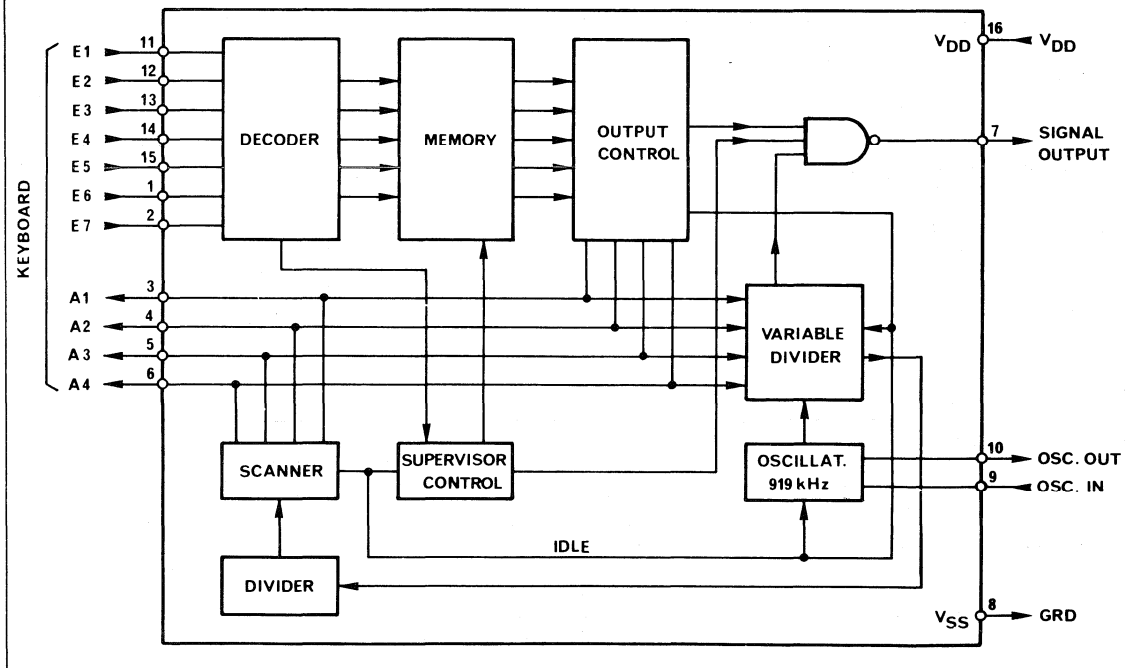


FIGURE 1 – BLOCK DIAGRAM & PIN ASSIGNEMENT

MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+12 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +55	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

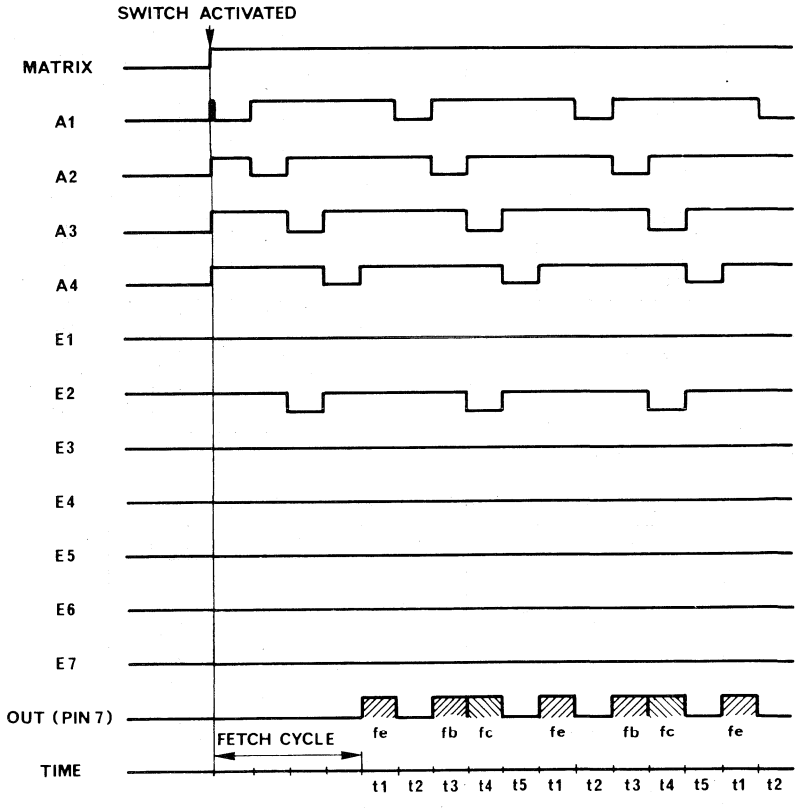
ELECTRICAL CHARACTERISTICS (T_A = 0 to 55 °C)

Characteristics	Pin	Min.	Typ.	Max.	Unit
Supply Voltage	16	4		9.6	Vdc
Supply Current Idle (V_{DD} = 6.4 V) Operating (V_{DD} = 6.4 V)	16		0.1 2	100	μA mA
Transmitted Frequency Output Drive Current Source (V_{OH} = V_{DD} −1 V) (V_{DD} = 4 V) Sink (V_{OL} = 1 V) (V_{DD} = 4 V)	7	 −1 0.2			 mA mA
Scanner Output Drive Current Source (V_{OH} = V_{DD} −1 V) (V_{DD} = 4 V) Sink (V_{OL} = 1 V) (V_{DD} = 4 V)	3, 4, 5, 6	 −50 0.6			 μA mA
Reference Oscillator Input Current Source (V_{IL} = 0 V) (V_{DD} = 6.4 V) Sink (V_{IH} = 6.4 V) (V_{DD} = 6.4 V)	9	 −2 2		 −200 200	 μA μA
Reference Oscillator Output Drive Current Source (V_{OH} = 3 V) (V_{DD} = 4 V) Sink (V_{OL} = 1 V) (V_{DD} = 4 V)	10	 −1.2 1.8			 mA mA
Reference Oscillator Frequency (V_{DD} = 4 V)	9	0.1	0.919	1.0	MHz
Decoder Input Current Source (V_{IH} = 5.4 V) (V_{DD} = 6.4 V) Sink (V_{IL} = 1 V) (V_{DD} = 4 V)	1, 2, 11, 12 13, 14, 15	 −10 		 −100	 μA μA

CIRCUIT OPERATION

In the stand-by mode, the scanning outputs A1, A2, A3, A4 are forced to "0" by the scan output stages, decoder inputs E1....E7 (see block diagram, Fig. 1) are forced to "1" by internal pull-up devices. If any of the keys of the matrix is now operated, the appropriate input will be forced to "0" and hence the circuit is instructed that a key has been operated. The supervisory control will now enable the reference oscillator and will release the scanning outputs. During the first scan cycle, called the fetch cycle, the IC is identifiying the key which initiated the fetch cycle. The memory will load the corresponding 5 bit word containing the modulation frequency combination to be supplied the output.

In the operating mode, the variable divider is generating sequentially five modulation frequencies (see Fig. 4). The sequence is controlled by the scanner. Frequency f_e is generated at time t_1, f_d at time t_2, f_b at time t_3, f_c at time t_4 and f_a at time t_5 (see timing diagram, Fig. 2). Following the fetch cycle, the output control block will enable the output buffer according to the wanted frequency combination, always beginning at t_1. Transmitted frequencies f_a...f_e and the scanner timing of 10 msec are both derived from a reference LC oscillator externally adjustable at 919 KHz.



EXAMPLE ABOVE: CHANNEL 7, CONNECTION A3 – E2

FIGURE 2 – TIMING DIAGRAM

FIGURE 4 – OUTPUT FREQUENCIES

COMMAND[1]		Transmitted frequencies						Matrix connections	
		Channel	f_a	f_b	f_c	f_d	f_e	Pin	to Pin
Program + ON									
1		1	0	0	0	0	1	11	3
2		2	1	0	0	0	1	11	4
3		3	0	1	0	0	1	11	5
4		4	1	1	0	0	1	11	6
5		5	0	0	1	0	1	12	3
6		6	1	0	1	0	1	12	4
7		7	0	1	1	0	1	12	5
8		8	1	1	1	0	1	12	6
9		9	0	0	0	1	1	13	3
10		10	1	0	0	1	1	13	4
11		11	0	1	0	1	1	13	5
12		12	1	1	0	1	1	13	6
13		13	0	0	1	1	1	14	3
14		14	1	0	1	1	1	14	4
15		15	0	1	1	1	1	14	5
16		16	1	1	1	1	1	14	6
Colour saturation	CS–	17	0	1	0	0	0	15	5
	CS+	18	1	1	0	0	0	1	3
Volume	VO–	19	0	0	1	0	0	15	3
	VO+	20	1	0	1	0	0	1	4
Brightness	BR–	21	0	1	1	0	0	15	6
	BR+	22	1	1	1	0	0	1	6
Standby	STB	23	0	0	0	1	0	2	3
Sound killer	SK	24	1	0	0	1	0	2	4
General Purpose	Q25	25	0	1	0	1	0	2	5
General Purpose	Q26	26	1	1	0	1	0	2	6
General Purpose	Not decoded by receiver	27	1	0	0	0	0	15	4
General Purpose		28	0	0	1	1	0	1	5
General Purpose		29	1	0	1	1	0	1 & 2	4
General Purpose		30	0	1	1	1	0	1 & 2	5
General Purpose		31	1	1	1	1	0	1 & 2	6

[1] When used in conjunction with the MC6529 receiver.

FIGURE 3 – TRANSMITTED FREQUENCY CODE

Frequencies	Timing	Output frequency	Division ratio
f_a	t_5	34.688 KHz	$\frac{f_2}{26.5}$
f_b	t_3	36.048 KHz	$\frac{f_2}{25.5}$
f_c	t_4	37.519 KHz	$\frac{f_2}{24.5}$
f_d	t_2	39.116 KHz	$\frac{f_2}{23.5}$
f_e	t_1	42.755 KHz	$\frac{f_2}{21.5}$

f_2 = 919.222 KHz reference frequency

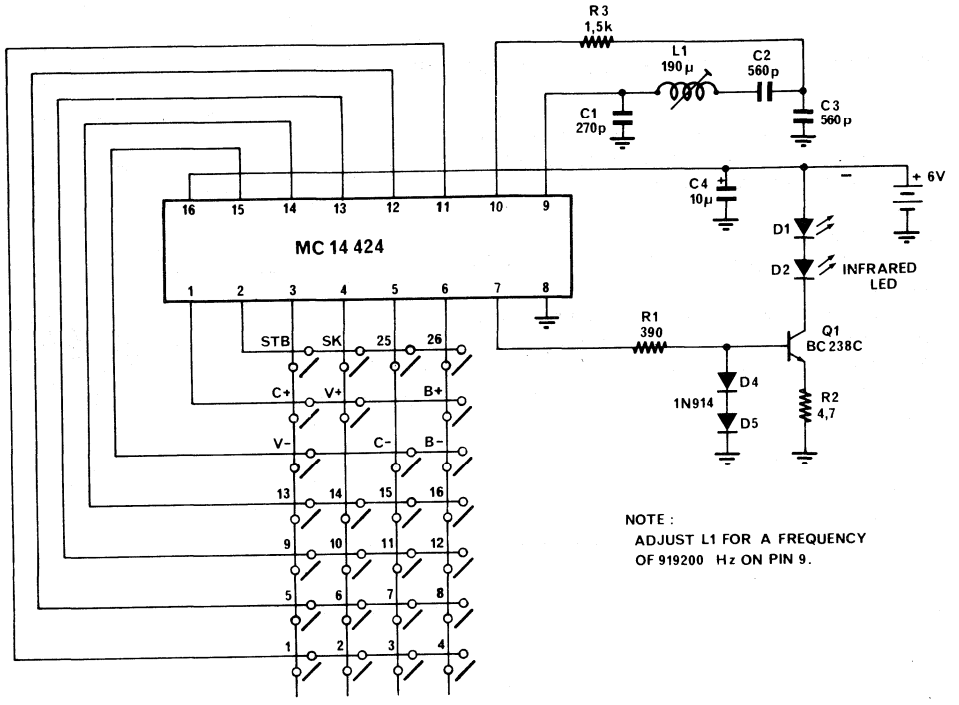
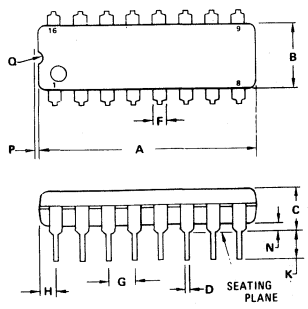
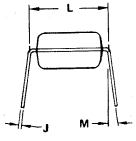


FIGURE 5 – INFRARED REMOTE CONTROL TRANSMITTER TYPICAL CIRCUIT DIAGRAM

PACKAGE DIMENSIONS



PLASTIC PACKAGE
CASE 648



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC14425P

TUNING MEMORY SYSTEM CONTROL CIRCUIT

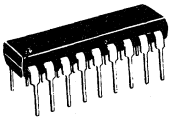
The MC14425 Control circuit will perform the following functions when used in conjunction with the MC14426 Memory and the UAA1008 or UAA1008A Linear Processors.

- LC Clock generator
- UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- 2, 3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual search of TV stations
- Automatic volume muting control during search and program change

CMOS

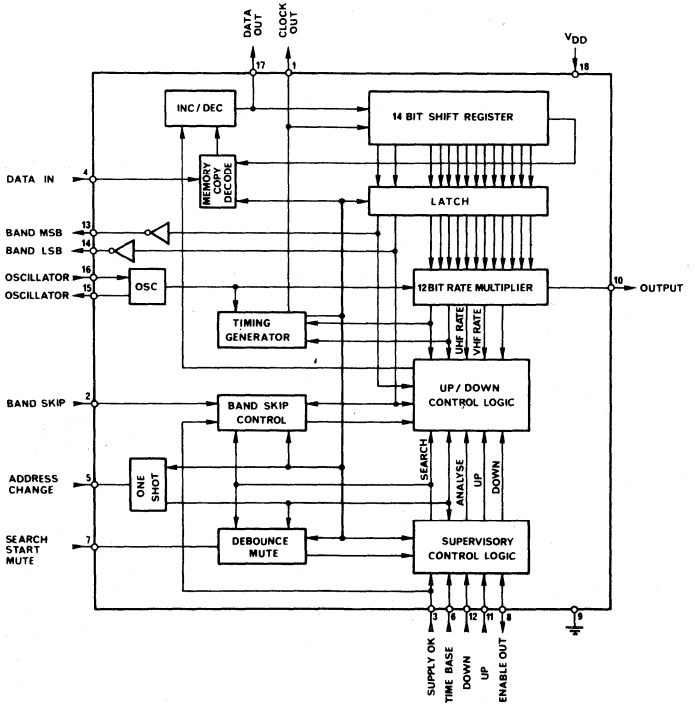
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

FIGURE 1 – MC14425 BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Voltages referenced to V_{SS}, pin 9

Characteristics	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Operating Range	18	V_{DD}		4.95	5.2	6	Vdc
Input Current, All inputs (except pins 5, 7)		I_{in}		–	10	–	pAdc
Enable Output Current	8	I_{OH} I_{OL}	V_{DD} −0.4 V 0.4 V	280 280			μAdc μAdc
Band Switching Output Current	13, 14	I_{OH} I_{OL}	V_{DD} −0.4 V 0.4 V	280 280			μAdc μAdc
Other Output Currents	1 10, 17	I_{OH} I_{OL}	V_{DD} −0.4 V_{OL} = 0,4 V	280 280			μAdc μAdc
One Shot Output, Search & Mute (see[1])	5, 7	I_{OL}	V_{OL} = 0,4	280			μA
Oscillator	15	I_{OH} I_{OL}	V_{DD} −0.4 V V_{OL} = 0.4 V	160 160			μA μA
Power Dissipation		P_D	@200 KHz		5		mW
Oscillator Frequency		f_o		50		350	KHz

[1] An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed[1]
UHF	0	0	10 sec.
VHF 1	1	0	2.5 sec.
VHF 3	0	1	2.5 sec.
CABLE	1	1	2.5 sec.

[1] At 200 KHz Clock frequency

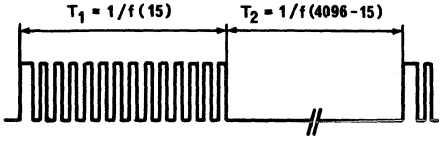
Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

CLOCK OUT – Clock pulses (PIN 1) control the transfer of data between the MC14425 control chip and the MC14426 memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 200 KHz, however frequency value is not critical.
The clock out signal timing is shown below.



f = Oscillator frequency;
$T_1 + T_2$ = Rate Multiplier;
T_1 = Shift Cycle.

BRM OUTPUT – The binary rate multiplier output is available on pin 10.
The binary word cycle is approximately 20msec for a clock frequency of 200KHz (5 μsec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A convertion.
In the block diagram of Figure 1 the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE – Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 10msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 10 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.
Mute is also provided when supply OK input (pin 3) is V_{SS}.
Three search modes are present:

1. Fast search, generally used for VHF applications, with a rate of change of 32 steps per clock cycle and a scan time of 2.5 seconds.
2. Slow search, generally used for UHF applications, with a rate of change of 8 steps per clock cycle and a scan time of 10 seconds.
3. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 80 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK – An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc... no memory information can be modified or lost. In operating conditions it should receive a 1 from the linear processor UAA1008. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the shift register.
However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified.

TIME BASE – This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processor circuit UAA1008. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 400 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached.
Should time base be 0 when the one shot times out, search will resume if the system was in search mode.
If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to the tristate condition.

ENABLE OUT – This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear processor circuit UAA1008.
Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	Enable OUT (PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	X	X	1

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received.
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.

UP & DOWN – These two inputs (pin 11 & 12) have two modes of operation.
When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1,

will interact with the system by stopping the search ramp. A 1 on only one of the two inputs neither stops search nor reduces search speed.

When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle.

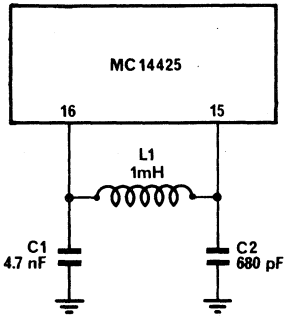
BAND CODE – Refer to band selection logic table for output code (pin 13 MSB, pin 14 LSB).

A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per table 1.

Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

APPLICATION INFORMATION

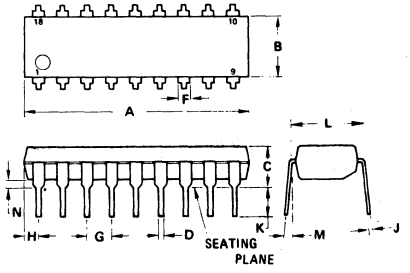
RECOMMENDED OSCILLATOR CONFIGURATION



f_O = 200 KHz

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 701-01



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

MC14426P

TUNING MEMORY SYSTEM MEMORY CIRCUIT

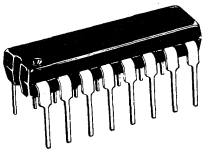
The MC14426 Memory Circuit provides the storage of the tuning voltage and band information for 8 TV stations when used in conjunction with the MC14425/9 Control Unit.

- 8 static shift registers of 14 bit length
- Expansion of up to 32 channels possible without external logic
- Output available indicating address change
- Low voltage (1 volt) technology requires a single cell battery as back up power source
- Extremely low power consumption

CMOS

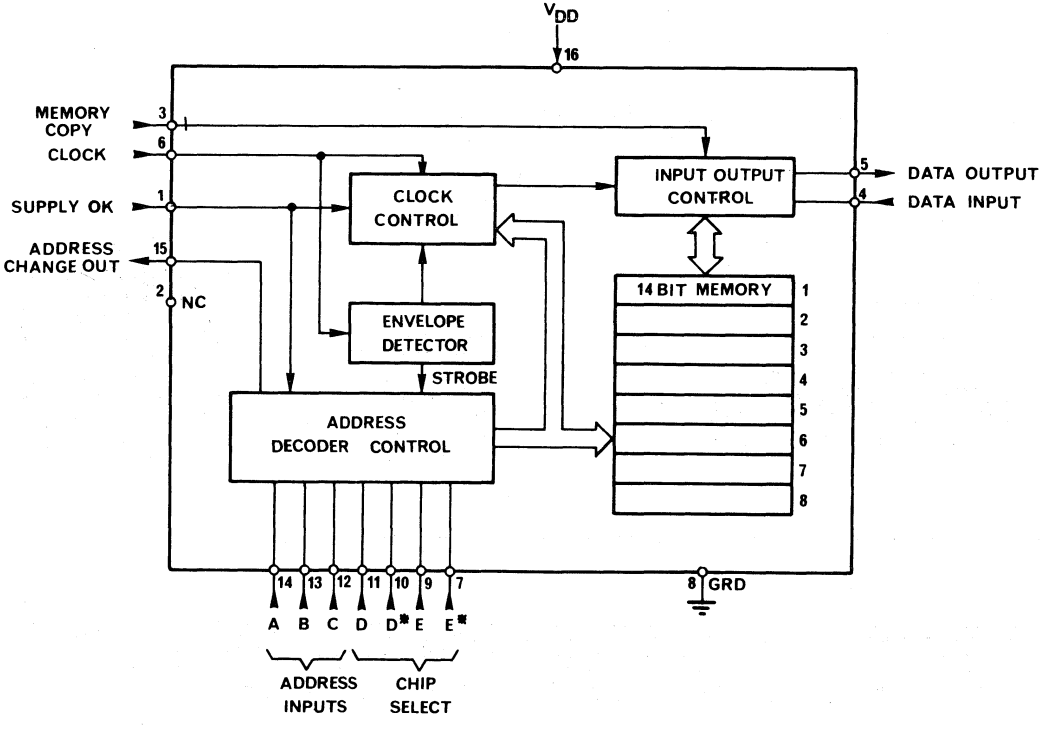
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM MEMORY CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – MC14426 BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current drain per pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Voltages referenced to V_{SS}, pin 8

Characteristic	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Supply Voltage	16	V_{DD}		4.0	5.2	6.0	Vdc
Standby Supply Voltage	16	V_{DD}	See[1]	1.2	1.5	6.0	Vdc
Quiescent Current	16	I_{DD}	V_{DD} = 1.5 Vdc V_{DD} = 5 Vdc		0.008 0.5	2.0 15.0	μAdc
Input Voltage	3, 6	V_{IL} V_{IH}	V_{DD} = 5 Vdc	 4.5		0.5	Vdc
Input Voltage	1, 4, 7, 9, 10, 11 12, 13, 14	V_{IL} V_{IH}	V_{DD} = 5 Vdc	 4.0		1.0	Vdc
Input Current all Inputs Except Pin 3.		I_{IN}	V_{DD} = 5 Vdc		10		pAdc
Input Current (see[2])	3	I_{IN}	V_{DD} = 5 Vdc	−1.5	−3.0	−6.0	μAdc
Input Capacitance all Inputs		C_{IN}	V_{IN} = 0		5.0	12.0	pF
Output Current all Outputs (sinking)		I_{OL}	V_{OL} = 0.4 V	0.4			mAdc
Three State Output Leakage Current (sinking)	5, 15	I_{TL}	V_{DD} = 5 V		±0.001	±5.0	μA
Clock Input Frequency	6	$f_{max.}$ $f_{min.}$	V_{DD} = 5 V	400	700 25	 100	KHz

[1] Standby mode is obtained by lowering Supply OK input to V_{SS} during a few read / write cycles. V_{DD} can then be lowered to its standby value, Pin 1 staying low.
In Standby mode no read / write operation can be performed.

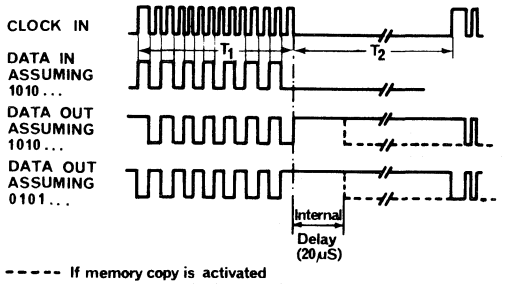
[2] An internal pull-up resistor is present on pin 3.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

DATA IN/OUT – The input/output control section provides the interface between the memory and the control circuit MC14425/9 via pins 5 and 4. The output network is active only when the chip is selected and supply OK (pin 1) is at 1. The relationship between clock and input/output signals is shown below:



----- If memory copy is activated

It should be noted that the memory copy information on pin 3 input is inserted into the serial data transfer line which goes to the control circuit during period T_2.

MEMORY COPY – This input is controlled by connecting pin 3 to V_{SS} (ground), which in turn holds down the memory output signal during period T_2. This function allows to transfer the content of the 14 bit shift register of the control circuit MC14425/9 into any memory location as long as this command is present.
Its utilisation is two-fold:

- To resume search for a TV station starting from the last selected station rather than from a random tuning voltage.
- To copy the content of a shift register into a different location. This permits to change the order of TV programs according to the user wish.

SUPPLY OK – In case of power failure this input (pin 1) is used to deactivate all functions of the chip so that no data is lost, rpovided that V_{DD} is held at 1 volt minimum. (See note 1.)
The supply OK signal is enabled in such a way that deactivation during transfer of information is prevented.

ADDRESS INPUTS – To select the 8 memory words only three A, B, C address bits are required. (pins 14, 13, 12.)

Channel	A	B	C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1

CHIP SELECT – To facilitate the parallel connection of several MC14426 memory circuits, four additional inputs D, D*, E, E* are provided for chip select.
The truth table of chip select inputs is given below.

Chip Selected	Channel	D	D*	E	E*
1	1 to 8	0	0	0	0
2	9 to 16	1	1	0	0
3	17 to 24	0	0	1	1
4	24 to 32	1	1	1	1
None	–	Any other combination			

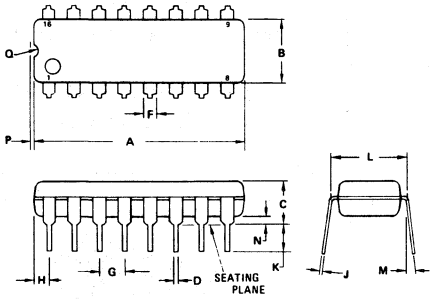
D* and E* are programming inputs of the chip select network and are normally connected to V_{SS} or V_{DD}.
The logic levels on these inputs specify the levels of the D and E inputs for chip selection.
The chip is selected if D = D* and E = E*.
As shown in the above truth table up to four circuits (32 channels) can be connected in parallel without external decoding.

CLOCK IN – (pin 6) See MC14425/9 data sheet.

ADDRESS CHANGE – An additional function (pin 15) is available to mute the sound section of the TV set during each address change. The 400msec. one-shot on the control circuit (MC14425/9) provides this feature. This one-shot is triggered by the address change signal supplied by the memory circuit. If the address is changed, the AC signal appears on the leading edge of the internal strobe pulse and lasts one ($T_1 + T_2$) cycle.

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 648



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC14429P

TUNING MEMORY SYSTEM CONTROL CIRCUIT

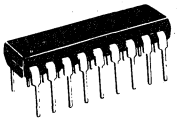
The MC14429 Control circuit will perform the following functions when used in conjunction with the MC14426 Memory and the UAA1008A Linear Processor.

- LC Clock generator
- UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- 2, 3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual search of TV stations
- Automatic volume muting control during search and program change

CMOS

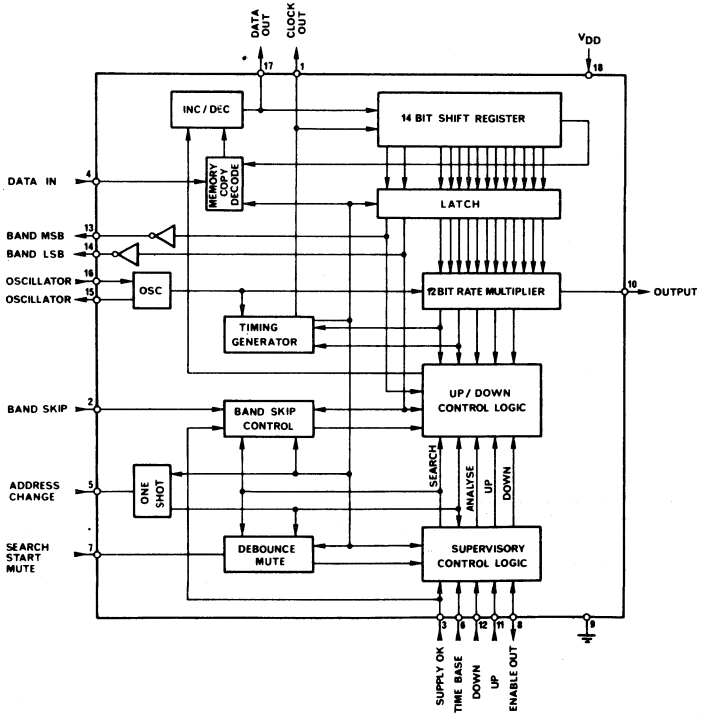
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

FIGURE 1 – MC14429 BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Voltages referenced to V_{SS}, pin 9

Characteristics	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Operating Range	18	V_{DD}		4.95	5.2	6	Vdc
Input Current, All inputs (except pins 5, 7)		I_{in}		–	10	–	pAdc
Enable Output Current	8	I_{OH} I_{OL}	V_{DD} −0.4 V 0.4 V	280 280			μAdc μAdc
Band Switching Output Current	13, 14	I_{OH} I_{OL}	V_{DD} −0.4 V 0.4 V	280 280			μAdc μAdc
Other Output Currents	1 10, 17	I_{OH} I_{OL}	V_{DD} −0.4 V_{OL} = 0,4 V	280 280			μAdc μAdc
One Shot Output, Search & Mute (see[1])	5, 7	I_{OL}	V_{OL} = 0,4	280			μA
Oscillator	15	I_{OH} I_{OL}	V_{DD} −0.4 V V_{OL} = 0.4 V	160 160			μA μA
Power Dissipation		P_D	@ 300 KHz		7.5		mW
Oscillator Frequency		f_o		50		350	KHz

[1] An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed[1]
UHF	0	0	7 sec.
VHF 1	1	0	7 sec.
VHF 3	0	1	7 sec.
CABLE	1	1	7 sec.

[1] At 300 KHz Clock frequency

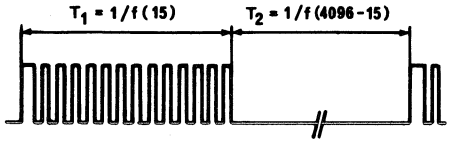
Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

CLOCK OUT – Clock pulses (PIN 1) control the transfer of data between the MC14429 control chip and the MC14426 memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 300 KHz, however frequency value is not critical.
The clock out signal timing is shown below.



f = Oscillator frequency;
$T_1 + T_2$ = Rate Multiplier;
T_1 = Shift Cycle.

BRM OUTPUT – The binary rate multiplier output is available on pin 10.
The binary word cycle is approximately 13 msec for a clock frequency of 300 KHz (3.3 μsec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A convertion.
In the block diagram of Figure 1. the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE – Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 10msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 10 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.
Mute is also provided when supply OK input (pin 3) is V_{SS}.
Two ramp modes are present:

1. Search mode, with a rate of change of 8 steps per clock cycle and a scan time of 7 seconds.
2. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 58 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK – An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc... no memory information can be modified or lost. In operating conditions it should receive a 1 from the linear processor UAA1008A. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the shift register.
However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified.

TIME BASE – This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processor circuit UAA1008A. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 200 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached.
Should time base be 0 when the one shot times out, search will resume if the system was in search mode.
If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to the tristate condition.

ENABLE OUT – This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear processor circuit UAA1008A.
Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	Enable OUT (PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	X	X	1
0	0	X	Tristate

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received.
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.
- The sixth line represents Address Change, enable out goes tristate during the on time of the one shot.

UP & DOWN – These two inputs (pin 11 & 12) have two modes of operation.
When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1,

will interact with the system by stopping the search ramp. A 1 on only one of the two inputs does not stop search nor reduce search speed.

When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle.

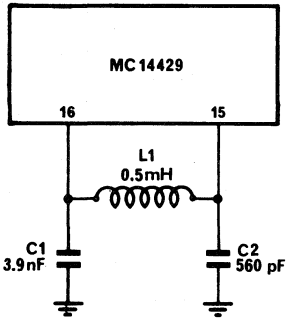
BAND CODE – Refer to band selection logic table for output code. (pin 13 MSB, pin 14 LSB).

A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per band selection logic table.

Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

APPLICATION INFORMATION

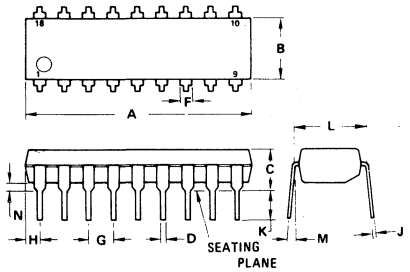
RECOMMENDED OSCILLATOR CONFIGURATION



$f_O = 300$ KHz

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 701-01



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

Comprehensive data sheet available January 1978.

ADVANCE INFORMATION

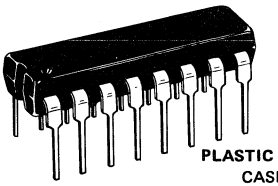
CMOS

INPUT ADDRESS ENCODER

INPUT ADDRESS ENCODER

The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

- 8 program inputs
- Binary coded open drain latched output
- Push button type keyboard allows for electrical isolation in live chassis applications
- Single or double keying operation possible
- Up to four circuits can be cascaded
- Normally closed or normally open switches can be used.



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

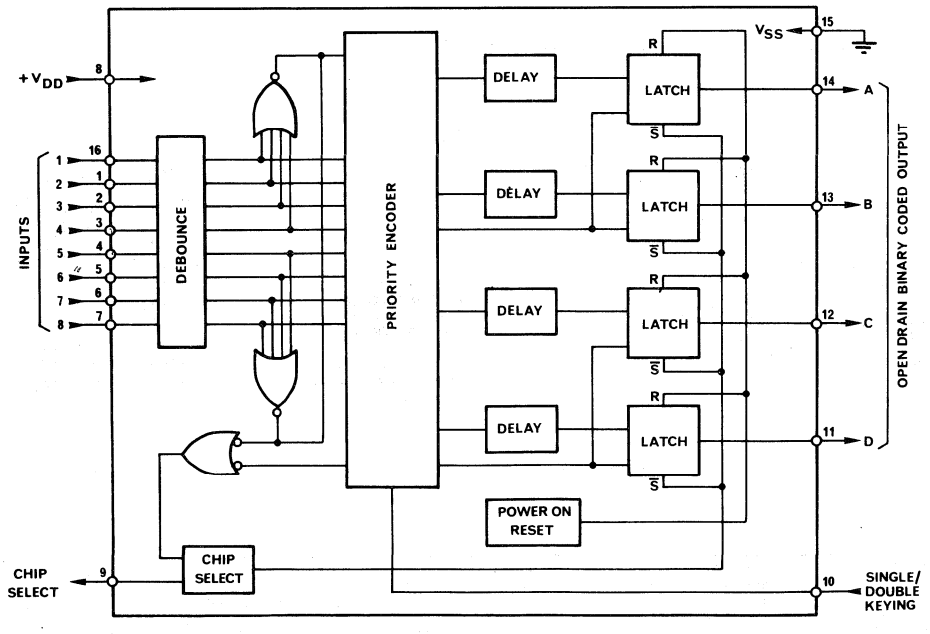


FIGURE 1 – MC14430 BLOCK DIAGRAM & PIN-OUT

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

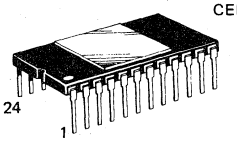
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- $Z_{in} > 1000$ M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs—Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count

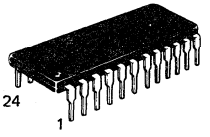
McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 716

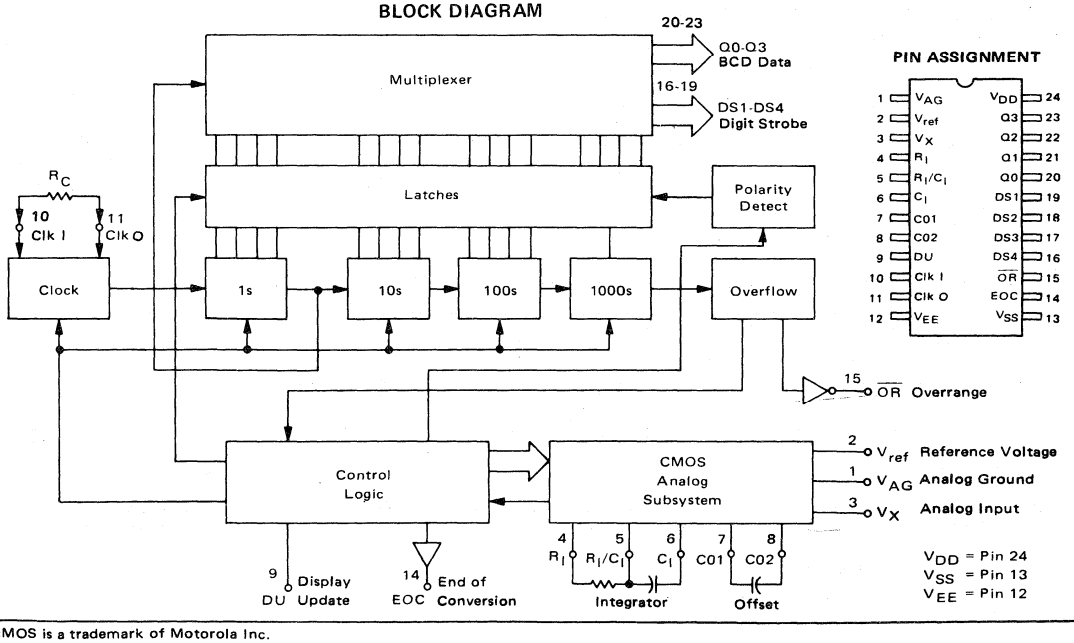


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT

McMOS is a trademark of Motorola Inc.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, any pin, referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground V_{EE} to Analog Ground	V_{DD} V_{EE}	+5.0 to +8.0 -2.8 to -8.0	Vdc
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{ref} = 2.000 V, R_I = 27 kΩ @ V_{ref} = 200.0 mV, C_o = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Linearity Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	-5.0			-0.05 -1 Count	±0.05	+0.05 +1 Count			
(V_{ref} = 200.0 mV)		5.0	-5.0								
Stability Output Reading	–										LSD
(V_X = 1.990 V, V_{ref} = 2.000 V)		5.0	-5.0					±1.0			
(V_X = 199.0 mV, V_{ref} = 200.0 mV)		5.0	-5.0					±1.0			
Zero Output Reading	–	5.0	-5.0				0	±1.0			LSD
(V_X = 0 V, V_{ref} = 2.000 V)											
Bias Current – Analog Input	–	5.0	-5.0				±20	±100			pAdc
Reference Input		5.0	-5.0				±20	±100			
Analog Ground		5.0	-5.0				±20	±500			
Common Mode Rejection		5.0	-5.0				65				dB
(V_X = 1.4 V, V_{ref} = 2.000 V, f_{oc} = 32 kHz)											
Output Voltage – Pins 14 to 23											Vdc
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	–	-4.95	–	-5.0	-4.95	–	-4.95	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current – Pins 14 to 23											mAdc
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.6	–	1.3	2.25	–	0.9	–	
Clock Frequency (Note 2)	f_{Clk}	5.0	-5.0				66				kHz
(R_C = 300 kΩ)											
Input Current – DU	I_{DU}	5.0	-5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Quiescent Current	I_Q	5.0	-5.0		3.7		0.9	2.0		1.6	mAdc
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	-8.0		7.4		1.8	4.0		3.2	
Supply Rejection	–	5.0	-5.0				0.5				mV/V
(V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000 V)											

Note 1: Accuracy – The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

Note 2: See Figure (table) 3 and Figure 4 for optimum NMRR.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

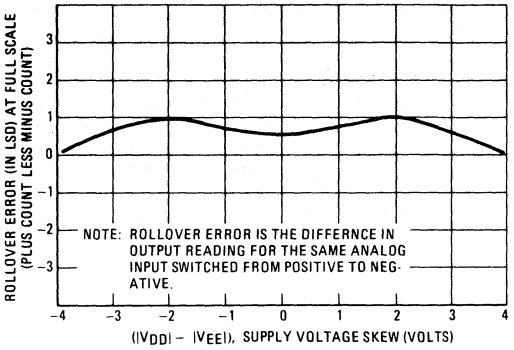


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

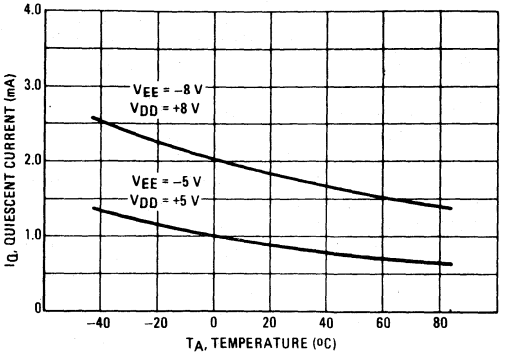


FIGURE (Table) 3 – FOR BEST 50 Hz NMRR (Normal Mode Rejection Ratio) AT DIFFERENT CLOCK FREQUENCIES

Clock frequency (KHz)	Integration time (msec)	Conversion rate (~ Hz)
200	20	12.5
100	40	6.25
66.6	60	4.16
50	80	3.12
40	100	2.5

The NMRR depends on the difference Δf (%) between a multiple of the power line frequency and the clock frequency.

FIGURE 4 – NMRR (dB) vs Δf (%)

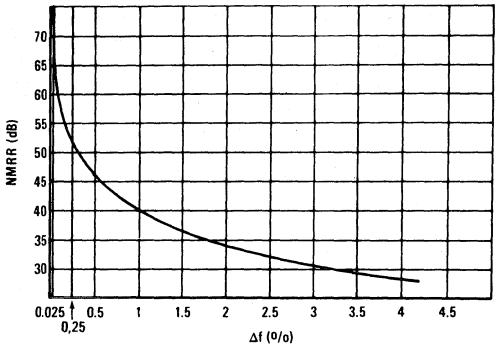


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

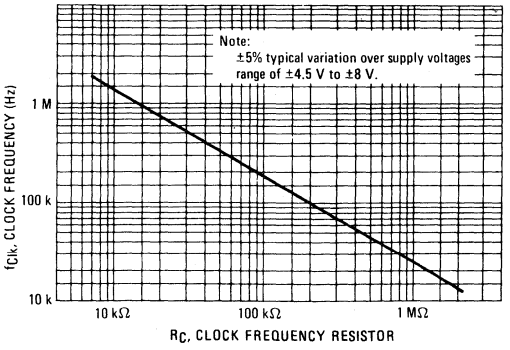
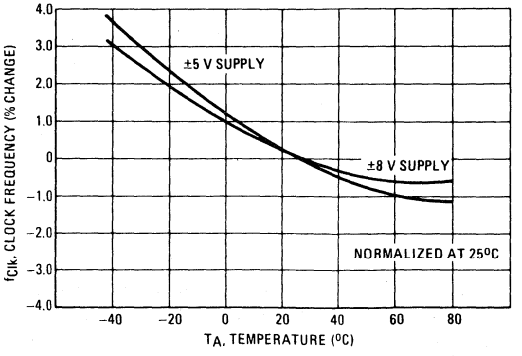


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

DEVICE OPERATION

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input.

REFERENCE VOLTAGE (V_{ref}, Pin 2)
UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, pin 2 functions as a reset for the A/D converter. When pin 2 is switched to V_{EE}, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T_N}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5$$

$$T_N = 4000 \times \frac{1}{f_{Clk}}$$

where:

V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{Clk} is the clock frequency at pin 10

Example:

$C_I = 0.1\ \mu F$
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480$ kΩ (use 470 k$\Omega \pm 5\%$)
For $V_X(max) = 200$ mV
$R_I = 28$ kΩ (use 27 k$\Omega \pm 5\%$)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow V + V_X to exceed V_{DD}. The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (CO1, CO2; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through pin 13.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$). When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between $V_{DD} - 3.0$ volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An inter-

digit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus, with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select ouptut and EOC signals is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q3, Q2, Q1, Q0; Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin.

RATIO OPERATION

The high impedance inputs of V_X and V_{ref} make the MC14433 very useful in ratio measurements. The count output is a simple relationship:

$$\text{Count output} = 2000 \times \frac{V_X}{V_{ref}}$$

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

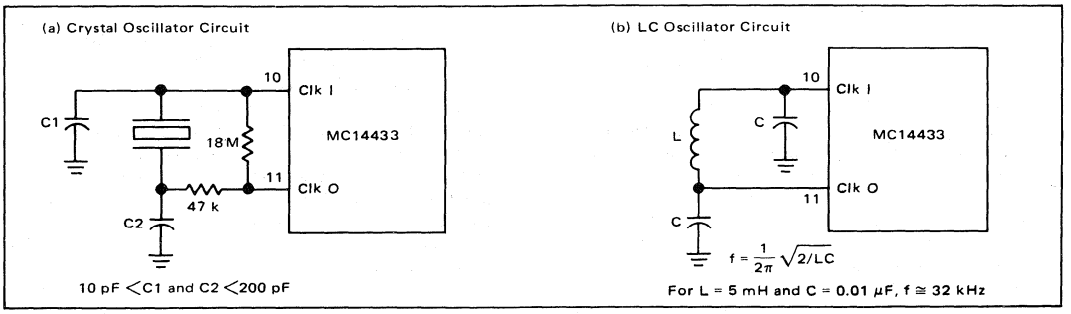


FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

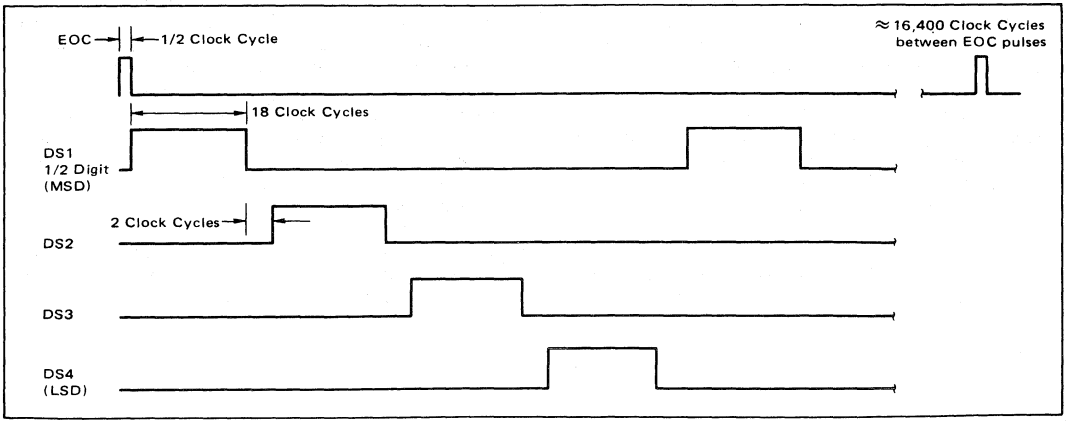


FIGURE 9 – INTEGRATOR WAVEFORMS AT PIN 6

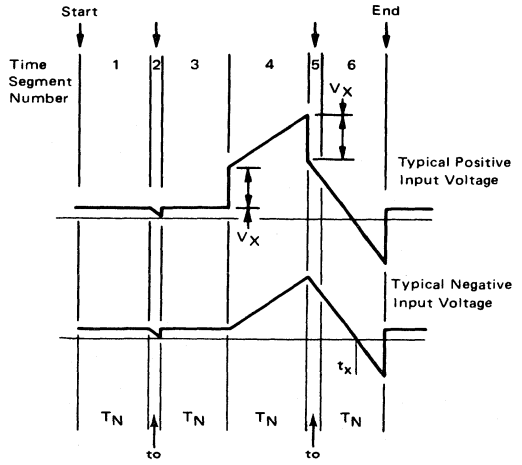
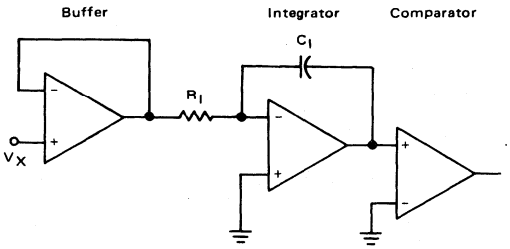


FIGURE 10 – EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 – The offset capacitor (C_0), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 – The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

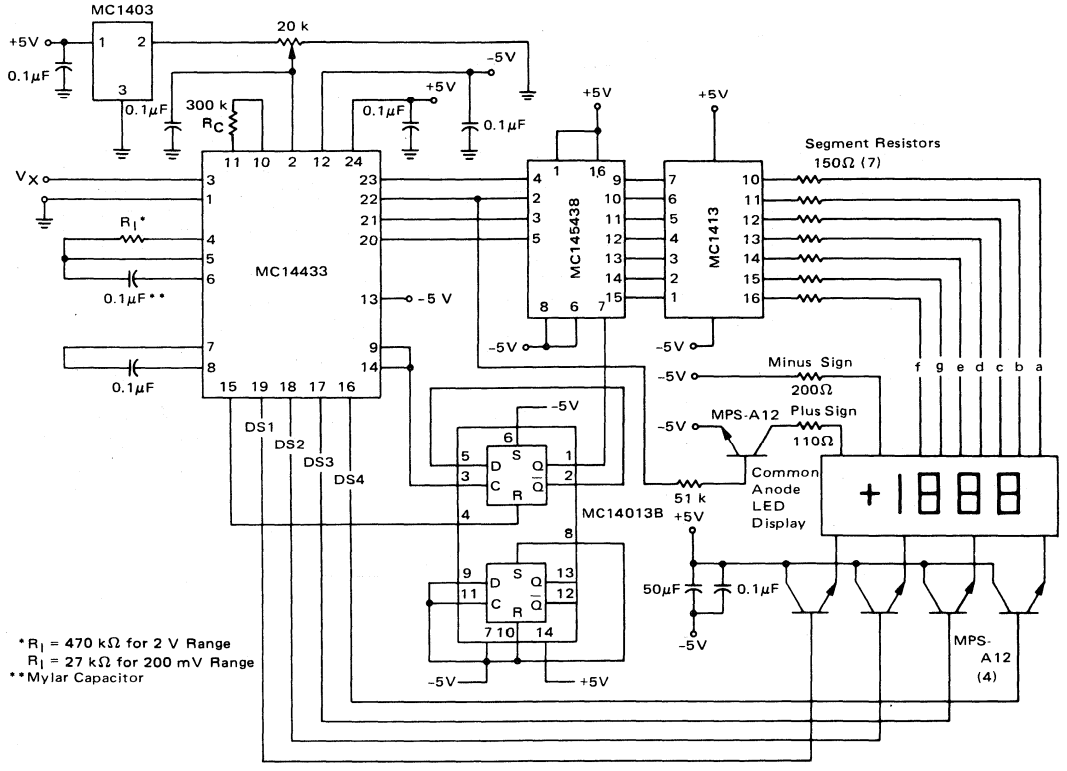
Segment 3 – This segment of the conversion cycle is the same as Segment 1.

Segment 4 – Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. This segment requires 4000 clock periods. Fig. 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 – This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 – This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 – 3-1/2 DIGIT VOLTMETER–COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

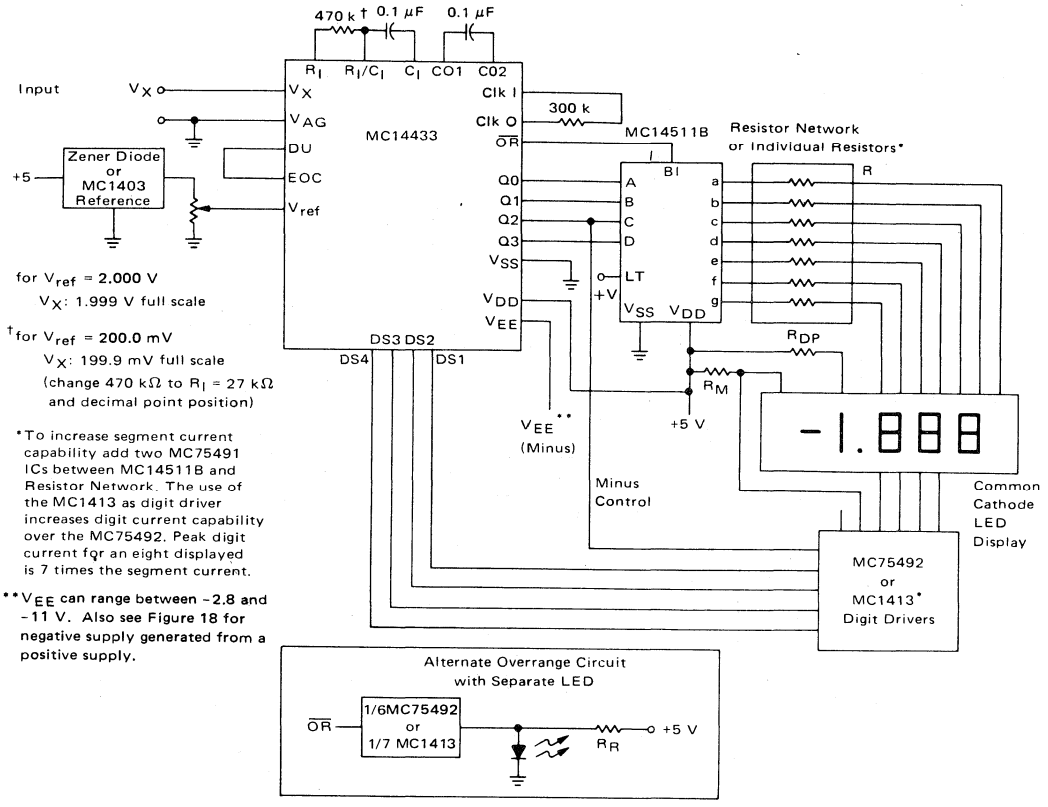
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and −5 V supplies is *not* required. See the recommended operating conditions and Figure 1, on pages 2 and 3.

FIGURE 12 – 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC75492 or MC1413 provides sink for digit current. (The MC75492 or MC1413 are devices with 6 or 7 darlingtons respectively with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC 75492 or MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

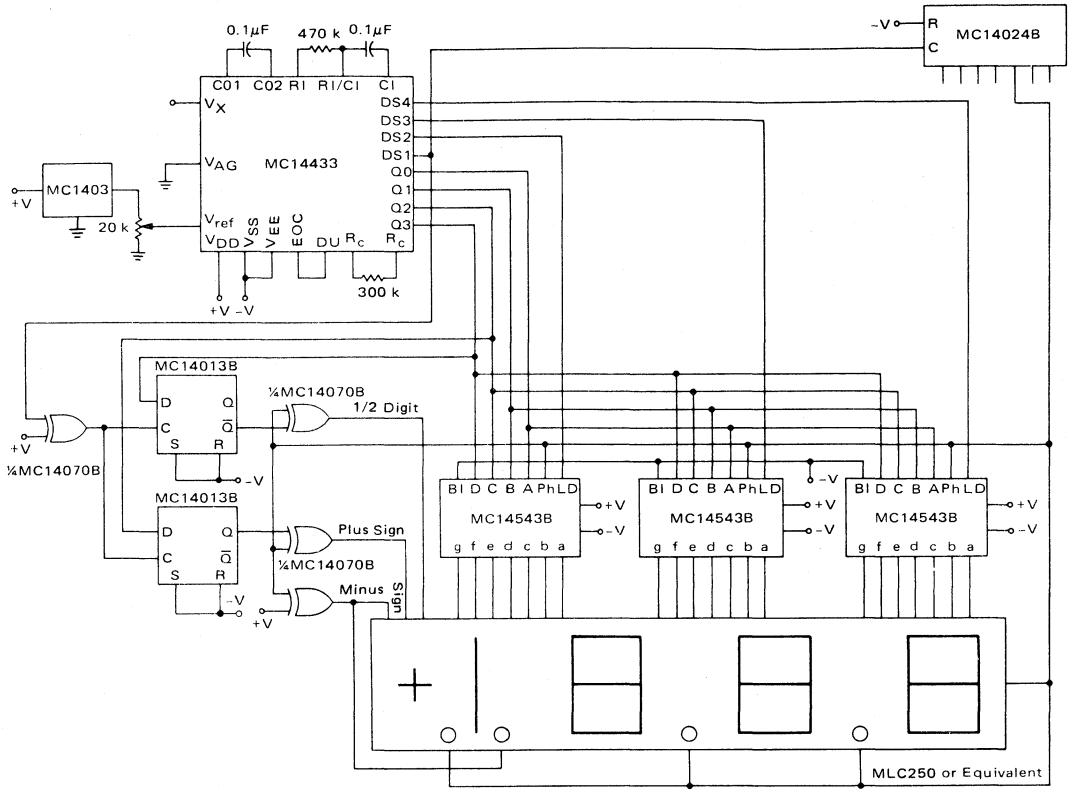
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown. There are leftover sections in either the MC75492 or MC1413.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of

FIGURE 13 – 3½ DIGIT VOLTMETER WITH LCD DISPLAY



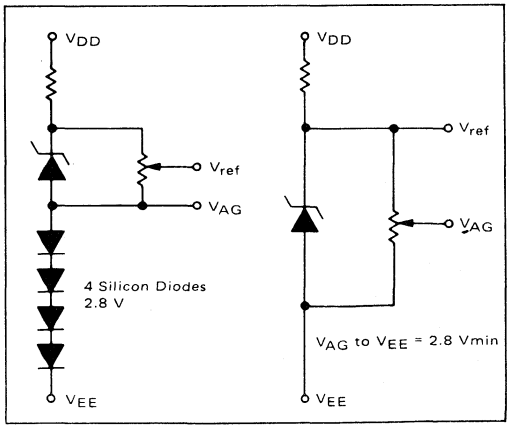
the LCD and to the individual segments through the combination of the output circuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 – TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



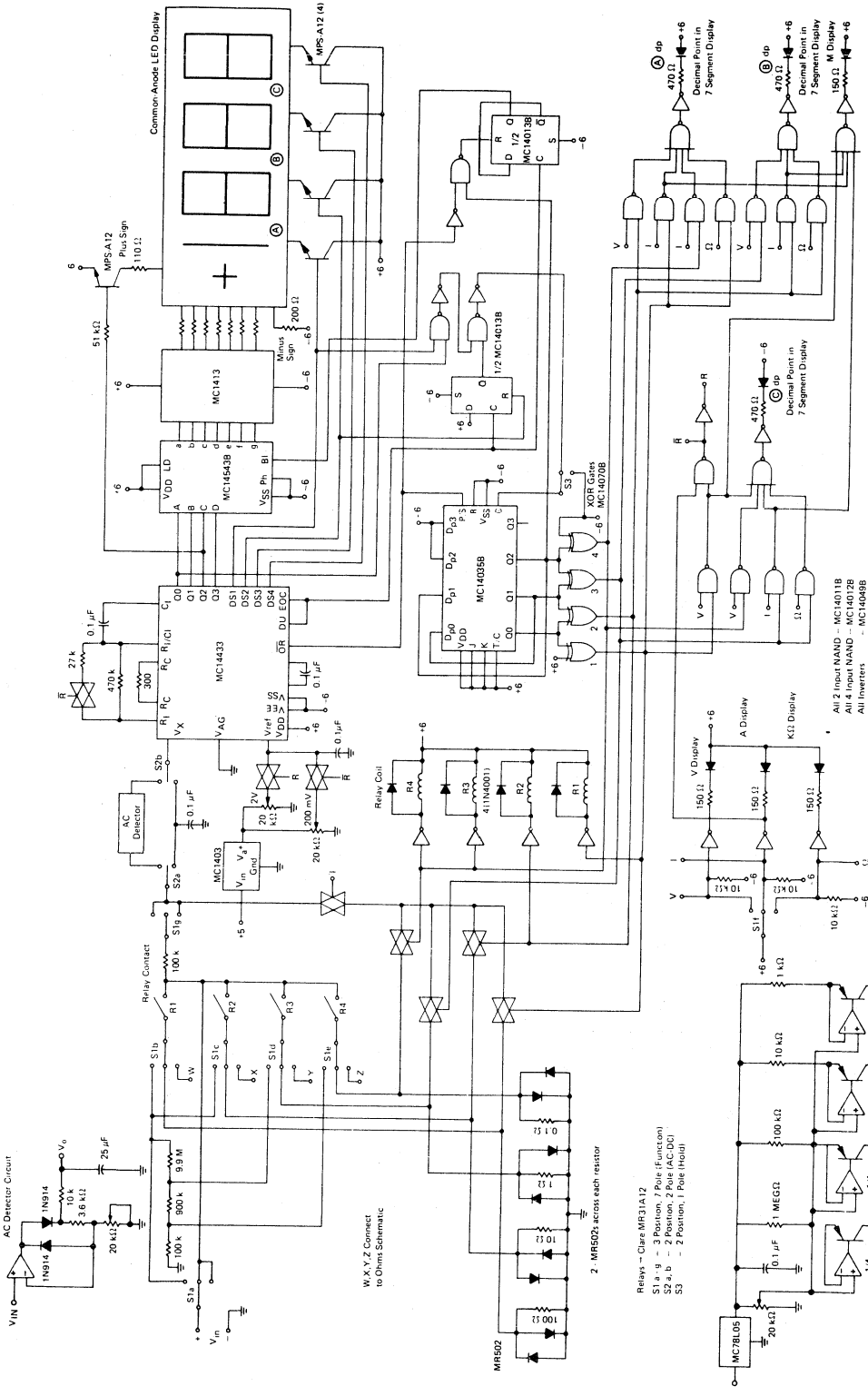


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER

3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."*

*Available January 1977.

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 – DEMULTIPLEXING FOR MC14433 BCD DATA

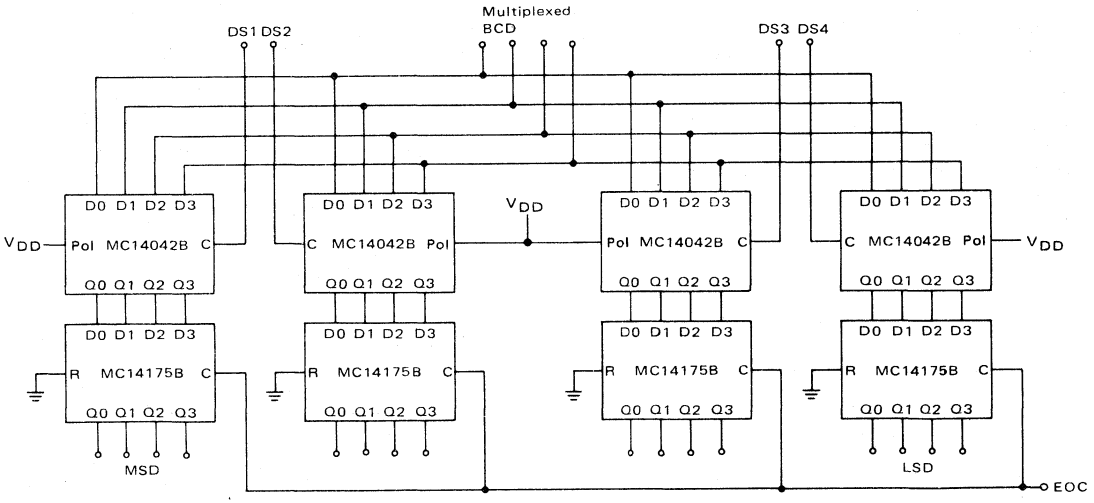
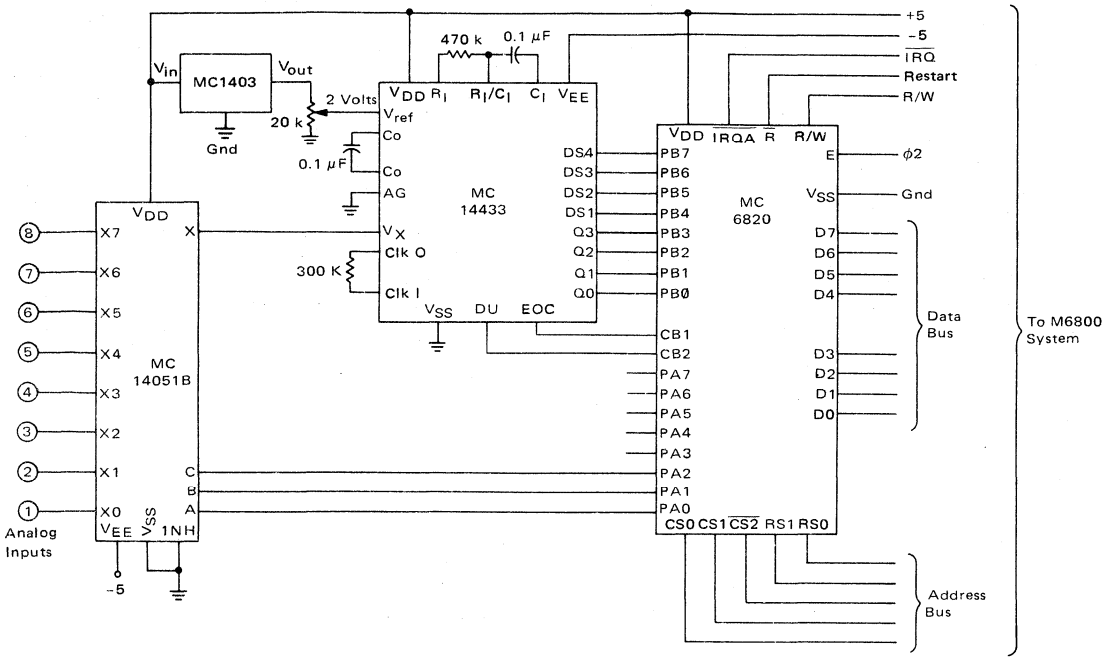


FIGURE 17 – CHANNEL DATA ACQUISITION HARDWARE



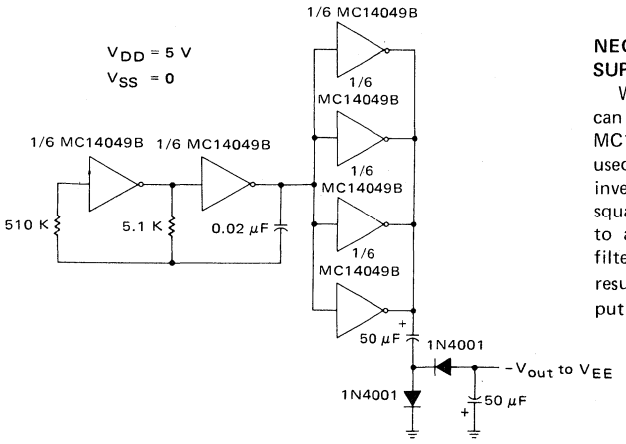
8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8 channel data acquisition network using the MC14433 and an M6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6820 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."*

*Available January 1977

FIGURE 18 – NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049B. Two inverters from CMOS hex inverter are used as an oscillator (≈ 3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a -4.3 V no load output voltage while the output with a 2 mA load is ≈ 3.4 V.

AUTOMOTIVE SPEED CONTROL PROCESSOR

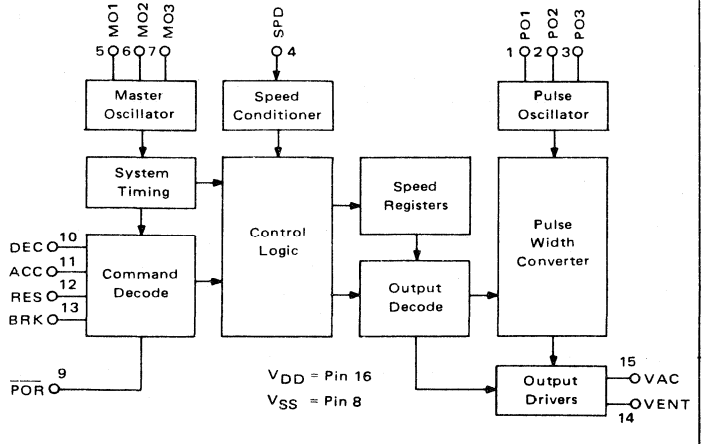
The MC14460 device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.

The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.

A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed.

- On-Chip Master Oscillator for System Time Reference
- Separate On-Chip Pulse Oscillator for Output Pulse Width Adjustment (Analogous to System Gain)
- Diode Protection on All Inputs
- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Buffered Outputs Compatible with Discrete Transistor Driver Interface
- Low Power Dissipation

BLOCK DIAGRAM



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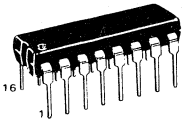
McMOS LSI

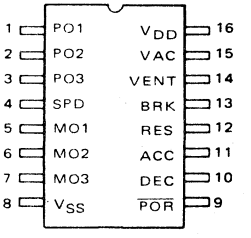
(LOW-POWER COMPLEMENTARY MOS)

AUTOMOTIVE SPEED CONTROL PROCESSOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Supply Voltage Pin 16	V_{DD}	–	4.0	5.0	6.0	Vdc
Output Voltage Pins 1, 2, 5, 6, 14, 15	V_{OL}	5.0	–	–	0.5	Vdc
	V_{OH}	5.0	4.5	–	–	Vdc
Input Voltage Pins 3, 7, 9, 10, 11, 12, 13	V_{IL}	–	–	–	0.3 V_{DD}	Vdc
	V_{IH}	–	0.7 V_{DD}	–	–	Vdc
Pin 4	V_{IL}	–	$\frac{V_{DD}}{2}$ -1.5	–	–	Vdc
	V_{IH}	–	–	–	$\frac{V_{DD}}{2}$ +1.5	Vdc
Input Hysteresis Pin 4 ($V_{IH} - V_{IL}$)	HYS	–	0.5	–	–	Vdc
Output Drive Current Pins 1, 2, 5, 6 V_{OH} = 4.6 Vdc	I_{OH}	5.0	-0.29	–	–	mAdc
V_{OL} = 0.4 Vdc	I_{OL}	5.0	+0.36	–	–	mAdc
Pins 14, 15 V_{OH} = 2.5 Vdc	I_{OH}	5.0	-2.0	–	–	mAdc
Input Current Pins 3, 4, 7, 10, 11, 12, 13 V_{IL} = 0.0 Vdc	I_{IL}	6.0	–	–	-1.0	μAdc
V_{OH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Pin 9 V_{IL} = 0.0 Vdc	I_{IL}	6.0	15	–	200	μAdc
V_{IH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Supply Current Pin 16 (Both Oscillators Active, VAC and VENT Outputs High)	I_{DD}	6.0	–	1.0	10	mAdc

FIGURE 1 – SYSTEM TIMING

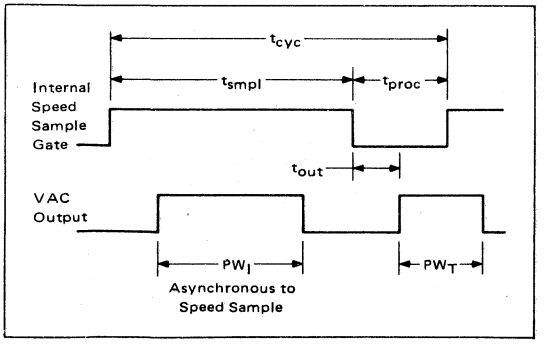
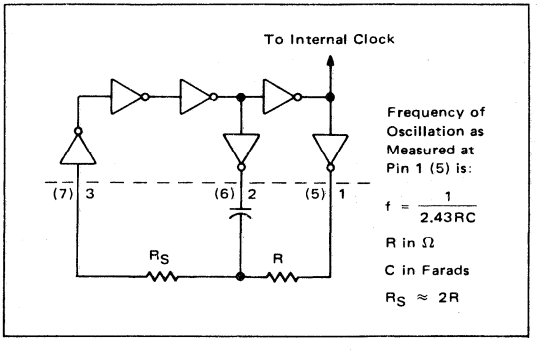


****FIGURE 2 – OSCILLATORS**



SWITCHING CHARACTERISTICS (T_A = 25°C, V_{DD} = 4–6 Vdc)

Characteristics	Symbol	Min	Typ	Max	Unit
ACCEL Input Hold Time	t_{ACC}	$16/f_M$	9.52*	–	ms
DECEL Input Hold Time	t_{DEC}	$16/f_M$	9.52*	–	ms
RESUME Input Hold Time	t_{RES}	1	–	–	μs
BRAKE Input Hold Time	t_{BRK}	1	–	–	μs
Master Oscillator Frequency** T_A = -40°C to +85°C, R_S = 100 kΩ R = 43 kΩ, C = 5600 pF Useful Range	f_M	 1596 1344	 1680 1680	 1764 2016	 Hz Hz
Pulse Oscillator Frequency** T_A = -40°C to +85°C, R_S = 100 kΩ R = 43 kΩ, C = 5600 pF Useful Range	f_P	 1596 400	 1680 1600	 1764 3200	 Hz Hz
Speed Input Frequency	f_S	–	–	300	Hz
Speed Sample Time ($1008/f_M$)	t_{smpl}	–	600*	–	ms
Speed Processing Time ($16/f_M$)	t_{proc}	–	8.9*	–	ms
System Cycle Time ($1024/f_M$)	t_{cyc}	–	608.9*	–	ms
Output Delay Time ($9/f_M$)	t_{out}	–	5.4*	–	ms
Output Pulse Width Initializations (≈$1/f_P$) Trim Outputs (≈$1/f_P$)	 PW_I PW_T	 280* 10*	 – –	 760* 80*	 ms ms

*f_M = 1680 Hz, f_P = 1600 Hz, f_S = 2.222 Hz/MPH

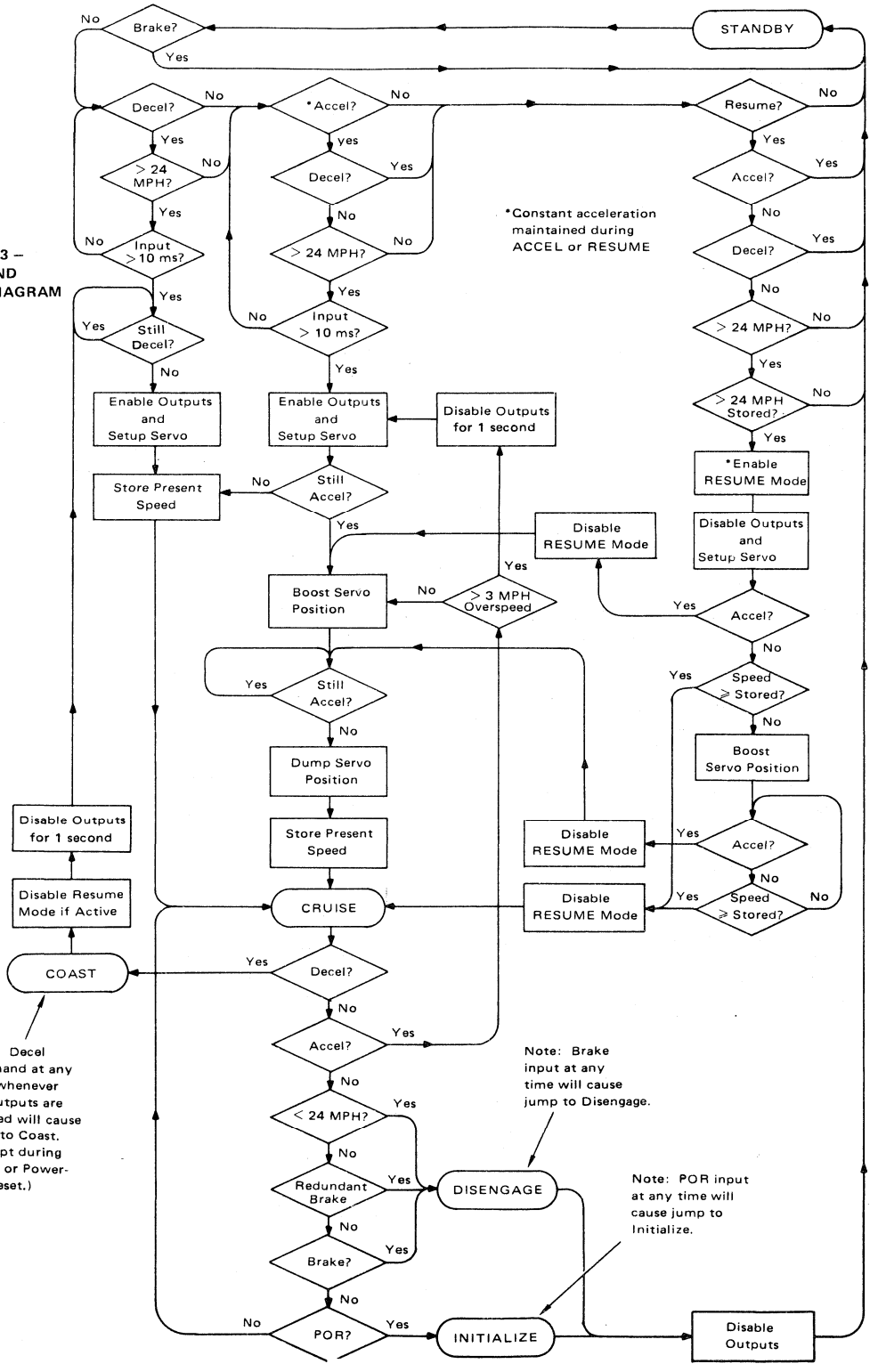
SYSTEM PERFORMANCE (T_A = 25°C, V_{DD} = 5 Vdc, f_M = 1680 Hz, f_S = 2.222 Hz/MPH)

Characteristic	Symbol	Typical	Unit
Speed Resolution ($f_M/2016\ f_S$)	S_{RES}	0.375	MPH
Minimum Operating Speed ($f_M/31.5\ f_S$)	S_{min}	24	MPH
Maximum Stored Speed ($f_M/8.4\ f_S$)	S_{max}	90	MPH
Controlled Acceleration Rate (ACCEL or RESUME Modes) $(f_M)^2/f_S$ (6.881) (10^5)	A	1.85	MPH/s
Redundant Brake Speed Drop Below Stored Reference Speed ($-f_M/63\ f_S$)	S_{RB}	-12	MPH
Speed Deviation Assumes Suitable Mechanical Hookup and Pulse Oscillator Frequency Adjusted to Suit Throttle Servo Requirements Level Road (no wind, ±1% grades) Transient Road Conditions (±10 MPH winds, ±7% grades)	 ΔS_N ΔS_T	 ±2 ±3	 MPH MPH
Stored Speed Accuracy Steady-State (Acceleration = 0) Transient (Acceleration = ± A MPH/s)	 RS_{SS} RS_T	 0.375 0.6 A	 MPH MPH

TRUTH TABLE

OUTPUT		
VAC	VENT	SERVO DRIVE
0	0	Decrease Speed
0	1	Hold Speed
1	0	Invalid Output
1	1	Increase Speed

FIGURE 3 – COMMAND FLOW DIAGRAM



DEVICE OPERATION

PULSE OSCILLATOR (PO1, PO2, PO3; Pins 1, 2, 3)

These pins are the output pins of the output Pulse Oscillator, which is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the relative pulse width of the VAC and VENT outputs.

SPEED (SPD, Pin 4)

This is the Speed input to be controlled or stored. This input is level sensitive with hysteresis to allow use of slowly changing waveforms. Input frequency should never exceed 1/3 the Master Oscillator frequency (f_M).

MASTER OSCILLATOR (MO1, MO2, MO3; Pins 5, 6, 7)

The Master Oscillator is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the master system timing.

POWER-ON RESET (POR, Pin 9)

This pin is the Power-On Reset input. As long as this input is LOW, the internal system is cleared and the VAC and VENT outputs are disabled. An internal pullup device will source 15–200 μAdc of current from this pin to allow capacitor charging for automatic power-on reset.

DECEL (DEC, Pin 10)

This is the DECEL command input. When held HIGH both VAC and VENT outputs will be LOW. When the DECEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

ACCEL (ACC, Pin 11)

This is the ACCEL command input. When held HIGH the VAC and VENT outputs will be modulated to maintain a fixed rate of acceleration. When the ACCEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

continued

THROTTLE SERVO

A. Two Coil Vacuum Powered

Truth Table:

VAC Coil	VENT Coil	Throttle Action
Off	Off	Release
Off	On	Hold
On	Off	Weak Pull
On	On	Pull

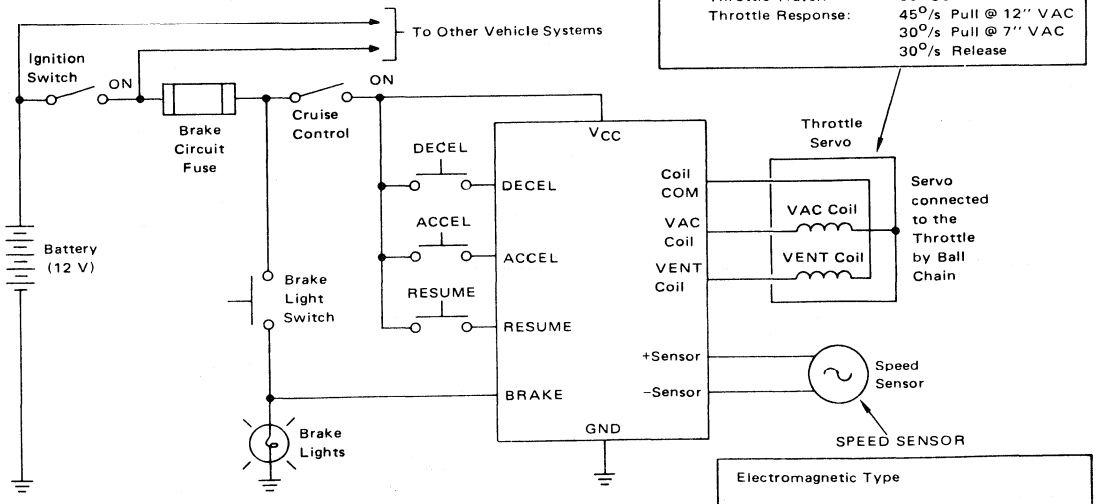
B. Coil Type

Coil Impedance: 80–90 Ω
Coil Inductance: 125–150 mH

C. Servo Response

Minimum Pulse Width: 5 ms
Throttle Travel: 50–60° full travel
Throttle Response: 45°/s Pull @ 12" VAC
30°/s Pull @ 7" VAC
30°/s Release

FIGURE 4 – TYPICAL AUTOMOTIVE CRUISE CONTROL APPLICATION



Electromagnetic Type

Poles: 8/revolution
Output Freq: 2.222 Hz/MPH (8000 pulses/mile)
Output Voltage: > 3.0 Vp-p @ 24 MPH
Maximum Freq: 360 Hz (162 MPH)
DC Resistance: < 40 Ω

DEVICE OPERATION continued

RESUME (RES, Pin 12)

This is the RESUME command input. When taken HIGH the system will lock into a mode where the VAC and VENT outputs are modulated to maintain a fixed rate acceleration. This acceleration ends when the SPD input sample matches the stored reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

BRAKE (BRK, Pin 13)

This is the BRAKE command input. When this input is taken HIGH the system is disabled (both VAC and VENT outputs LOW) until a DECEL, ACCEL, or RESUME command is received. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

VENT (Pin 14)

This is the VENT output. See Truth Table for operation.

VAC (Pin 15)

This is the VAC output. See Truth Table for operation.

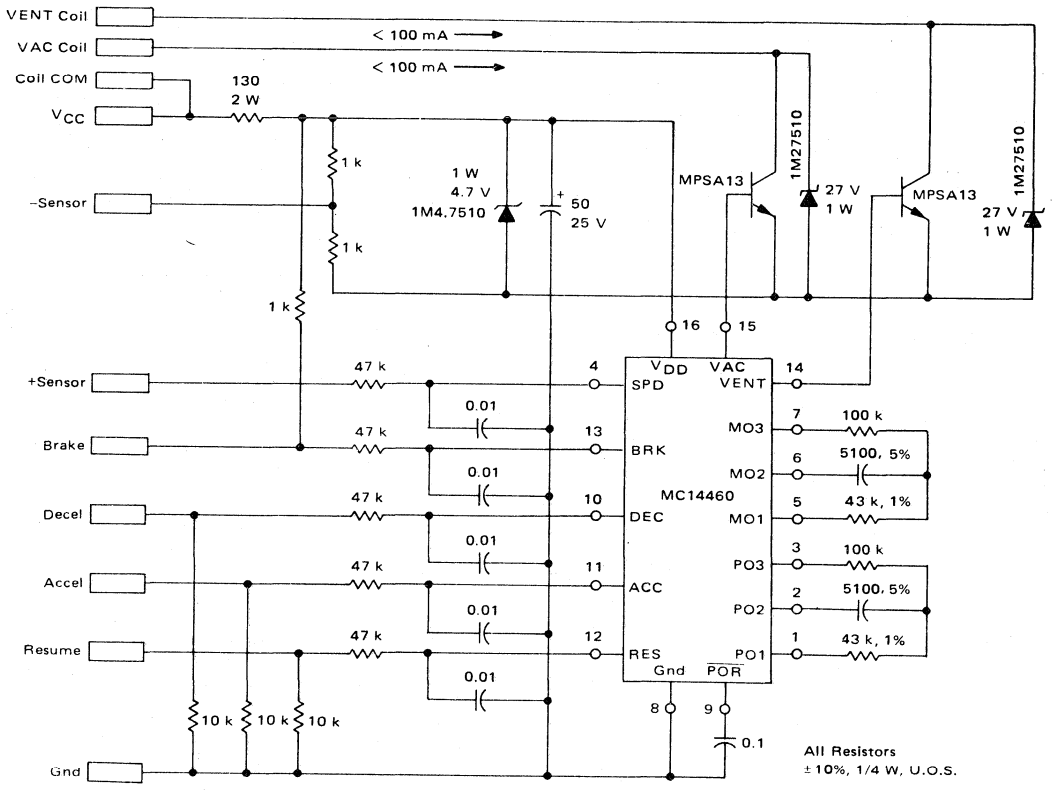
GROUND (V_{SS}, Pin 8)

Pin 8 is the ground connection for the package.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

Pin 16 is the power supply connection for the package.

FIGURE 5 – PC BOARD MODULE FOR CRUISE CONTROL



Environment

Ambient Temperature (T_A)	-40°C to 85°C
V_{CC} Operating Range	11–15 Vdc
V_{CC} Transients	9–16 Vdc
Load Dump	80 V Peak decaying to 12 V in < 200 ms
Inductive	±300 V Peak decaying in < 1 ms
Jump Start	+24 Vdc for 5 min.
Reverse Battery	-12 Vdc continuous

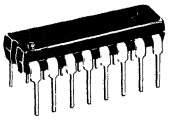
DIODE MATRIX ENCODER

The SAA 1006 provides a 16 line to 4-bit binary encoding for general purpose applications.

It is also suitable to be used in conjunction with the remote control receiver MC6525, MC6526, MC6527, MC6529 for local instruction encoding.

DIODE MATRIX ENCODER

SILICON MONOLITHIC INTEGRATED CIRCUIT



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CASE 648

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Forward Current per Pin	I_F	20	mAdc
Reverse Voltage all Pins	V_R	6,5	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C)

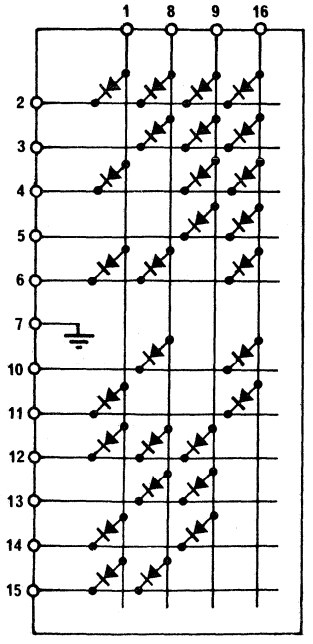
Characteristics	Symbol	Min.	Typ.	Max.	Unit
Reverse Current per Pin @ V_R = 6.0 V	I_R			30	μA
Forward Voltage Drop per Pin @ I_F = 2.0 mA	V_F			1	Volt

FUNCTIONAL TRUTH TABLE

		INPUT PINS[1]															
		2	3	4	5	6	10	11	16	12	13	14	9	15	8	1	all open
OUTPUT PINS	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	8	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	9	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	16	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

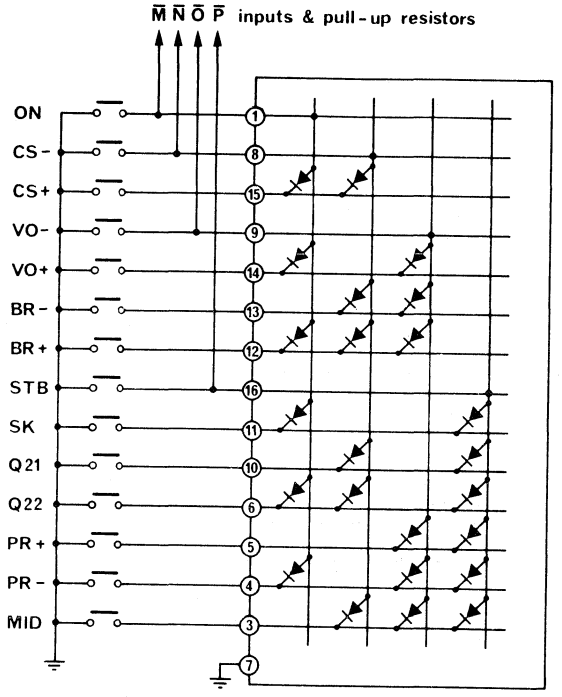
[1] One pin at a time to be grounded.

FIGURE 1 – PINOUT AND FUNCTIONAL SCHEMATIC

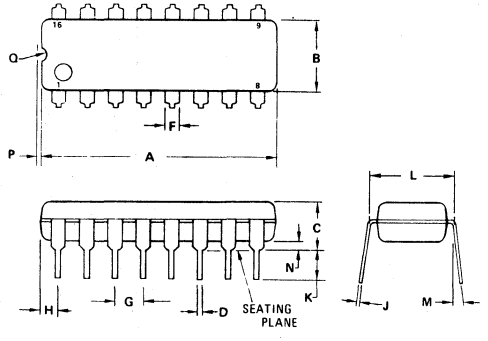


APPLICATION INFORMATION

When used in conjunction with the remote control receivers MC6525/6/7/9 it will encode the following commands.



PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

TBA120C
TBA120D*

FM IF AMPLIFIER, LIMITER AND DETECTOR

An integrated circuit specifically designed for use in the sound section of TV-receivers and the FM/IF portion of radio receivers.

The TBA 120 C is pin for pin and function compatible with the proelectron type TBA 120 S but includes an improved D.C. volume control, which makes "grouping" or selection unnecessary.

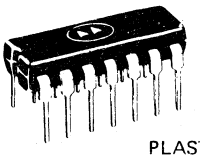
The TBA 120 D is pin for pin compatible with the proelectron type TBA 120, which is using external phase shift capacitors.

Features:

- Excellent 3dB limiting
- High A.M. rejection
- Wide supply voltage range
- Auxiliary zener diode & transistor
- Minimum number of external components required.

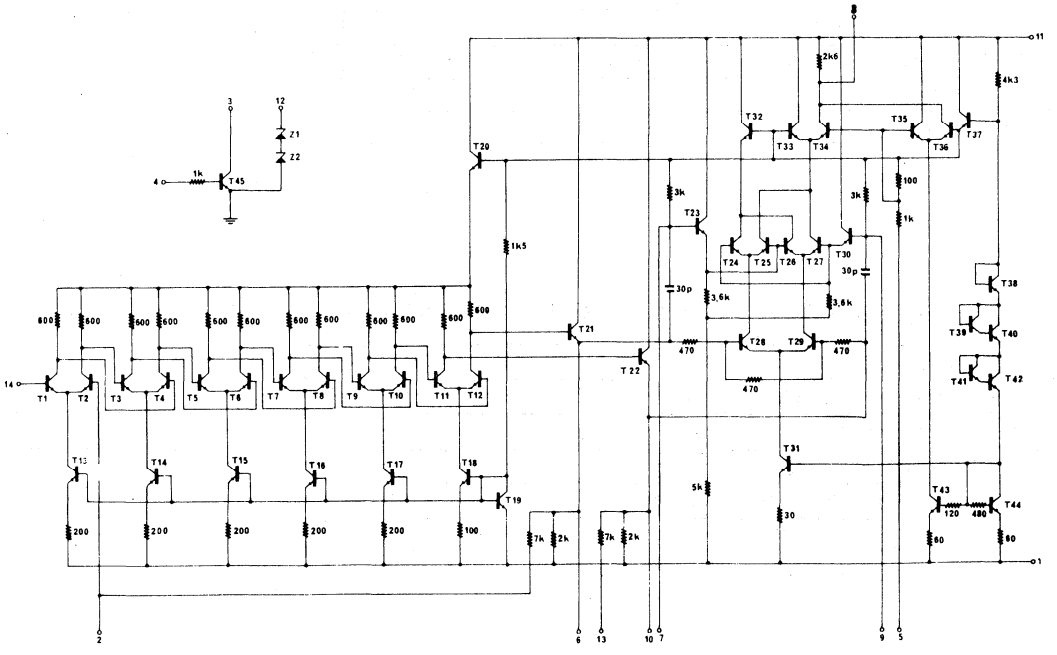
FM IF AMPLIFIER, LIMITER, FM DETECTOR AND AUDIO PREAMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646 TO-116

CIRCUIT SCHEMATIC



*TBA 120 D: Pins 6 and 10 are not connected internally otherwise same as TBA 120 C.

MAXIMUM RATINGS ($T_A = +25^oC$ unless other wise noted.)

Rating	Value	Unit
Power Supply Voltage	+ 18	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above $T_A = +25^oC$	 625 5.0	 mW $mW/^oC$
Operating Temperature Range	0 to + 75	^oC
Storage Temperature Range	−65 to + 150	^oC

ELECTRICAL CHARACTERISTICS: ($T_A = +25^o$, $V_{CC} = 12V$, $R^* = 20K$, Test circuit: FIG. 1)

Characteristic	Min	Typ	Max	Units
Supply Voltage Range	6	–	18	Volts
Supply Current	10	14	18	mA
Audio Output ($f_o = 5.5$ MHz, $\Delta f = 50$ KHz, $Q = 45$)		1		Volts R.M.S.
Audio Output ($f_o = 10.7$MHz, $\Delta f = 75$KHz, $Q = 35$)		.38		Volts R.M.S.
3dB Limiting ($f_o = 5.5$MHz, $\Delta f = 50$KHz, $Q = 45$)		30	60	μV R.M.S.
3dB Limiting ($f_o = 10.7$MHz, $\Delta f = 75$ KHz, $Q = 35$)		40		μV R.M.S.
A.M. Rejection ($f_o = 5.5$MHz, R.F. Input: 500 μV)	45			dB
A.M. Rejection ($f_o = 10.7$MHz, R.F. Input: 500 μV)	40			dB
Volume Control Range	65	75		dB
Output Impedance		2.6		KΩ

ELECTRICAL CHARACTERISTICS OF AUXILIARY Z DIODE AND TRANSISTOR T45 ($T_A = +25^o$)

Characteristic	Min	Typ	Max	Units
Z–Voltage @ 5 mA (Pin 12)	11.2		13.2	Volts
Z–Resistance (Pin 12) @ 1 KHz, 5 mA		15		Ω
T45 Breakdown Voltage V_{CEO}	13			Volts
T45 Current Gain @ $I_C = 1$ mA, $V_{CE} = 5$ V	40	100		–

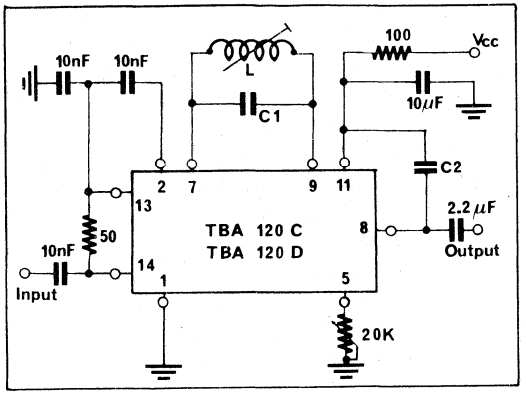


FIGURE 1 – TEST CIRCUIT

COMPONENT VALUES:

	L	C_1	Q
5.5MHz	.55μH	1.5nF	45
6MHz	.55μH	1.2nF	45
10.7MHz	2.2μH	100pF	35

C2 = 22nF, together with the integrated resistor of 2.6KΩ (PIN 8) gives the deemphasis and can be reduced if required. For stereo 470pF should be used to provide H.F. decoupling.

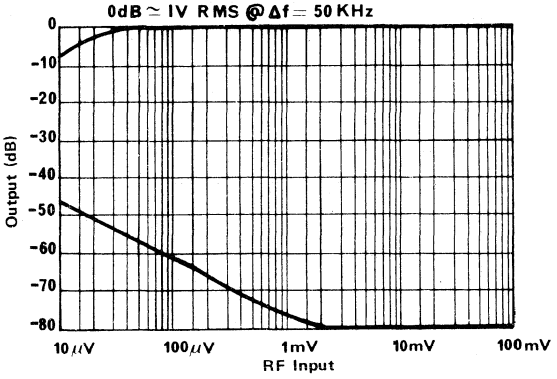


FIGURE 2 – AUDIO OUTPUT AND S/N VERSUS INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz

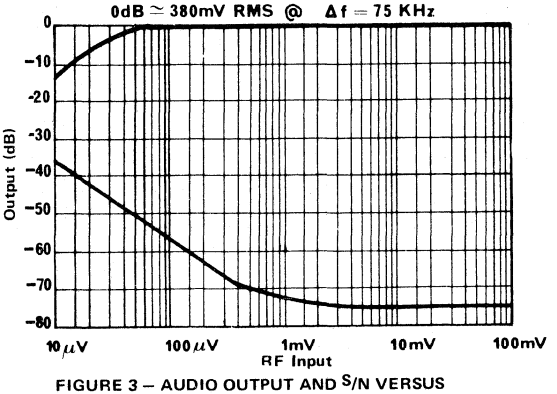


FIGURE 3 – AUDIO OUTPUT AND S/N VERSUS INPUT SIGNAL LEVEL AT 10.7 MHz

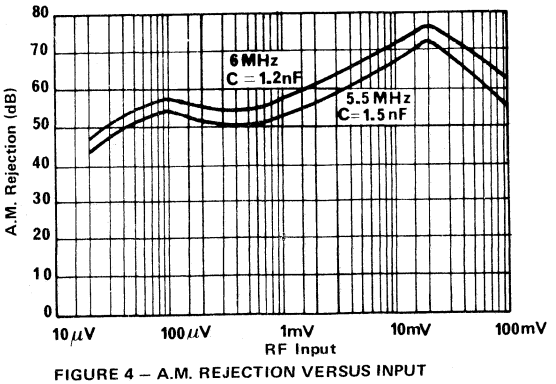


FIGURE 4 – A.M. REJECTION VERSUS INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz (30% A.M., 50 KHz F.M.)

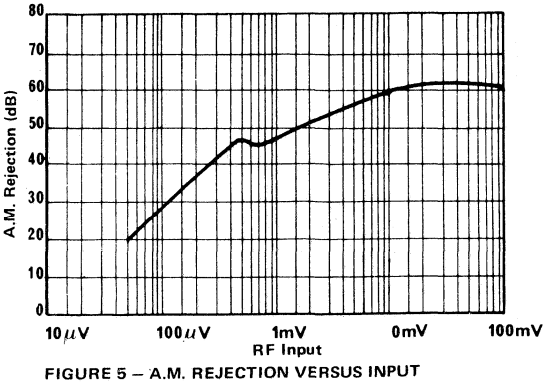


FIGURE 5 – A.M. REJECTION VERSUS INPUT SIGNAL LEVEL AT 10.7MHz (30 o/o A.M., 75KHz FM)

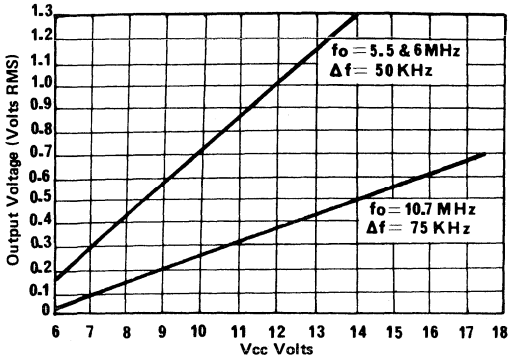


FIGURE 6 – OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

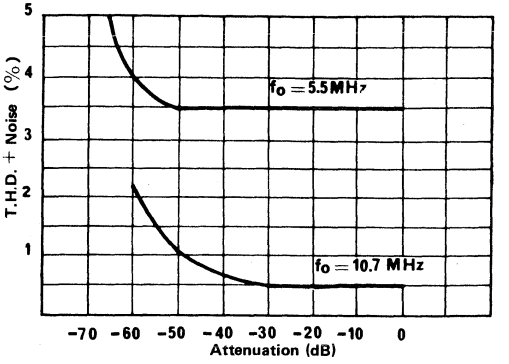


FIGURE 7 – T.H.D. + NOISE VERSUS ATTENUATION (D.C. VOLUME CONTROL)

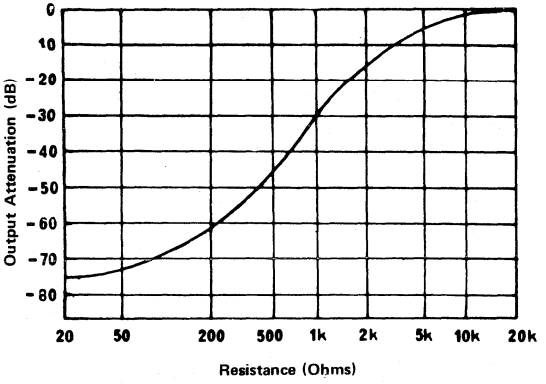


FIGURE 8 – OUTPUT SIGNAL ATTENUATION VERSUS VOLUME CONTROL RESISTANCE

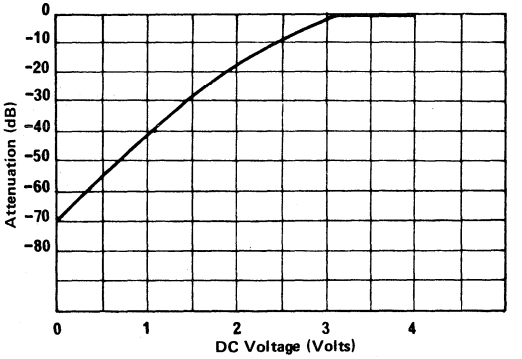


FIGURE 9 – OUTPUT SIGNAL ATTENUATION VERSUS D.C. VOLTAGE AT PIN 5.

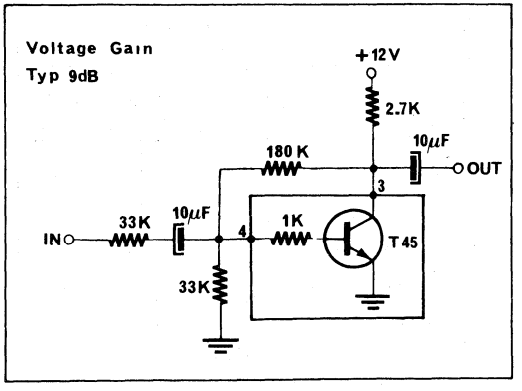


FIGURE 10 – AUDIO PREAMPLIFIER TEST CIRCUIT

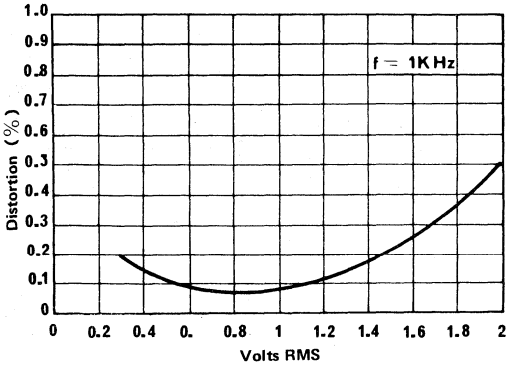


FIGURE 11 – T.H.D. VERSUS OUTPUT VOLTAGE FOR AUDIO PREAMPLIFIER SHOWN IN FIGURE 10.

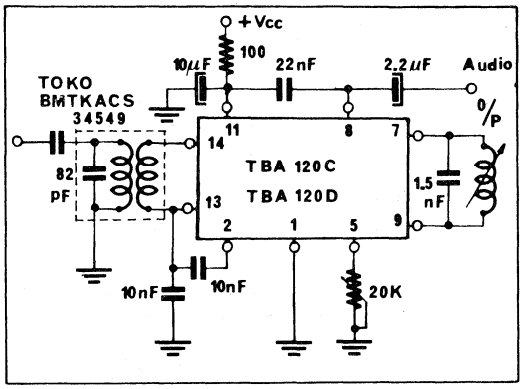


FIGURE 12 – TYPICAL APPLICATION FOR 5.5MHz WITH L-C INPUT FILTER

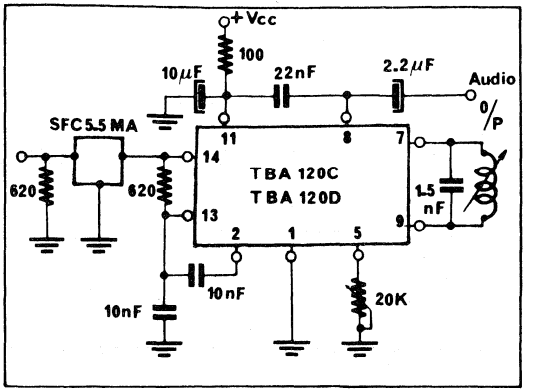


FIGURE 13 – TYPICAL APPLICATION FOR 5.5MHz WITH CERAMIC INPUT FILTER

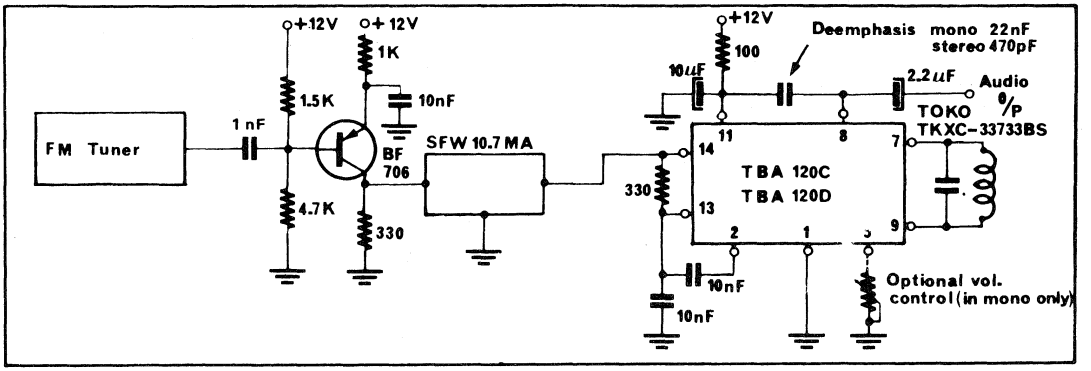
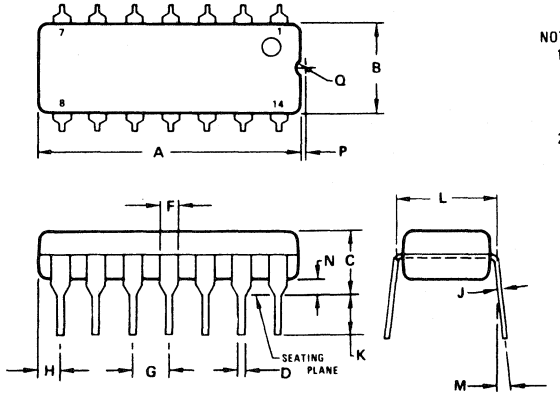


FIGURE 14 – TYPICAL APPLICATION FOR 10.7MHz WITH CERAMIC FILTER

OUTLINE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

TBA120U

FM IF AMPLIFIER, LIMITER AND DETECTOR

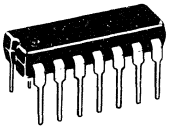
Specially designed for use in the sound section of the most advanced TV receivers.

FEATURES

- Additional audio input and constant audio output for connection of VTR or headphones
- No selection of volume control potentiometer is necessary
- Wide supply voltage range for constant audio output
- Excellent signal to noise ratio

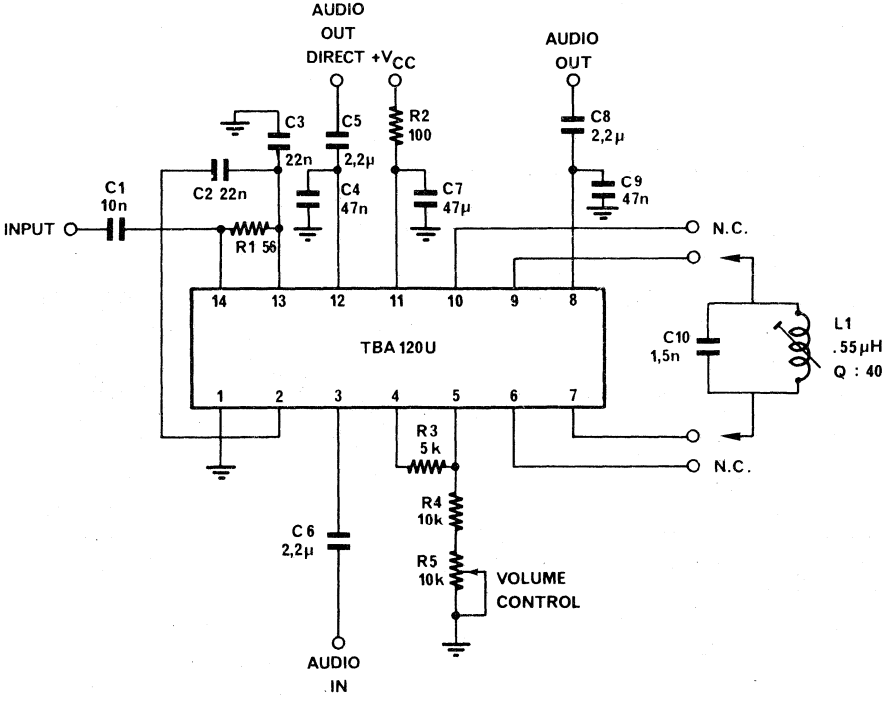
FM IF AMPLIFIER
LIMITER, FM DETECTOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646 (TO-116)

FIGURE 1 – TBA120U TEST CIRCUIT



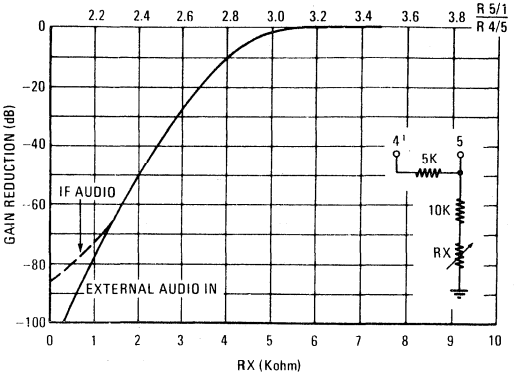
MAXIMUM RATINGS (T_A = +25 °C unless other wise noted)

Value	Value	Unit
Power Supply Voltage	18	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25 °C	 1200 10	 mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C, Test circuit: Fig. 1)

Characteristic	Min.	Typ.	Max.	Unit
Supply Voltage Range	9.5	12	18	Volts
Supply Current		14		mA
Audio Output (f_o = 5.5 MHz, Δf = 40 KHz,) pin 8 pin 12		1 0.9		Volts R.M.S.
3dB Limiting (f_o = 5.5 MHz, Δf = 40 KHz)		40		μV R.M.S.
A.M. Rejection (f_o = 5.5 MHz, R.F. Input: 500 μV)		55		dB
Volume Gain Reduction for $R_{4\text{-}5}$ = 5.0 KΩ, $R_{5\text{-}1}$ = 13 KΩ	20	28	36	dB
Volume Control Range		83		dB
Output Impedance (pins 8 and 12)		1.2		KΩ
THD (f_o = 5.5 MHz, RF input: 10 mV, Δf = 40 KHz)		1.7		%
S/N (f_o = 5.5 MHz, RF input: 10 mV, Δf = 40 KHz)		87		dB

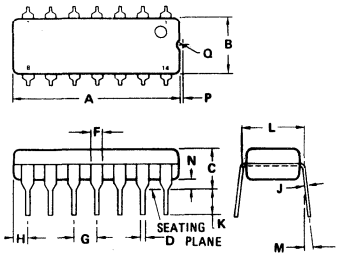
FIGURE 2 – VOLUME CONTROL CURVE



[1] Pin 4 nominally at 4.8 Vdc.

OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 646



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

TBA395

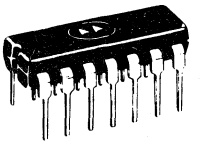
CHROMINANCE COMBINATION

A Silicon integrated circuit for use in PAL television receivers.

- internal supply line stabilization
- 20 dB A.C.C. range
- low external component count
- designed to be used in conjunction with TBA 396 and TBA 327/MC1327

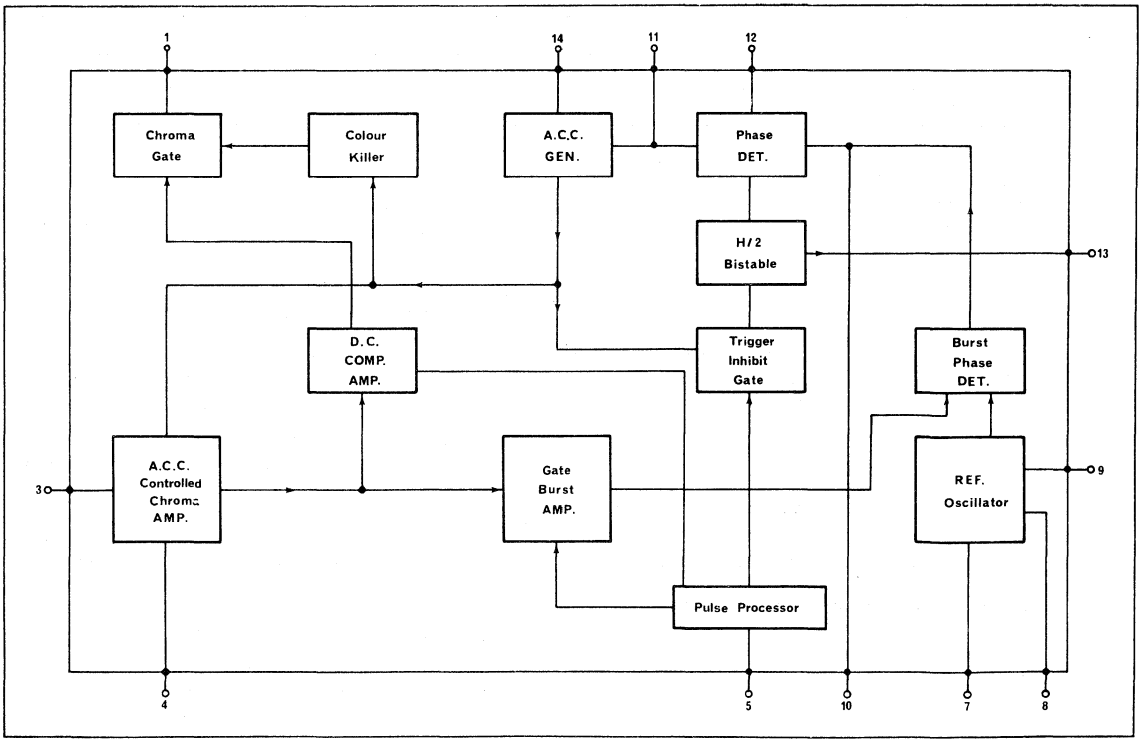
CHROMINANCE COMBINATION

MONOLITHIC SILICON INTEGRATED CIRCUIT



P. SUFFIX PLASTIC PACKAGE
CASE 646 TO–116

SYSTEM BLOCK DIAGRAM



MAXIMUM RATINGS ($T_A = +25^oC$ unless otherwise stated)

Rating	Pin	Value	Unit
Power Supply Current	2	60	mA
D.C. Current Capability of Reference Output	9	4.0	mA
Chrominance Input Voltage	3	1.2	V p.t.p.
Operating Temperature Range		0 to + 70	^oC
Power Dissipation (Package Limitation) Derate above $T_A = +25^oC$		625 5.0	mW mW/^oC
Storage Temperature Range		− 65 to +150	^oC

ELECTRICAL CHARACTERISTICS ($T_A = +25^oC$ unless Otherwise Stated)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	2	7.5	8.4	9.5	V d.c.
Forward Transconductance (Chrominance Output Load = 560 Ω) (f_{IN} = 4.43 MHz)	3–1	6.4			mmho
Chrominance Input Resistance	3	2.0			KΩ
Reference Oscillator Pull-in Range		±250			Hz
Reference Output	9	400	700		mV
H/2 Bistable Output	13	1.3			V p.t.p.
Burst Gate Operating Voltage	5	2.0		5.0	V
Chrominance Output D.C. Current 1. Colour killer operating 2. Colour killer off		 200		 4.0	 μA μA

APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 (8.4 volt circuit supply point) must be decoupled closely to pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.

2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.

3. The connection from pin 1 (chroma output) should be also as short as possible to prevent capacitive loading of the 1K8Ω output resistor.

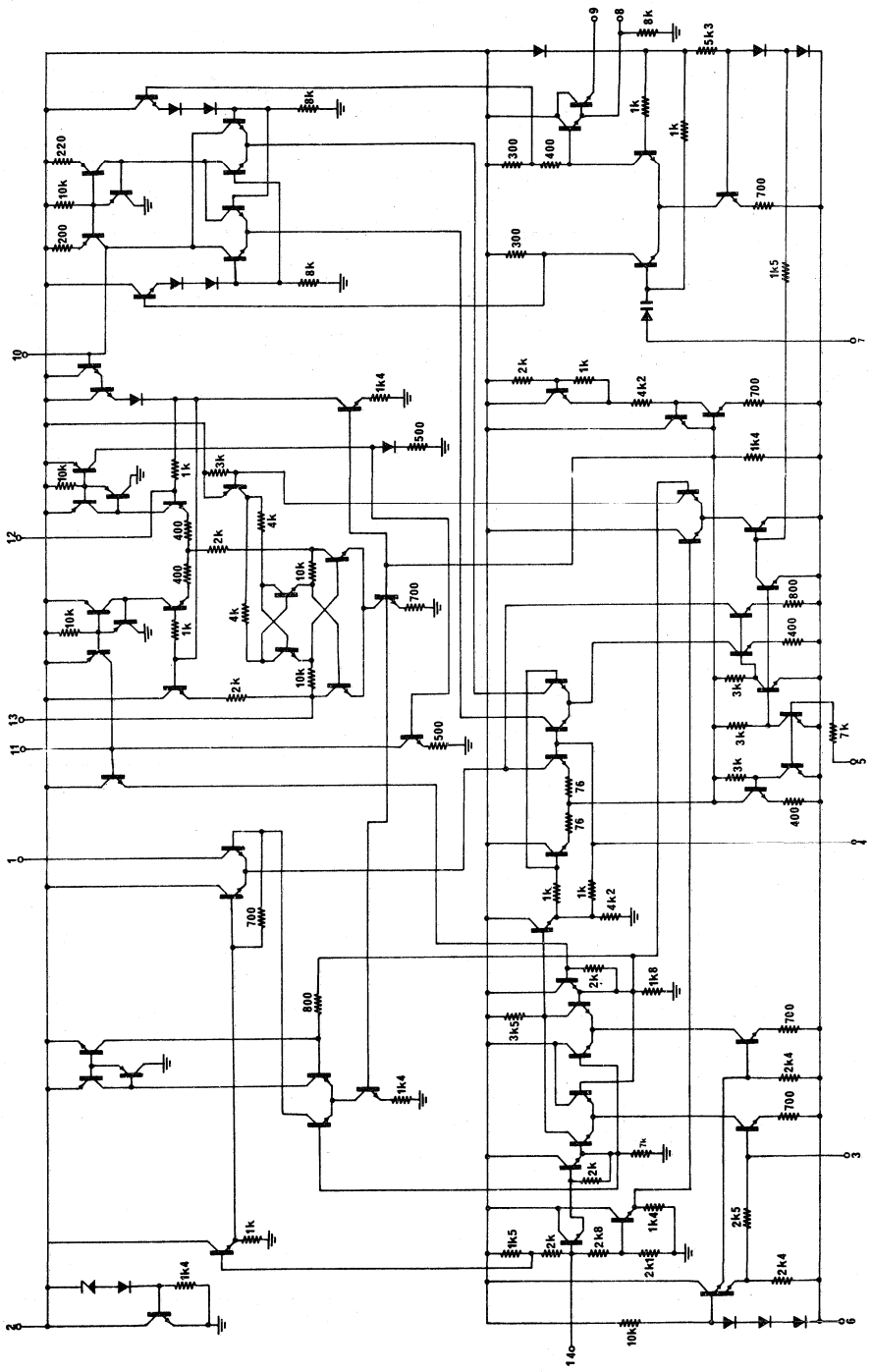
SETTING–UP NOTES

For subcarrier oscillator adjustment the chrominance input must be bypassed to ground via a 1 nf capacitor. The Acc potentiometer is then set to 1.2 volts below pin 2 voltage using a high input impedance oscilloscope or Voltmeter (>10MΩ). While the adjustment is made burst gate pulses must be applied to pin 5.

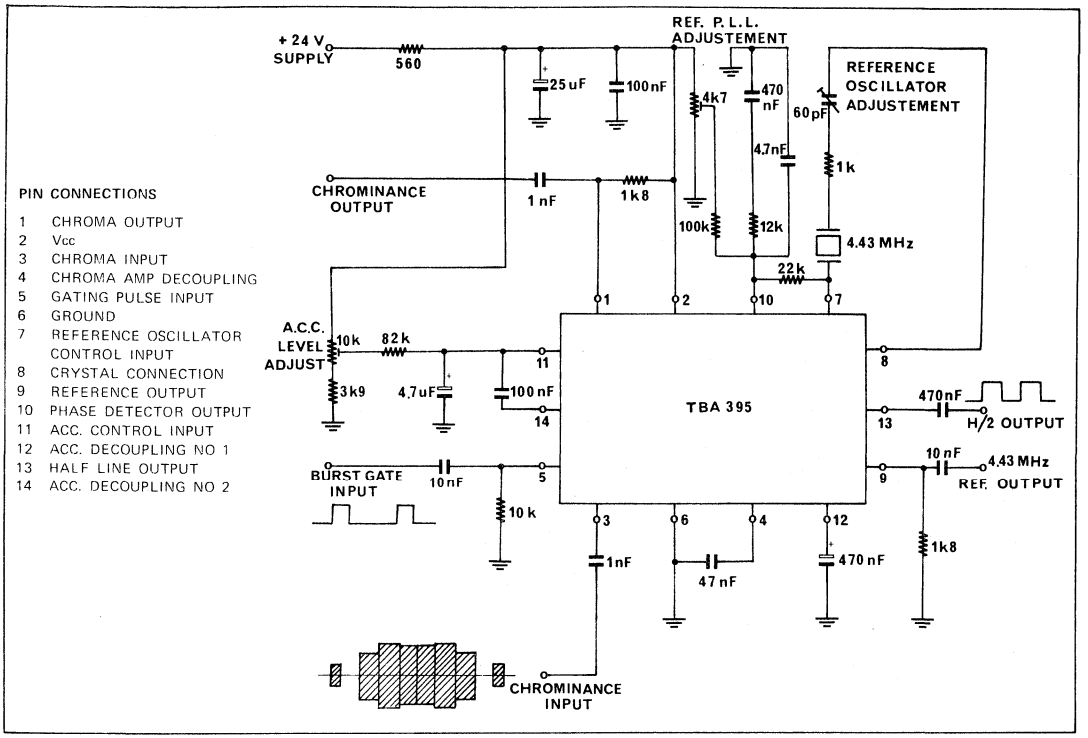
The oscillator free-running frequency can then be adjusted to sub-carrier value ±10 Hz. The loop will lock if a chrominance signal is re-connected.

With a peak to peak signal of 250 mV (100^o/o bars) the output on pin 1 should be adjusted to 400 mV peak to peak using the A.C.C. control potentiometer.

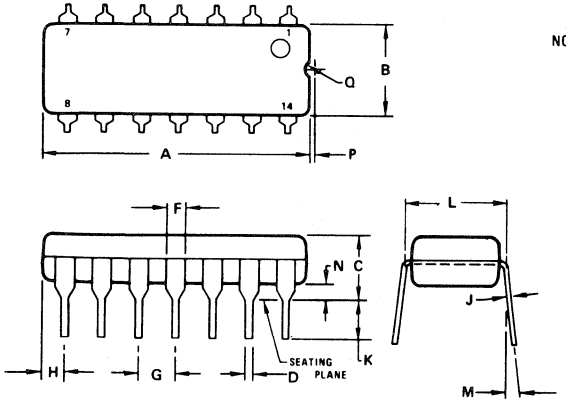
CIRCUIT SCHEMATIC



TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

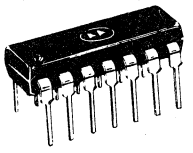
LUMINANCE CHROMINANCE COMBINATION

A Silicon Integrated circuit designed for use in PAL television receivers.

- dc control of brightness, contrast & saturation
- tracking of saturation with contrast control changes
- beam current limiting
- black level clamping
- designed to be used in conjunction with TBA395, TDA3950 & MC1327

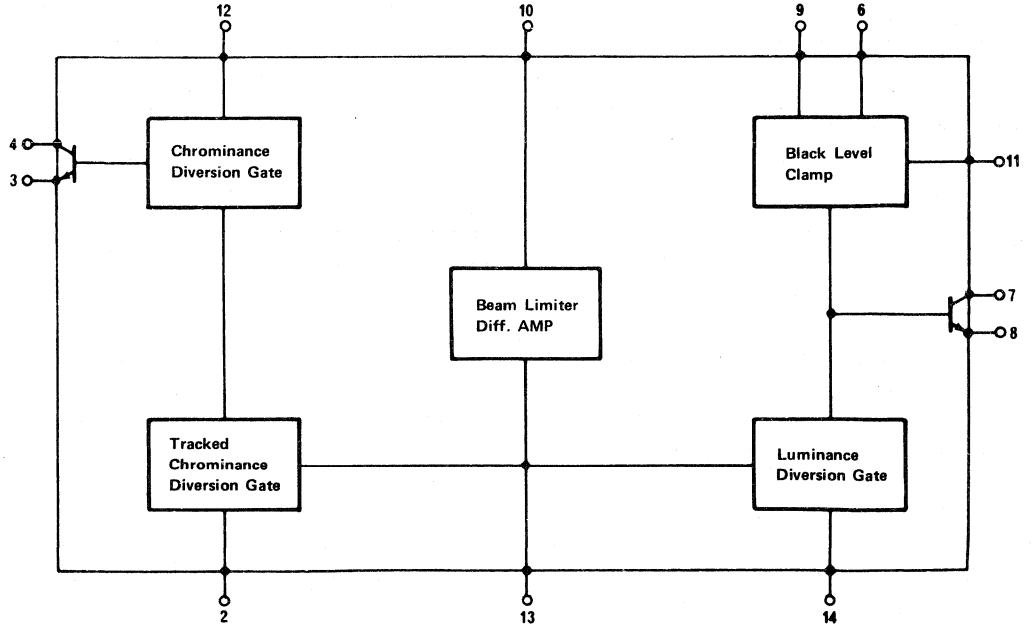
LUMINANCE AND CHROMINANCE CONTROL COMBINATION

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX PLASTIC
PACKAGE CASE 646 TO-116

FIGURE 1 – SYSTEM BLOCK DIAGRAM



MAXIMUM RATINGS ($T_A = +\ 25^oC$ unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	5	20	V d.c.
Luminance Output Collector Voltage	7	30	V d.c.
Luminance Output Emitter Current	8	7.0	mA
Chrominance Output Emitter Current	3	5.0	mA
Operating Temperature Range		0 to + 70	^oC
Power Dissipation (Package Limitation) Derate above $T_A = -\ 25^oC$		625 5.0	mW mW/^oC
Storage Temperature Range		−65 to + 150	^oC

ELECTRICAL CHARACTERISTICS (T_A=+25^{o}C Unless Otherwise Stated)

Characteristic	Pin	Min	Typ	Max	Unit
Luminance Input Resistance	14	100			K Ω
Luminance gain	14-8	0.6	1.0	1.2	
Change of black level with contrast and signal changes (black to white 4 μS gating)				3.0	$^o/_o$
Black level clamp gating pulse	11	50		1000	μA
Contrast control range		35			dB
Saturation control range		35			dB
3dB luminance bandwidth (resistive load)	14-8		7.5		MHz
Video input aperture	14	1.4		3.4	V.p.t.p.
Chrominance input resistance	2	5.0			K Ω
Chrominance voltage gain (Resistive load)	2-3	2.5	3.8	5.0	
Chrominance phase shift with saturation control				± 3	$^o/_o$
Chrominance phase shift with contrast control				± 3	$^o/_o$
Chrominance/Luminance tracking error with contrast control				± 2	dB
Threshold of beam limiter	10	1.8	2.0	2.2	V

APPLICATION NOTES

1. The d.c. controls are relatively insensitive to interference if the decoupling associated with these lines is close to the I.C.

2. Good decoupling is required close to the "cold" end of the PAL delay line driving coil to prevent spurious subcarrier components reaching the I.C. supply line.

SETTING UP NOTES

The pre-set brilliance control must be adjusted to give the correct black level of − 16.5 V at pin 7. If the color demodulator IC MC1327 is used to complete the system a voltage of − 7.5 V at the chroma outputs can be set using the same procedure.

This operation must be performed with the brilliance control at the centre of its range.

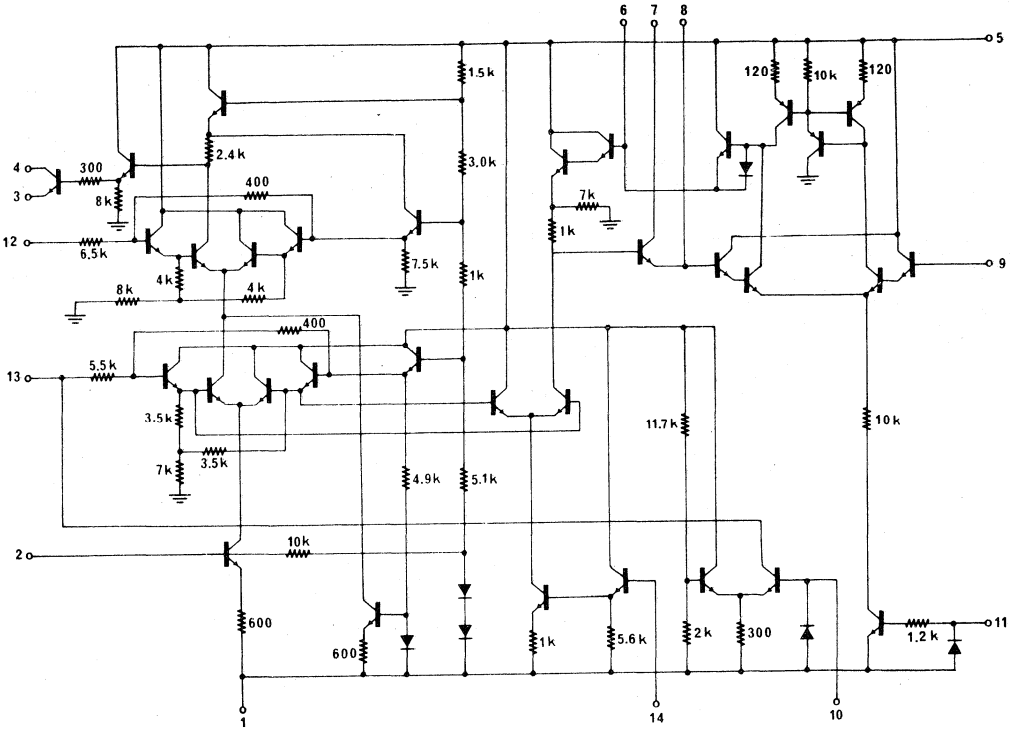
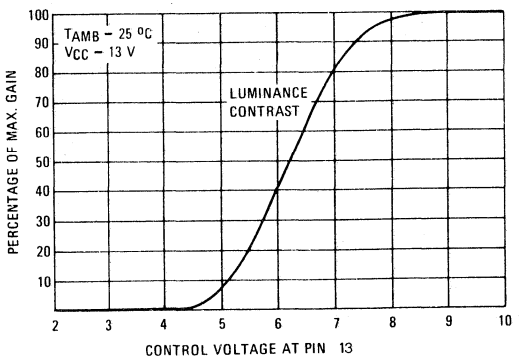


FIGURE 2 – CIRCUIT SCHEMATIC

FIGURE 3 – TYPICAL CONTROL VOLTAGE/GAIN CURVES



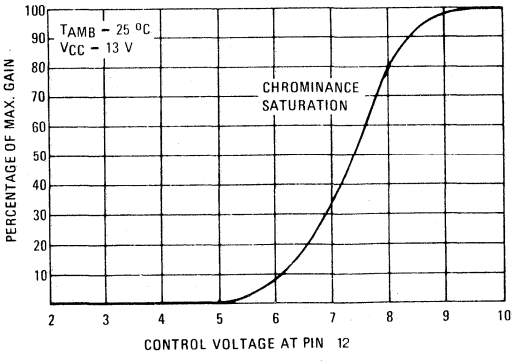
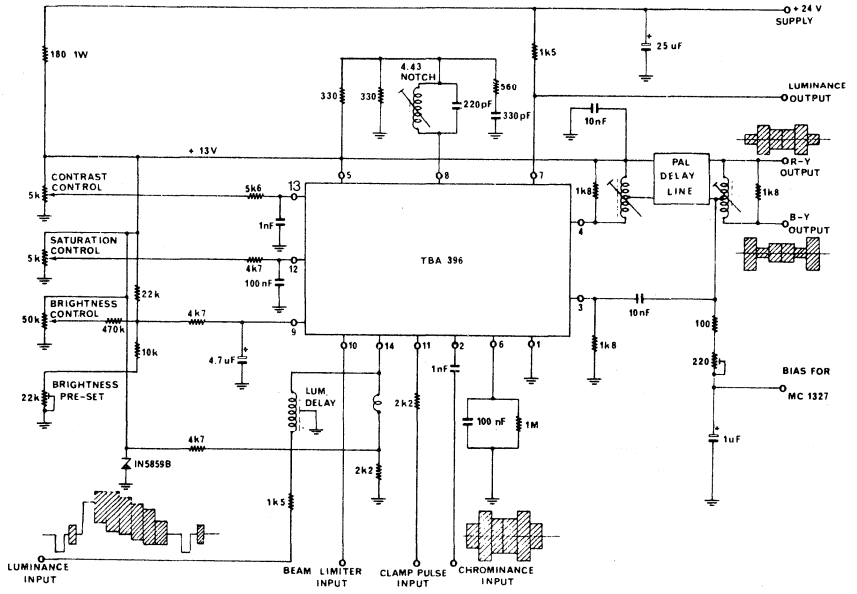


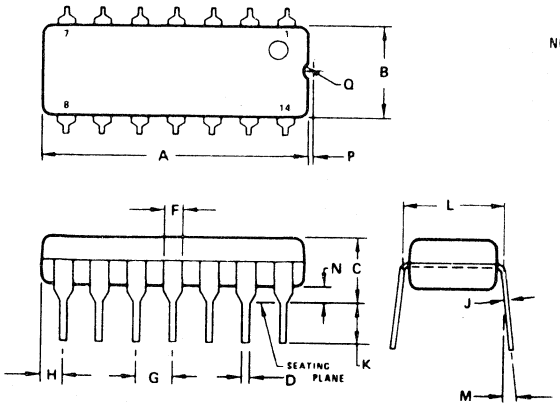
FIGURE 4 – TYPICAL CIRCUIT CONFIGURATION

PIN CONNECTIONS

1 GROUND
2 CHROMA INPUT
3 CHROMA OUTPUT EMITTER
4 CHROMA OUTPUT COLLECTOR
5 Vcc
6 CLAMP TIME CONSTANT
7 LUMINANCE OUTPUT COLLECTOR
8 LUMINANCE OUTPUT EMITTER
9 D.C. BRIGHTNESS CONTROL
10 BEAM LIMITER INPUT
11 BLACK LEVEL CLAMP GATE INPUT
12 D.C. SATURATION CONTROL
13 D.C. CONTRAST CONTROL
14 LUMINANCE INPUT



OUTLINE DIMENSIONS



NOTES:
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2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

TBA920
TBA920S

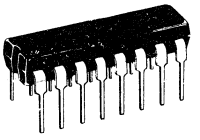
HORIZONTAL COMBINATION

The TBA920 is a line oscillator combination integrated circuit for use in television receivers with transistor or thyristor output stages. It combines the following features:

- Line oscillator
- Noise gated sync separator
- Phase comparison between flyback pulse and oscillator
- Loop gain and time constant switching (also for VCR applications)
- Output stage to drive a variety of line output stages

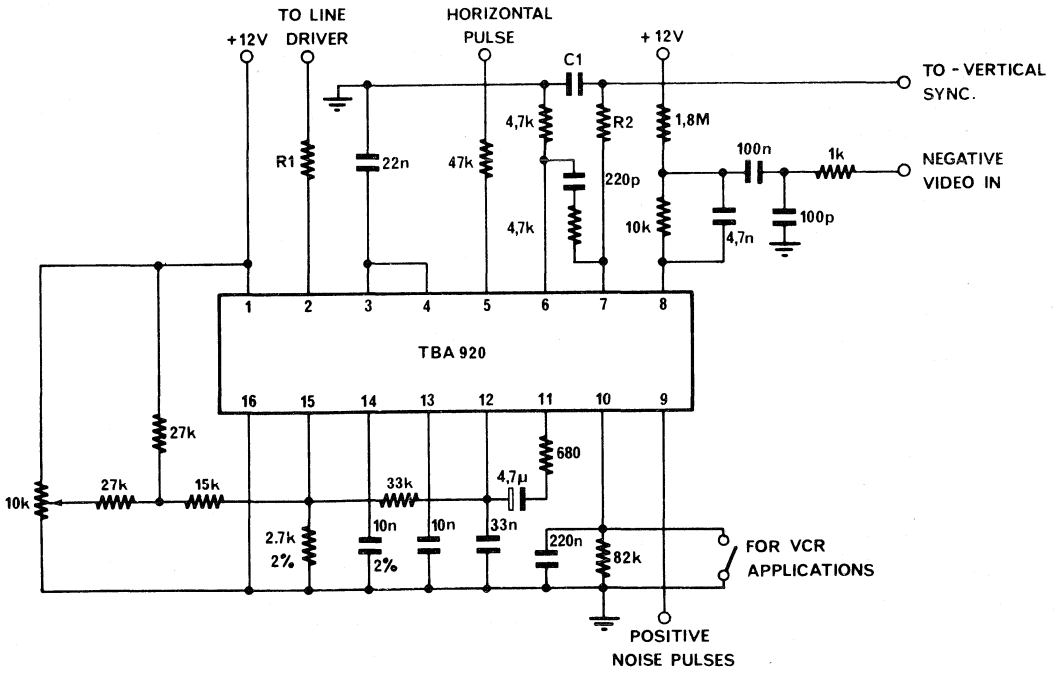
HORIZONTAL COMBINATION

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25 °C unless otherwise stated)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	13.2	Vdc
Power Dissipation Derate Above T_A = +25 °C	P_D	1.2 10	W mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

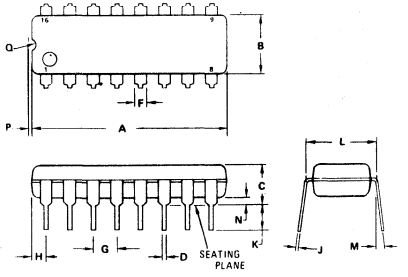
Characteristic	Pin	Symbol	Min.	Typ.	Max.	Unit
Power Supply Operating Voltage	1	V_{CC}	10.8	12	13.2	Vdc
Current Consumption	1	I_{CC}		24		mAdc
Input Signals:						
– Video (Positive going sync)	Fig. 1			3		Vp/p
– Noise Gating	9	V_9	0.7			Vp/p
– Flyback Pulse	5	V_5		±1		Vp/p
Pulse Duration @ 15.625 KHz	5	t_5	10			µsec
Output Signals:						
– Driver Pulse Amplitude	2	Vo		10		Vp/p
Output Current Average	2	Io			20	mA
Peak					200	mA
– Composite Sync Pulses	7	V_7		10		Vp/p
Oscillator:						
– Free Running Frequency	Fig. 1	fo		15625		H_z
– Frequency Spread (TBA920)		$\frac{\Delta fo}{fo}$			±5	%
(TBA920S)					±1.5	%
– Frequency Change, V_{CC} = 5.0 V		$\frac{\Delta fo}{fo}$			5	%
– Frequency Control Sensitivity		$\frac{\Delta fo}{\Delta I\ 15}$		16.5		Hz/µA
– Adjustment Range	Fig. 1			±10		%
– Influence of Supply Voltage Variations @ V_{CC} = 12 V on frequency		$\frac{\delta\ fo/fo}{\delta\ V_{CC}/V_{CC}}$			5	%
Control Loop 1:						
– Control Voltage Range	12	V_{12}	0.5		5.8	V
– Control Current						
$V_{10} > 4.4$ V, $V_6 > 1.5$ V	12	I_{12}		±2		mA p/p
$V_{10} < 2$ V, $V_6 > 1.5$ V				±6		mA p/p
– Loop Gain of APC System						
Coincidence between sync.		$\frac{\Delta t}{\Delta t}$		1		KHz/µsec
and Flyback or $V_{10} > 4.5$ V						
No coincidence or $V_{10} < 2$ V				3		KHz/µsec
– Catching and Holding Range		Δf		±1		KHz

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

Characteristic	Pin	Symbol	Min.	Typ.	Max.	Unit
Control Loop 2						
– Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse.		td	0		15	µsec
– Static Control Error		$\frac{\Delta t}{\Delta tol}$			0.5	%
– Output Current at Flyback		I_4		±0.7		mA
Phase Relations						
– Phase relation between leading edge of sync pulse and middle of flyback pulse		t		4.9[1]		µsec
– Tolerance of Phase Relation (TBA920) (TBA 920S)		t			0.7 0.4	µsec µsec
– Voltage for T_2 = 12 to 32 µsec	3	V_3	6		8	V
– Adjustment Sensitivity	3			10		µsec/V
– Input Current	3	I_3			2	µA

[1] With leading edge syncronization as shown in circuit diagram Fig. 1

PACKAGE DIMENSIONS



PLASTIC PACKAGE
CASE 648

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

TCA4500A

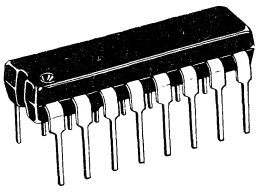
ADVANCE INFORMATION

FM STEREO DEMODULATOR DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

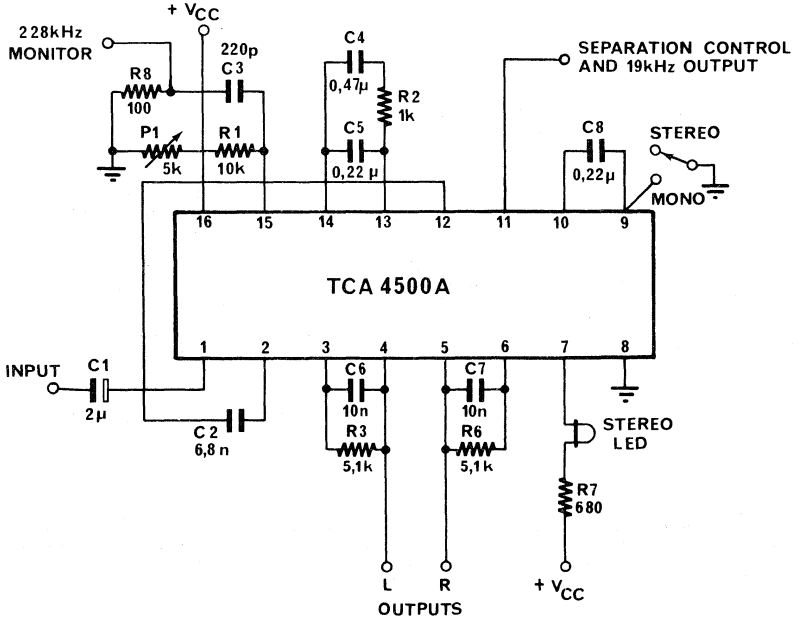
- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 KHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 KHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

FM STEREO DEMODULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648



PIN FUNCTIONS

1 – Input
2 – Preamplifier output
3 – Left amplifier input
4 – Left channel output
5 – Right channel output
6 – Right amplifier input
7 – Stereo indicator Lamp
8 – Ground
9 – Stereo switch filter
10 – Stereo switch filter
11 – 19 KHz output/blend
12 – Modulator input
13 – Loop filter
14 – Loop filter
15 – Oscillator RC network
16 – V_{CC}

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Power Dissipation (Package limitation) Derate above T_A = +25 °C	1800 15	mW mW/°C
Operating Temperature Range (Ambient)	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Lamp Drive Voltage (Max. voltage at pin 7 with lamp "off")	30	Volts
Lamp Current	100	mA
Blend Control Input Voltage (pin 11)	10	Volts

ELECTRICAL CHARACTERISTICS Unless otherwise noted: V_{CC} = +12 Vdc, T_A = 25 °C, 2.5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 KHz and with 10% pilot level, using circuit of Figure 1.

Characteristic	Min.	Typ.	Max.	Unit
Stereo Channel Separation: Unadjusted Optimised on other channel[1]	30 40			dB dB
Monaural Voltage Gain[1]	0.8	1	1.2	
THD at 2.5 V-pp Composite Input Signal at 1.5 V-pp Composite Input Signal		 0.2	0.3	% %
Signal/Noise Ratio DIN45405 Quasi Peak Reading RMS 20 Hz – 15 KHz		85 90		dB dB
Ultrasonic Frequency Rejection 19 KHz 38 KHz		31 50		dB dB
Stereo Switch Level (19 KHz input level for lamp "on") Hysterises	12	16 6	20	mVrms dB
Quiescent Output Voltage Change with Mono/Stereo Switching		5	20	mVdc
Stereo Blend Control Voltage (pin 11) 3 dB Separation (see Fig. 2) 30 dB Separation		0.7 1.7		V V
Minimum Separation (pin 11 at 0 V)			1	dB
Monaural Channel Imbalance (pilot tone off)			0.3	dB
ARI 57 KHz Pilot Tone Influence on THD[2]			0.5	%
Sub-carrier Harmonic Rejection 76 KHz 114 KHz 152 KHz		45 50 50		dB dB dB
Supply Ripple Rejection		50		dB
Input Impedance		50		KΩ
Output Impedance		100		Ω
Blend Control Current[1]			−300	μA
Capture Range		±5		%
Operating Supply Voltage	8		16	V
Current Drain (lamp off)		35		mA

Notes: [1] See Applications Information and Circuit Description
[2] ARI Test – Input signal: 1.5 Vp-p standard composite signal, 1 KHz modulation added to a CW 50 mVrms signal at 57.3 KHz.

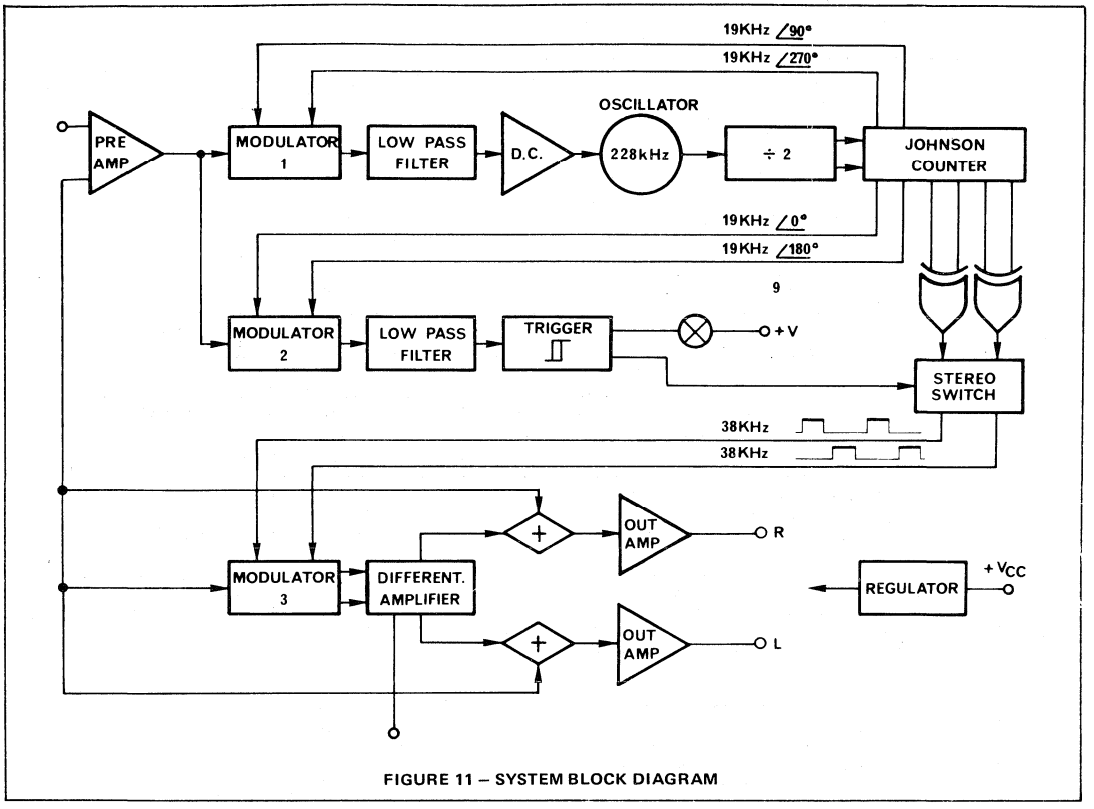


FIGURE 11 – SYSTEM BLOCK DIAGRAM

CIRCUIT DESCRIPTION

INTRODUCTION – The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 KHz pilot tone is absent.

The elimination of sensitivity to the third harmonic of the sub-carrier (114 KHz) excludes interference from the side-bands of adjacent transmitters, while the elimination of sensitivity to the third harmonic of the pilot tone (57 KHz) excludes interference from the ARI* system which employs this frequency.

* Auto Radio Informationen.

CIRCUIT OPERATION – The block diagram of the circuit, shown in Fig. 11, consists of three sections, the phase-lock-loop, including the digital waveform generator, the stereo switch, and the decoder, in which the composite stereo signal is demodualted and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 KHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 KHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in Fig. 12, which are used to drive the various modulators in the circuit, are developed.

The use of such drive waveforms produces the modulating functions also shown in Fig. 12. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency

translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 KHz tones of the ARI system. The TCA4500A is inherently free from these effects.

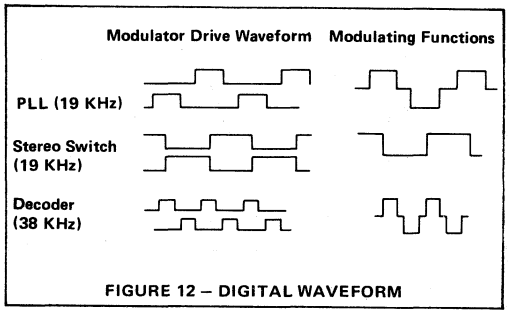


FIGURE 12 – DIGITAL WAVEFORM

The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 12) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is disactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

APPLICATION INFORMATION

GAIN AND DE-EMPHASIS – The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R_3 C_6 R_4 C_7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 KΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 13.

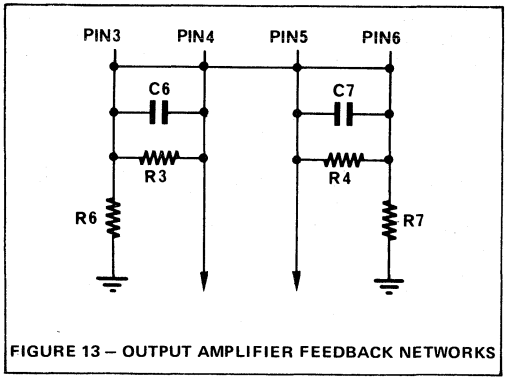


FIGURE 13 – OUTPUT AMPLIFIER FEEDBACK NETWORKS

The resistors R_6, R_7 are added to correct the output quiescent voltages levels which are optimised for R_3 R_4 = 5.1 KΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

Gain (dB)	R_3, R_4	C_6, C_7		R_6, R_7
		50 µs	75 µs	
0	5.1KΩ	10nF	15nF	
3	6.8KΩ	6.8nF	10nF	47K ±10%
6	10K	4.7nF	6.8nF	27K ±10%

The maximum output level is 1 Vrms; consequently the max. input is limited to 1.4 V-pk-pk if the gain is set to 6 dB.

SEPARATION ADJUSTMENT – A separation adjustment may be added, as shown below, (Fig. 14), to compensate for the receiver's IF characteristics.

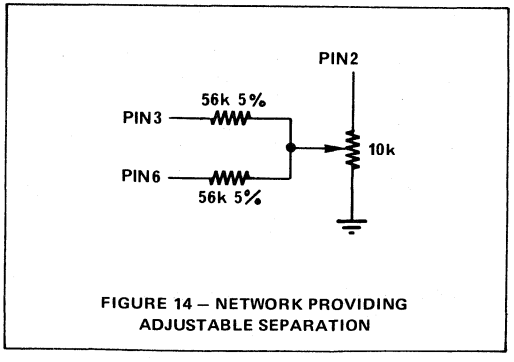


FIGURE 14 – NETWORK PROVIDING ADJUSTABLE SEPARATION

This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 KHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimised on one channel. Optimisation of both channels is possible if separate potentiometers are used to feed each output amplifier.

VARIABLE SEPARATION (BLEND) CONTROL AND 19 KHz OUTPUT – To retain the 16 pin package the blend control has been combined with the 19 KHz output on pin 11. The internal circuit providing this combination is shown below (Fig. 15).

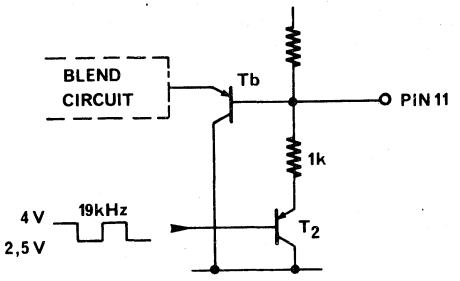


FIGURE 15 – BLEND CONTROL INPUT CIRCUIT

If pin 11 is left open-circuit the 19 KHz signal appears at a mean d.c. level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 KHz signal can be used to tune the internal oscillator.

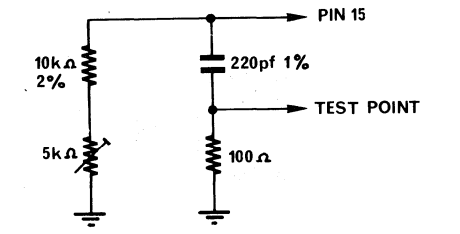


FIGURE 17 – OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT

To reduce the separation the voltage on pin 11 is reduced. At 3.2 V Ta ceases conduction and the 19 KHz signal disappears.
At 2.3 V the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 16.

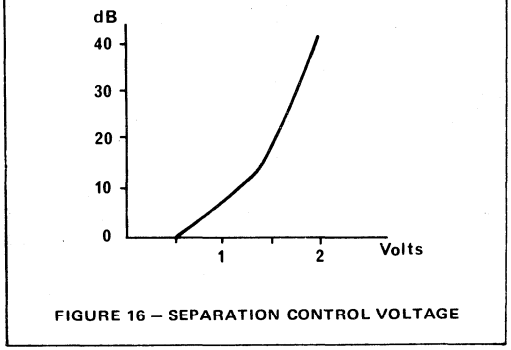


FIGURE 16 – SEPARATION CONTROL VOLTAGE

OSCILLATOR TUNING – If the variable separation facility is not required pin 11 is left open-circuit and the 19 KHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 KHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as below (Fig. 17).

The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 KHz.

HIGH LOOP GAIN COMPONENTS – For applications demanding operation under low pilot level (e.g. car radio) the following component changes to Fig. 1 are recommended.

R1 = 12K
R2 = 1.5K
R8 = 330
P1 = 10K
C3 = 150pF
C4 = 330nF
C5 = 150nF

TYPICAL CHARACTERISTICS

Unless otherwise noted V_{CC} = +12 V, T_A = +25 °C, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 17.)

———— : **High Loop Gain Circuit**

– – – – – – : **Normal Circuit**

FIGURE 2 – CHANNEL SEPARATION VERSUS COMPOSITE INPUT LEVEL

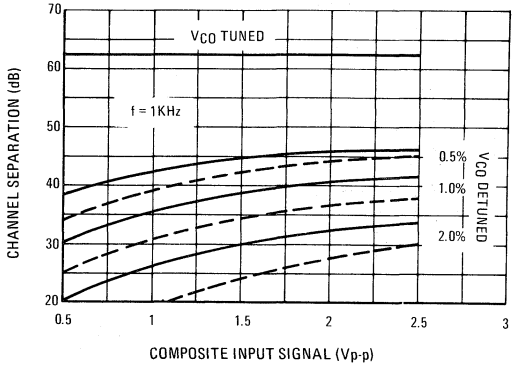


FIGURE 3 – V_{CO} FREE-RUNNING FREQUENCY VERSUS TEMPERATURE

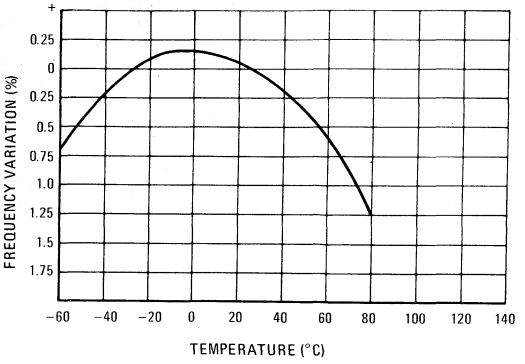


FIGURE 4 – STEREO SWITCH LEVEL VERSUS V_{CO} FREE RUNNING FREQUENCY

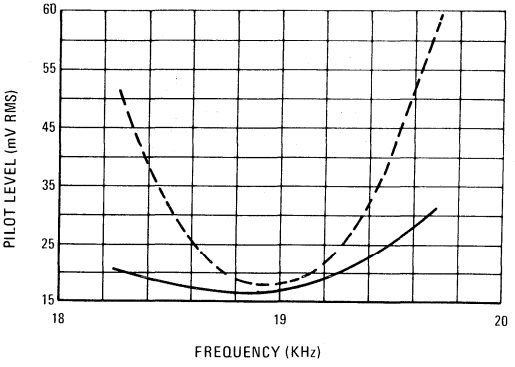


FIGURE 5 – SUPPLY RIPPLE REJECTION VERSUS SUPPLY VOLTAGE

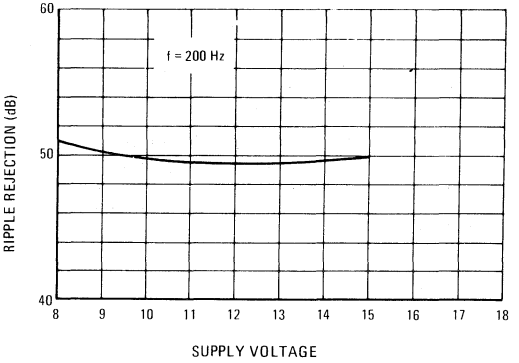


FIGURE 6 – T_{HD} VERSUS COMPOSITE INPUT LEVEL

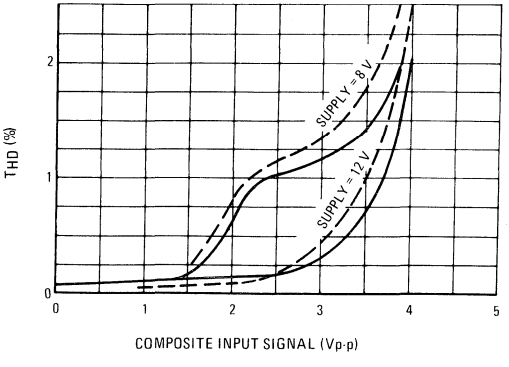


FIGURE 7 – CAPTURE AND HOLDING RANGE WITH 20 MV PILOT LEVEL

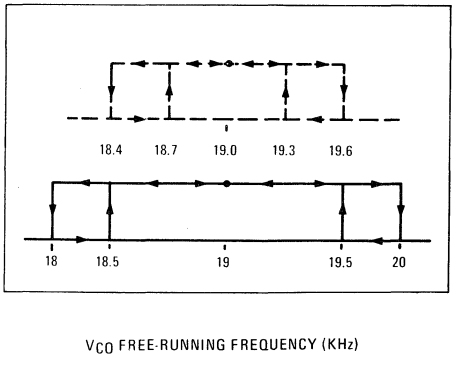


FIGURE 8 – BEAT NOTE DISTORTION VERSUS FREQUENCY

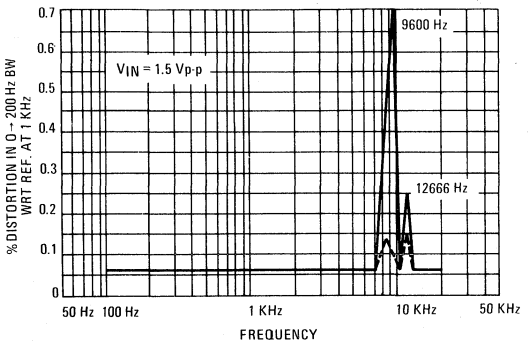


FIGURE 9 – CHANNEL SEPARATION VERSUS FREQUENCY

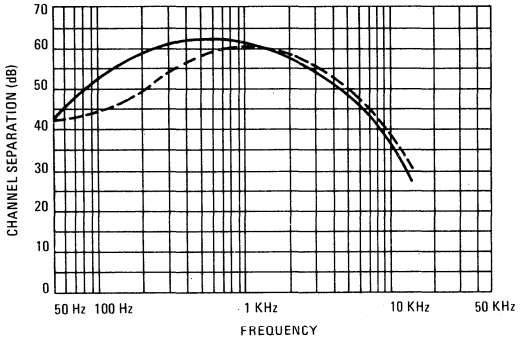
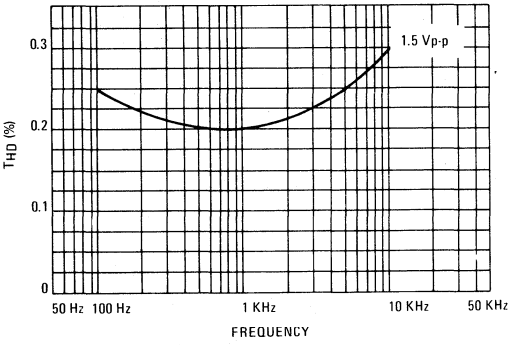


FIGURE 10 – T_{HD} VERSUS FREQUENCY



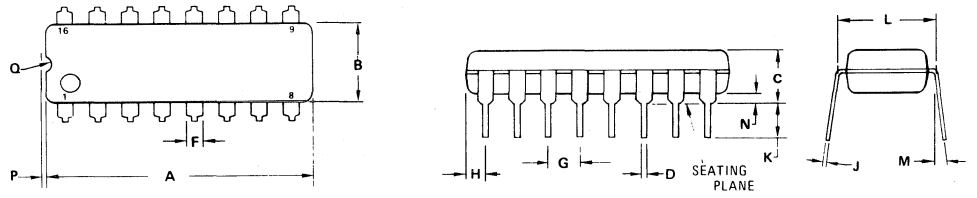
EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING – If required the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 KHz oscillator will be automatically killed.
The conditions governing Mono/Stereo switching on pin 9 are the following:
- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operation (with 100 mVrms pilot level): 10 μA (from pin 9 to ground)
  Hysteresis: 0.7 μA
- Stereo/mono switching & oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS –
P1 – 19 KHz frequency adjustment
P2 – channel separation adjustment and compensation for IF roll-off.
R3, R6 – gain fixing resistors. The values shown in the schematic are for unity gain.
C6, C7 – deemphasis capacitors. Value to give: RC = 50 μsec.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 V RMS.

OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 648



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

TDA1190Z

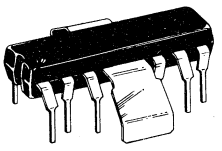
TV SOUND SYSTEM

The TDA1190Z 4.0 watt sound system is designed for television and related applications. Functions performed by this circuit include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.0 Watts Output Power
  (V_{CC} = 24 V, R_L = 16 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

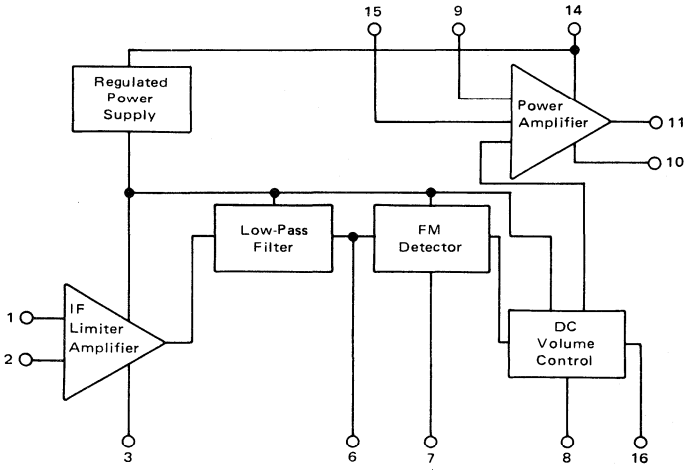
TV SOUND SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

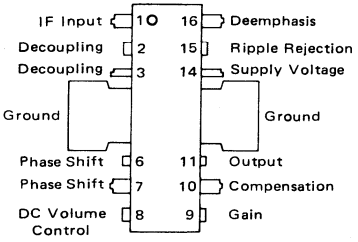


PLASTIC PACKAGE
CASE 722A

BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
TDA1190Z	0 to +75°C	Plastic

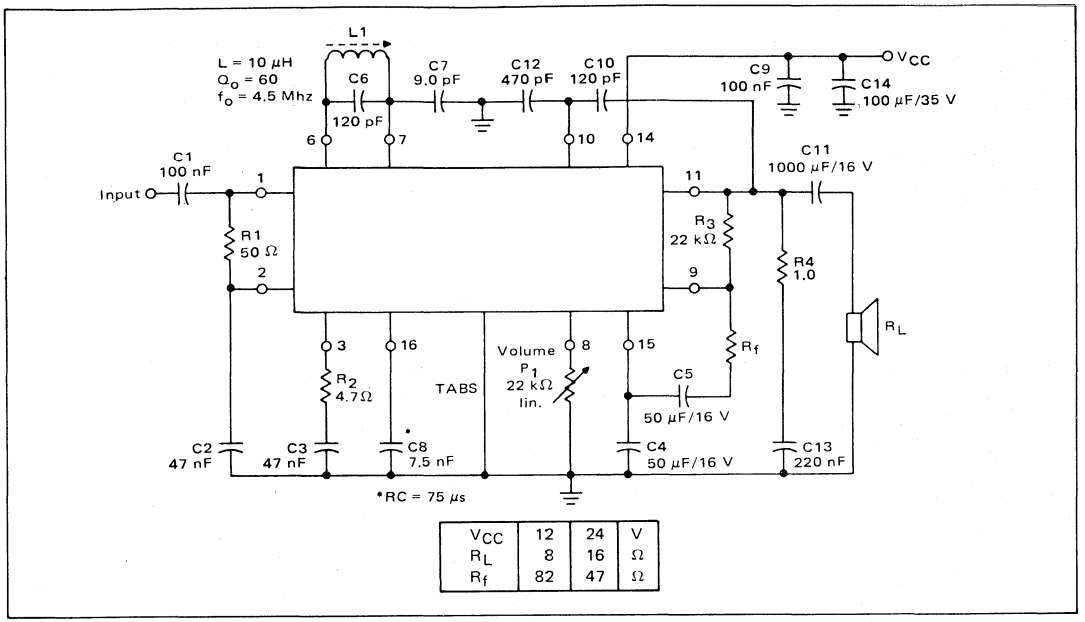
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	V
Input Signal Voltage	V_I	1.0	V
Output Peak Current (Non-repetitive) (Repetitive)	I_o	2.0 1.5	A
Operating Temperature Range	T_A	0 to +75	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C unless otherwise noted.)

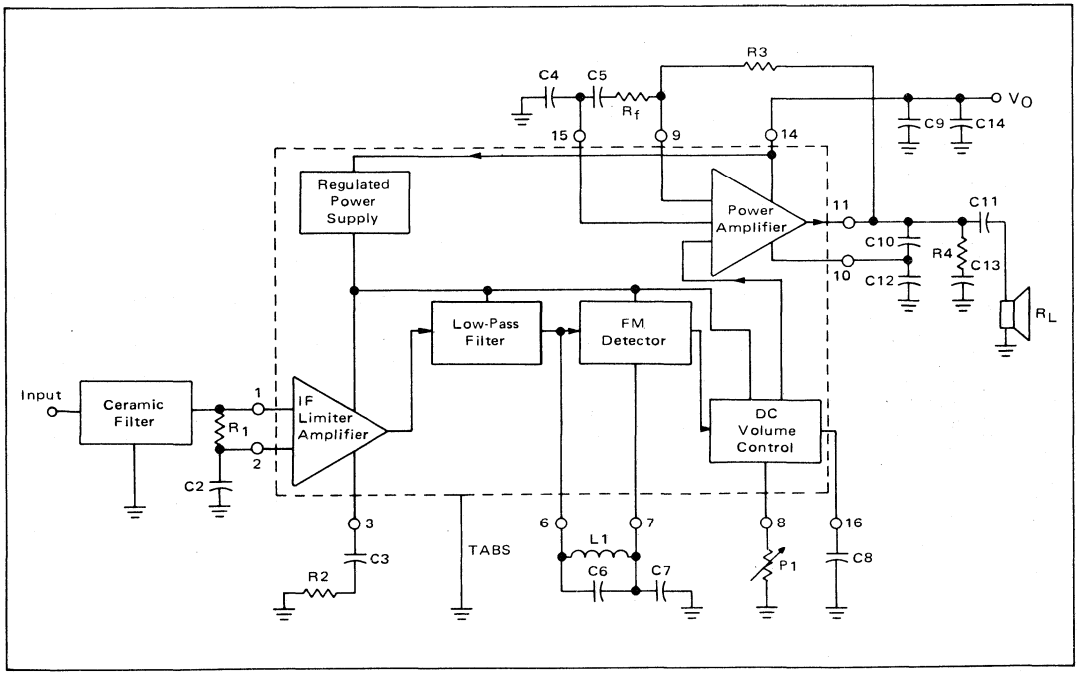
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Quiescent Output Voltage (pin 11) V_{CC} = 24 V V_{CC} = 12 V	V_O	 11 5.1	 12 6.0	 13 6.9	V
Quiescent Drain Current (P1 = 22 kΩ) V_{CC} = 24 V V_{CC} = 12 V	I_D	 11 –	 22 19	 35 –	mA
Output Power (d = 10%, f_m = 400 Hz) V_{CC} = 24 V, R_L = 16 Ω V_{CC} = 12 V, R_L = 8.0 Ω (d = 2%, f_m = 400 Hz) V_{CC} = 24 V, R_L = 16 Ω V_{CC} = 12 V, R_L = 8.0 Ω	P_O	 – – – –	 4.2 1.5 3.5 1.4	 – – – –	W
Input Limiting Threshold Voltage (-3.0 dB) at pin 1 Δf = ±7.5 kHz, f_m = 400 Hz, Set P1 for 2.0 Vrms on pin 11	V_I	–	40	100	μV
Distortion (P_O = 50 mW, f_m = 400 Hz, Δf = ±7.5 kHz) V_{CC} = 24 V, R_L = 16 Ω V_{CC} = 12 V, R_L = 8.0 Ω	d	 – –	 0.75 1.0	 – –	%
Frequency Response of Audio Amplifier (-3.0 dB) (R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ) R_f = 82 Ω R_f = 47 Ω	B	 – –	 70 to 12 k 70 to 7.0 k	 – –	Hz
Recovered Audio Voltage (pin 16) ($V_I \geq$ 1 mV, f_m = 400 Hz, Δf = ±7.5 kHz, P_1 = 0)	$V_{o'}$	–	120	–	mV
Amplitude Modulation Rejection ($V_I \geq$ 1.0 mV, f_m = 400 Hz, m = 30%)	AMR	–	55	–	dB
Signal and Noise to Noise Ratio ($V_I \geq$ 1.0 mV, V_o = 4.0 V, f_m = 400 Hz)	$\frac{S+N}{N}$	50	65	–	dB
Input Resistance (pin 1) (V_I = 1.0 mV)	r_i	–	30	–	kΩ
Input Capacitance (pin 1) (V_I = 1.0 mV)	C_i	–	5.0	–	pF
DC Volume Control Attenuation (P1 = 12 kΩ)	–	–	90	–	dB

TEST CIRCUIT

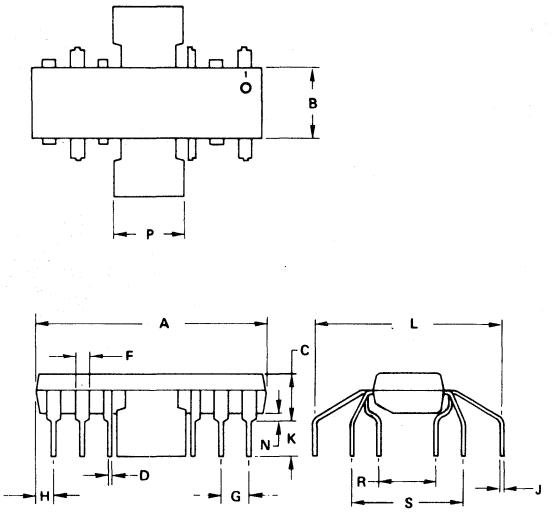


V_{CC}	12	24	V
R_L	8	16	Ω
R_f	82	47	Ω

TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS



PLASTIC PACKAGE
CASE 722A
$R_{\theta JA}$ = 60°C/W (Typ.)

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	2.92	3.43	0.115	0.135
L	16.94	17.45	0.667	0.687
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
R	4.83	5.33	0.190	0.210
S	9.91	10.41	0.390	0.410

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

TDA2002

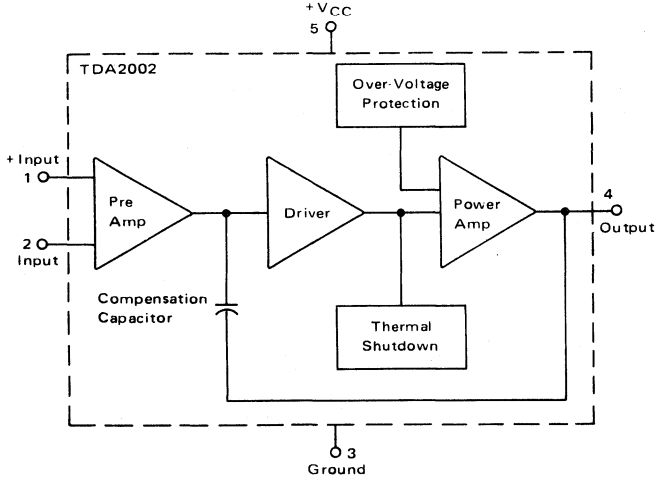
Advance Information

8 WATT AUDIO POWER AMPLIFIER

The TDA2002 is a class B audio power amplifier in a 5 lead plastic package for use in automotive radio applications. It provides an output power of 8 watts (typ) with R_L = 2 Ω and 5 watts (min) with R_L = 4 Ω at 14.4 volts.

- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Supply Over Voltage Protection
- Wide Supply Voltage Range (8 – 18 Volts)
- Low External Component Count

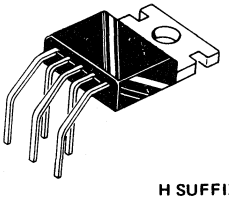
BLOCK DIAGRAM



8 WATT

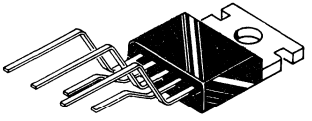
AUDIO POWER AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

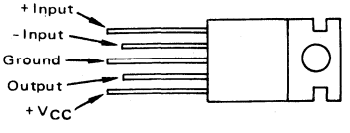


H SUFFIX
PLASTIC PACKAGE
CASE 314A

V SUFFIX
PLASTIC PACKAGE
CASE 314B



PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C)

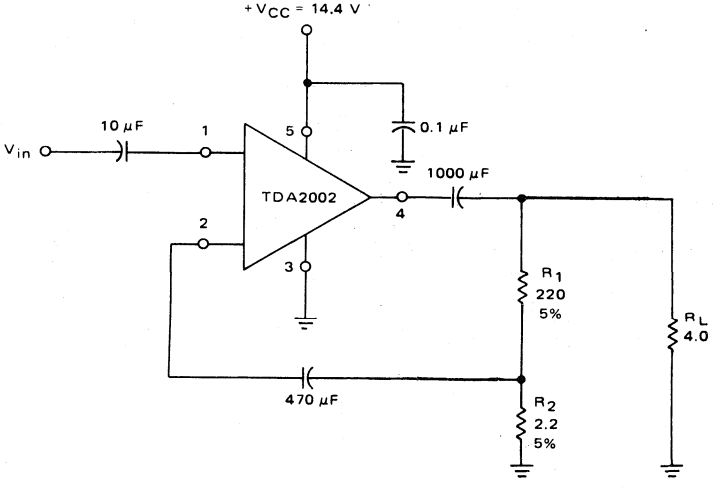
Rating	Value	Unit
Power Supply Voltage – Steady State Transients of 50 ms or less	28 40	V
Operating Power Supply Voltage	18	V
Peak Output Current (Non-Repetitive) (Repetitive)	4.5 3.5	A
Junction Temperature	150	°C
Storage Temperature	-65 to 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.4 Vdc, R_L = 4.0 Ω, f = 1.0 kHz, T_A = 25°C unless otherwise noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Drain Current (V_{in} = 0)	I_D	–	–	80	mA
Quiescent Output Voltage (V_{in} = 0)	V_O	6.4	7.2	8.0	V
Power Output – 10% Distortion (V_{CC} = 14.4 V, R_L = 4.0 Ω) (V_{CC} = 14.4 V, R_L = 2.0 Ω) (V_{CC} = 16 V, R_L = 4.0 Ω) (V_{CC} = 16 V, R_L = 2.0 Ω)	P_o	 4.8 7.0 – –	 5.2 8.0 6.5 10	 – – – –	W
Input Resistance (Pin 1)	r_i	70	150	–	kΩ
Equivalent Input Noise Voltage (R_S = 0, Bandpass = 20 Hz to 15 kHz)	e_n	–	4	–	μV
Equivalent Input Noise Current (R_S = 0, Bandpass = 20 Hz to 15 kHz)	i_n	–	0.1	–	nA
Power Supply Rejection Ratio (f_{ripple} = 100 Hz)	P_{SRR}	30	35	–	dB

*See Test Circuit – Figure 1.

FIGURE 1 – APPLICATION AND TEST CIRCUIT



TDA3950

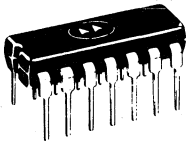
CHROMINANCE COMBINATION

A silicon integrated circuit for use in PAL Television receivers:

- Internal supply line stabilisation
- 30 dB ACC range
- ± 400 Hz min oscillator pull-in.
- Fast identification
- Only one adjustment necessary
- 2 V p-p reference output with high harmonic filtering
- Designed to be used in conjunction with the TBA396 & MC1327.

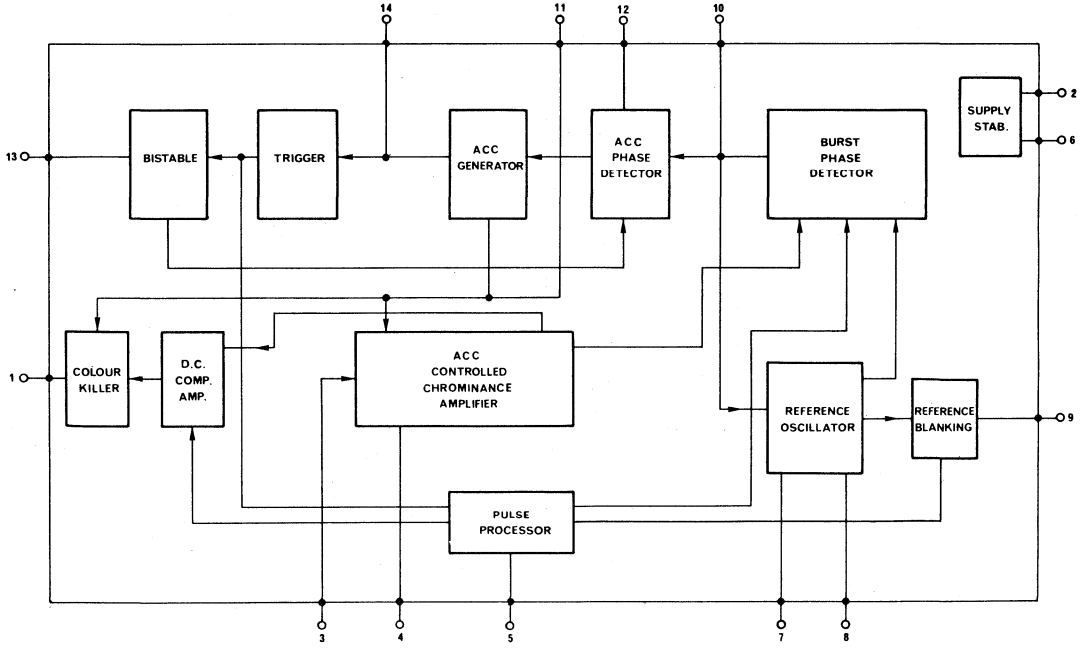
CHROMINANCE COMBINATION

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646 TO-116

FIGURE 1 – SYSTEM BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = +25 °C unless otherwise stated)

Rating	Pin	Value	Unit
Power Supply Current	2	60	mA
D.C. Current Capability of Reference Output	9	10	mA
Chrominance Input Voltage	3	8	V p-p
Operating Temperature Range		0 to + 70	°C
Power Dissipation (Package Limitation) Derate above T_A = + 25°C		625 5.0	mW mW/°C
Storage Temperature Range		− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C unless otherwise stated — See test circuit Fig. 3)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Voltage	2		8.7		Vdc
Chrominance Output Voltage	1	300	400	500	mV p-p
Colour Killer Operation: Kill Level (Burst) Unkill Level (Burst) Hysteresis	3	 6.5 9.0	 10 13 2.0	 17 20	 mV p-p dB
Maximum Chrominance Input Voltage	3	1			V p-p
Chrominance Output D.C. Current: Colour Killer Operating Colour Killer Off	1		 0 1.0		 mA
Change in Chrominance Output due to 20 dB change in Chrominance Input.	3, 1		2		dB
Chrominance Input Impedance	3		5.0		K Ω
Reference Output	9		2.2		V p-p
Reference Oscillator Pull-In Range		±400	±600		Hz
Phase Accuracy			2.5		°/100 Hz
Reference Oscillator Temperature Drift (no burst pulse applied)	9		−1.0		Hz/°C
Burst Gate Operating Voltage	5	2.0		8.0	V
Burst Gate Input Impedance	5		7.0		K Ω
H/2 Bistable Output	13		7.0		V p-p
Identification Time			1.0		msec

APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 must be decoupled closely to pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.

2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.

SETTING UP NOTES

Disconnect the burst gate pulses and adjust the P.L.L. potentiometer to give "Zero beat" from the sub-carrier reference oscillator. Reconnect the burst gate pulses.

FIGURE 2 – CIRCUIT SCHEMATIC

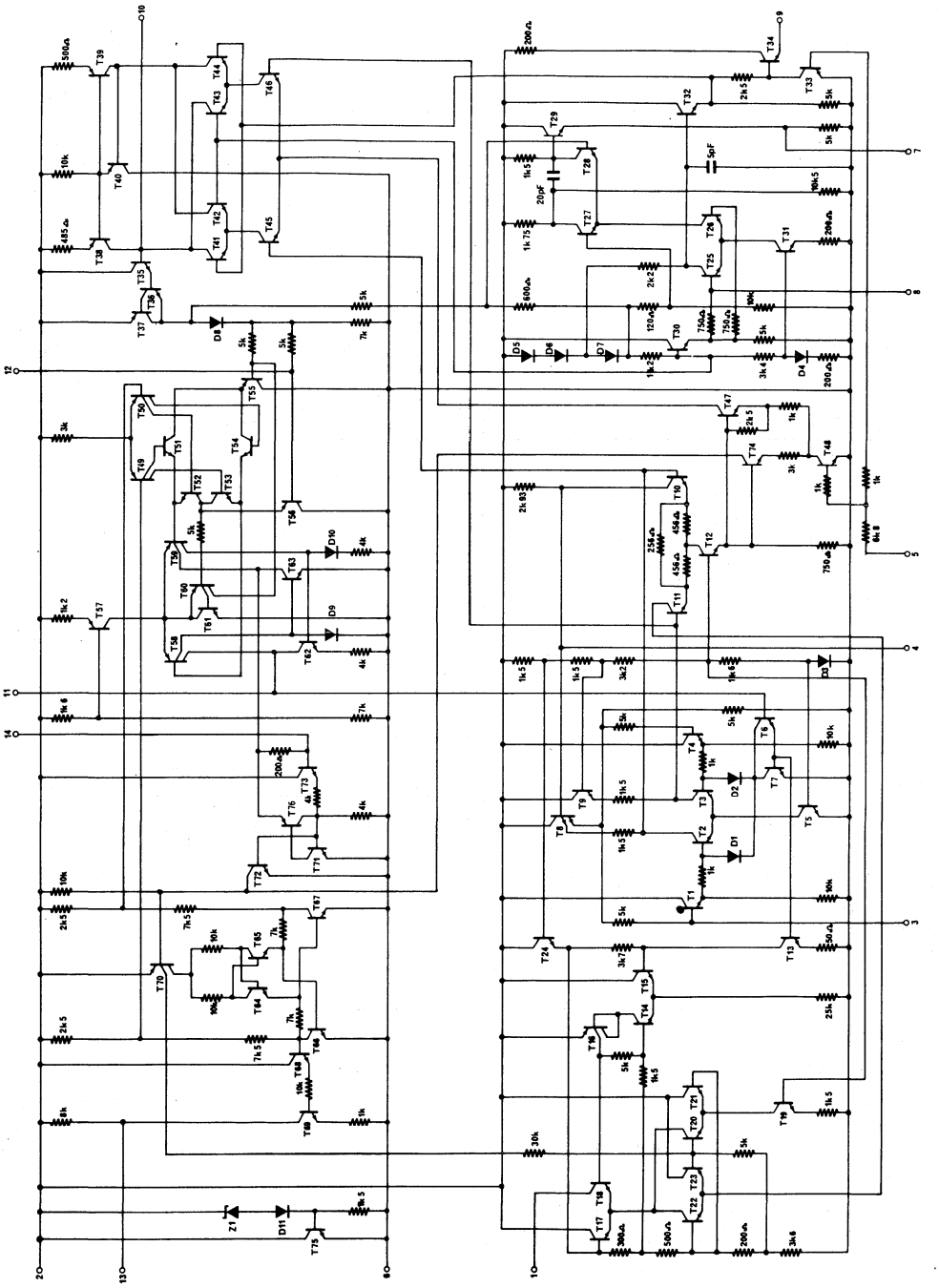
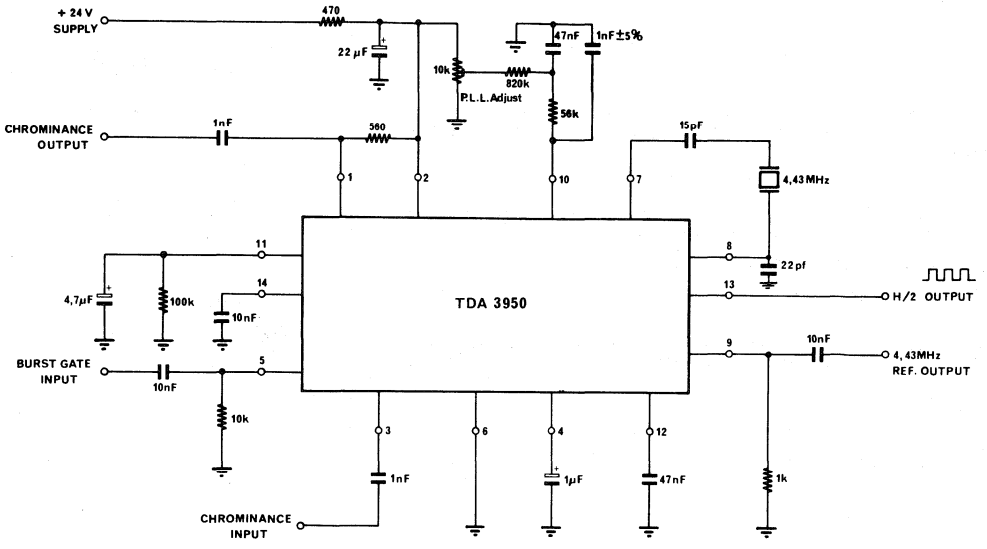
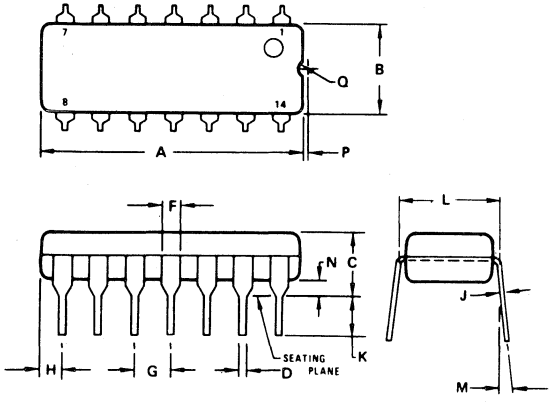


FIGURE 3 – TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

UAA1004-DP
UAA1004-CM

ZERO VOLTAGE SWITCH

Designed for use in high volume AC power switching applications with output drive capable of triggering SCR's or triacs. Other operational features include:

- Direct AC line or DC operation.
- A zero voltage crossing detector that synchronises the SCR or the triac at the zero crossing of the AC line voltage.
- High impedance input differential amplifier.
- Built-in hysteresis which avoids a DC current component through the load.
- Fail safe: a high impedance differential amplifier which supervises the sensor and insures that the triac will never turn "on" due to sensor failure.
- High power, asymmetric gate trigger pulses for power saving with internal current limitation. (Negative pulses)
- Voltage regulator for the supply of the sensor or other external circuits.

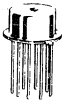
Typical Applications:

- heater control
- hot plate control
- photo control
- threshold detector
- valve control
- on-off power control
- relay driver
- lamp driver

ZERO VOLTAGE SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

DP SUFFIX
PLASTIC PACKAGE
CASE 626



CM SUFFIX
METAL PACKAGE
CASE 601
TO–99

PIN CONNECTIONS

1. INVERTING INPUT (INPUT AMP.)
2. NON INVERTING INPUT (FAIL SAFE)
3. AUXILIARY VOLTAGE (—)
4. + V_{CC} (GROUND)
5. AC LINE
6. OUTPUT
7. — V_{CC}
8. NON INVERTING INPUT (INPUT AMP.)

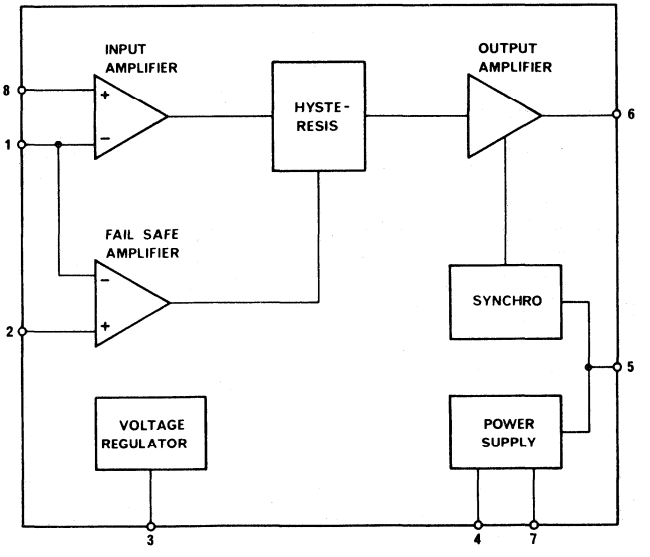


FIGURE 1 - BLOCK DIAGRAM

MAXIMUM RATINGS

Rating	Symbol	UAA1004-DP	UAA1004-CM	Unit
External DC Power Supply	V_{CC} (4-7)	20		Vdc
AC Peak Supply Current (sine wave, 50-60 Hz)	I_{AC} (5-4)	55		mA
Differential Input Voltage	V_{in} (1-8)	± 6		Vdc
	V_{in} (1-2)	± 6		Vdc
Power Dissipation T_A = 25°C	P_D	625	680	mW
Derate above 25°C	$1/\theta_{JA}$	5.0	4.6	mW/°C
Operating Temperature Range	T_A	— 20 to + 75	— 55 to + 125	°C
Storage Temperature Range	T_{stg}	— 55 to + 125	— 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (T_A = + 25°C Unless Otherwise Stated)

Characteristics		Symbol	Fig./Note	Min	Typ	Max	Unit
Input Differential Amplifier	Input Common Mode	CMV_{in}		— 1		— V_{CC} + 2	V
	Input Bias Current	I_{bin}	Note 1			1	μA
	Input Offset Voltage	V_{oin}	Fig. 5	— 10		+ 10	mV
Schmitt-Trigger	Hysteresis	V_{Hin}		+ 10		+ 20	mV
Fail Safe Amplifier	Input Common Mode	CMV_{fs}		— 1		— V_{CC} + 2	V
	Input Bias Current	I_{bin}	Note 1			1	μA
	Input Offset Voltage	V_{ofs}	Note 2	— 20		+ 20	mV
Synchronization	Pulse Duration	t_{LII}	Fig. 3 + 4	100			μs
		t_{LIII}		75			μs
		t_H			20		μs
Output Amplifier	Current Sink	I_{out}	Note 4	80			mA
Voltage Regulator	Auxiliary Voltage	V_{Aux}			— 7.7		V
		TC_{Aux}			— 0.7		mV/°C
	Output Impedance	$Z_{o\ Aux}$			10		Ω
	Load Current Range	I_{Aux}	Fig. 3	0.2		3	mA
Main Supply	AC Operation	V_{CC}	Fig. 3/Note 3		— 14		V
	DC Operation	V_{CC}		— 11			V
		I_{CC}	Note 5		1.9		mA

NOTES

1. As the input amplifier has a common pin with the fail safe amplifier, the input bias current of each amplifier is defined as:
$$I_{bin} = \frac{1}{4}(I_{b8} + I_{b1} + I_{b2})$$
2. This characteristic can be measured as in Fig. 5. The function generator must be connected between pins 1 & 2 and the input amplifier must be biased with pin 8 positive and pin 1 negative.
3. Measured with I_{Aux} = 0
4. Measured at V_{CC} = 14 V
5. Measured with I_{out} = 0 and I_{Aux} = 0

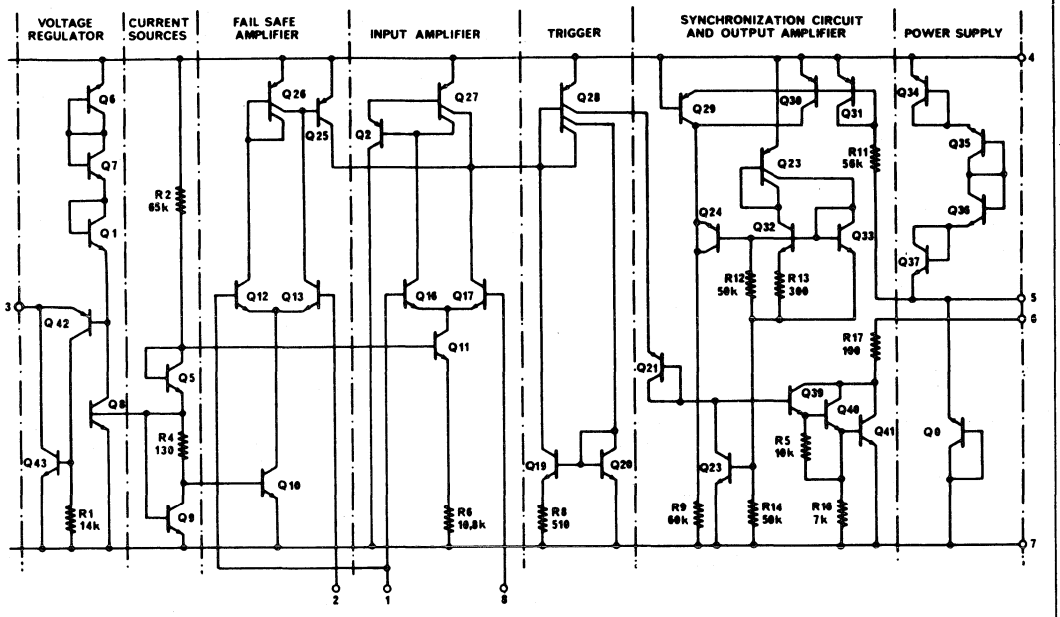


FIGURE 2 - CIRCUIT SCHEMATIC

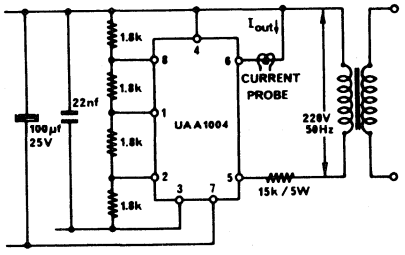


FIGURE 3 - BASIC TEST CONFIGURATION

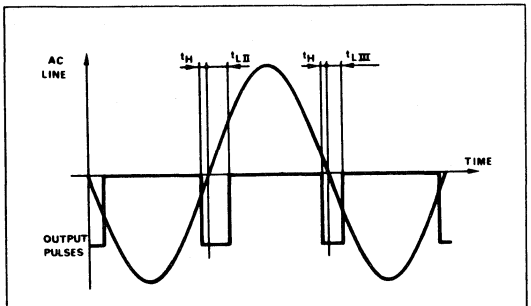
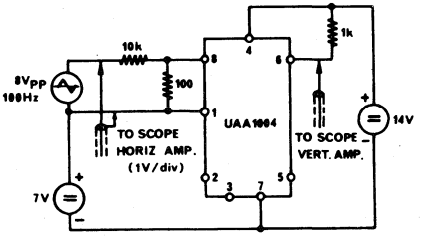


FIGURE 4 - ASYMMETRIC PULSES DEFINITION



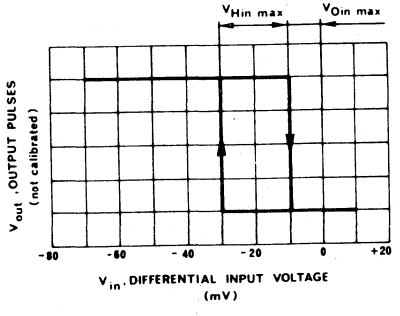


FIGURE 5 - OFFSET VOLTAGE AND HYSTERESIS MEASUREMENT

TYPICAL APPLICATIONS

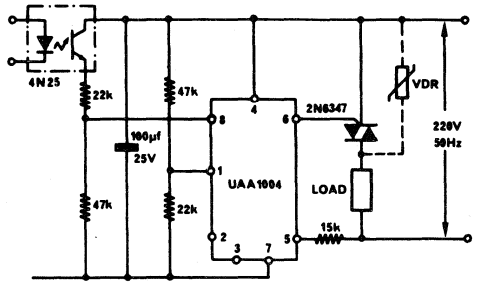


FIGURE 6 - ISOLATED STATIC SWITCH

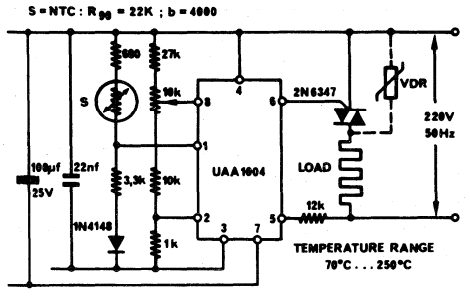


FIGURE 7 - FLAT IRON TEMPERATURE CONTROL

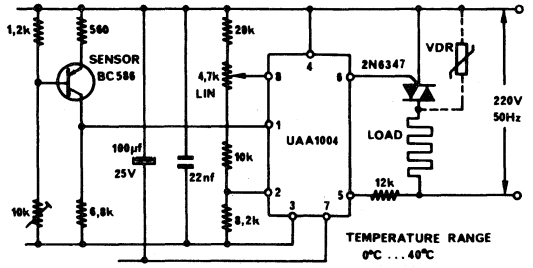
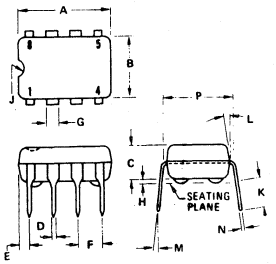


FIGURE 8 - PANEL HEATER TEMPERATURE CONTROL

NOTE: In applications of Fig. 7 & 8, noise on the input amplifier (pins 8 & 1) must be kept below the minimum hysteresis specified. Care must be then taken in the layout of the PC board and in the wiring, or if necessary, put a RC filter at this input.

OUTLINE DIMENSIONS

DP SUFFIX
PLASTIC PACKAGE
CASE 626

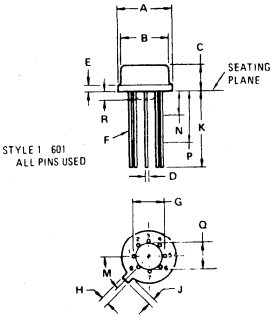


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.39	9.90	.370	.390
B	6.09	6.35	.240	.250
C	3.43	3.94	.135	.155
D	.381	.483	.015	.019
E	–	1.14	–	.045
F	2.54 TP		0.100 TP	
G	.762	1.52	.030	.060
H	508 NOM		.020 NOM	
J	.762	1.02R	.030	.040R
K	2.92	3.43	.115	.135
L	7° TYP		7° TYP	
M	0°	10°	0°	10°
N	.203	.279	.008	.011
P	7.37	7.87	.290	.310

NOTES:
1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL.
2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED

Weight ≈0.446 gram

CM SUFFIX
METAL PACKAGE
CASE 601
TO–99



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.510	9.390	0.335	0.370
B	7.750	8.500	0.305	0.335
C	4.200	4.690	0.165	0.185
D	4.070	0.533	0.016	0.021
E	–	1.020	–	0.040
F	0.406	0.482	0.016	0.019
G	5.080 TP		0.200 TP	
H	0.712	0.864	0.028	0.034
J	0.737	1.140	0.029	0.045
K	12.700	–	0.500	–
M	45° TYP		45° TYP	
N	–	1.270	–	0.050
P	6.350	12.700	0.250	0.500
Q	3.560	4.060	0.140	0.160
R	0.254	1.010	0.010	0.040

Weight ≈0.920 gram

UAA1008A

Advance Information

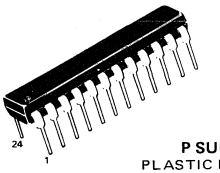
TUNING SYSTEM LINEAR PROCESSOR CIRCUIT

The UAA1008A provides the interfacing between the digital section of the tuning memory system and the TV set. In addition, it supplies the necessary functions and stabilized voltages for operating the complete system.
When used in conjunction with the MC14425/29 and MC14426 it will perform the following:

- D/A conversion of varicap voltage
- 34 Volt regulation
- 5 volt regulation for supply of all V_{DD} external lines
- Supply voltage supervisory control
- Band decoding and driver (35 mA)
- TV station capture control with help of fly-back, video, and AFC signals.

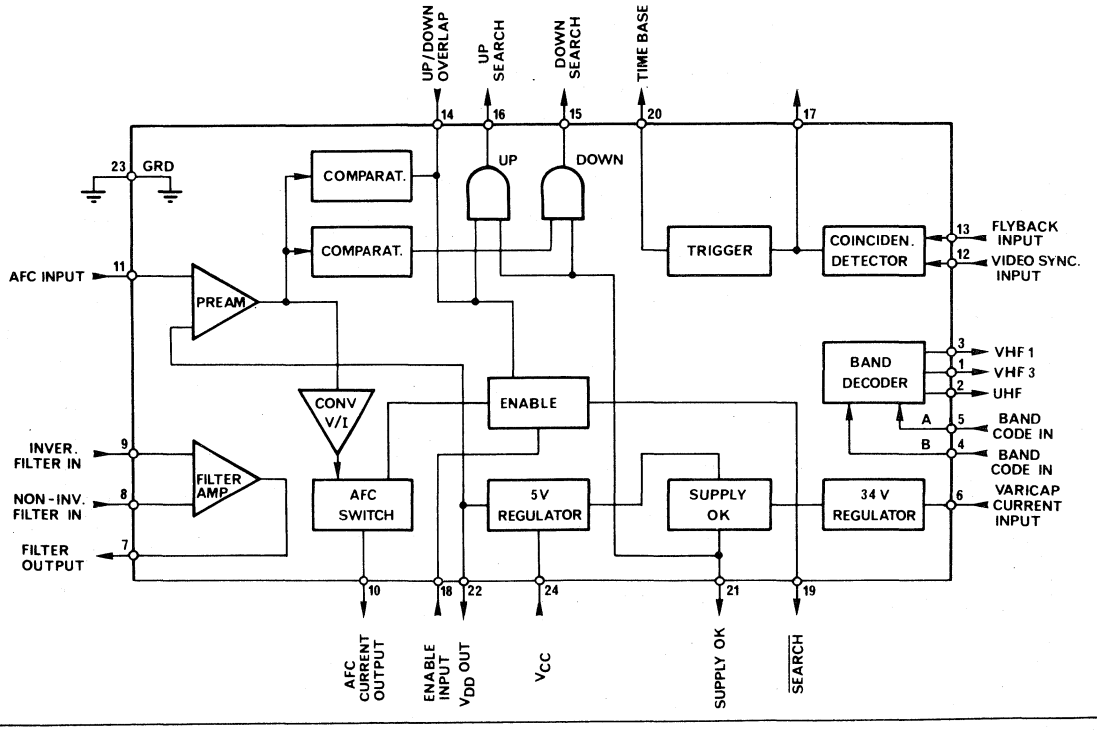
TUNING MEMORY SYSTEM LINEAR PROCESSOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724

FIGURE 1 – UAA1008A BLOCK DIAGRAM AND PINOUT



MAXIMUM RATINGS (T_A = 25 °C unless otherwise stated)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	Vdc
Varicap Supply Current	I_{VV}	10	mA
Continuous Band Switch Output Current[1]	I_b	35	mA
Filter/Amplifier Output Current	I_{fout}	+0.4 to −1	mA
Band Switch Output Voltage	V_b	V_{CC} to −2	Vdc
Output Current (pins 15, 16, 19, 20, 21)	I_o	1	mA
Pin 19 Output Voltage	V_o	18	Vdc
Pin 22 Output Current	I_{DD}	15	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

[1] Upon request devices allowing a Max. Capacitive Load of 22 µF on band switch outputs can be supplied.

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

Characteristic	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Operating Voltage	24	V_{CC}		12		18	Vdc
Power Supply Current (@ V_{CC} = 18 V)	24	I_{CC}	Band driver current = 0			21	mAdc
Varicap Voltage Supply	6	V_{VV}	I_{VV} = 2 mA	33.5		40.5	Vdc
Stabilized Voltage Output	22	V_{DD}	I_{DD} = 10 mA max.	4.95	5.2	5.45	Vdc
Input Signals:							
– Negative video modulation positive sync. pulses	(12)	V_{vid}	See typ. application		2		V P/P
– Positive flyback signal	(13)	V_{fly}	See typ. application		60		V P/P
– Video carrier discriminator negative going for Δf positive (Referenced to V_{DD})	11	V_{afc}			±250		mV
Time Base Output Voltage	20	V_{OH}	I_{OH} = 20 µA I_{OL} = 500 µA	4		1	V
Supply OK	21	V_{OH} V_{OL}	I_{OH} = 500 µA I_{OL} = 10 µA	4		1	V
UP / DOWN Output Voltage	15, 16	V_{OH} V_{OL}	I_{OH} = 20 µA I_{OL} = 500 µA	4		1	V
AFC Signal Processor							
– Gm (I_{10} /V_{11})	10	I_{afc}		0.9	1.2	1.37	mmhos
– Maximum AFC current	10			±123	±200	±305	µA
– Comparator threshold			See Fig. 2		±50		mV

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Contd.

Characteristics	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Varicap Filter & Amplifier:							
– Input bias current	8, 9					0.7	μA
– Offset voltage	8, 9			−20		+20	mVdc
– Output voltage swing	7	V_{OL} V_{OH}				0.5	V
– Open loop voltage gain				31	60		V dB
Band Switch Output:							
– Output current	1, 2, 3	I_{OH}	$V_{OH} = V_{CC} - 1.6$ V			35	mA
– Leakage current (open collector)	1, 2, 3	I_{OL}	$V_{OL} = -2$ V			1	μA
Binary Coded Band Input Voltage	4, 5	V_{IH} V_{IL}	I_{IH} = 300 μA I_{IL} = 300 μA	V_{DD} −0.55		0.55	V
Enable Input Voltage	18	V_{IH} V_{IL} tristate	I_{IH} = 300 μA I_{IL} = 300 μA	V_{DD} −0.55 2		0.55 3.15	V
Search Output	19	V_{OH} V_{OL}	Open collector I_{IL} = 500 μA			0.5	V

TUNING MEMORY SYSTEM ENABLE FUNCTIONAL TABLE

MODE	ENABLE IN	LINEAR AFC	MEMORY UPDATE	TIME BASE	UP/DOWN OVERLAP	SEARCH
Memory	L	ON	YES	X	NO	H
Memory	Tristate	OFF	NO	X	NO	H
Search	H	OFF	YES	X	YES	L
Verification	L	ON	YES	X	NO	L

X : don't care

FIGURE 2 – AFC TRANSFER FUNCTION

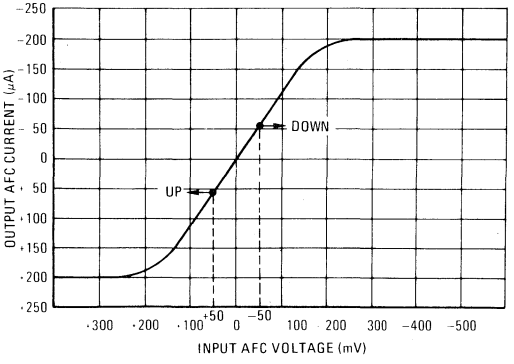
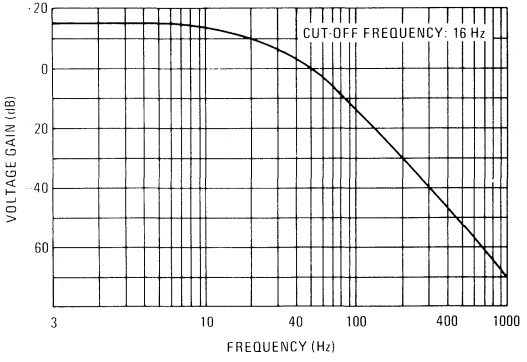


FIGURE 3 – FILTER/AMP FREQUENCY RESPONSE



INPUT/OUTPUT FUNCTIONS

AFC INPUT & OUTPUT – The AFC input (pin 11) generates UP & DOWN commands whenever the input level varies by more than V_{DD} ±50 mV.
At the same time the AFC voltage is converted into a proportional AFC output current (pin 10) limited to an excursion of ±200 μA (see Fig. 2). The AFC output current source is gated by the Enable input function (pin 18). See enable functional table.

UP & DOWN – The UP output (pin 16) changes to high whenever the AFC input (pin 11) is higher than V_{DD} + 50 mV, the DOWN output (pin 15) when lower than V_{DD} −50 mV.
For pin 11 voltage included between V_{DD} −50 mV and V_{DD} +50 mV no UP or DOWN commands will be generated. By means of an RC time constant on pin 14 it is possible to delay the falling edge of the UP command to make it overlap with the DOWN command provided that ENABLE IN (pin 18) is high.
Should it be necessary to defeat the UP and/or DOWN commands, the correspondent pin 16 and 15 can be grounded.

FILTER & AMPLIFIER – (Inverting input: pin 9; non-inverting input: pin 8; output: pin 7.) This operational amplifier provides the integration of the MC14425/9 binary rate multiplier output and the amplification of the same (usually around 6.5 times) to cover the required varicap tuning voltage range, according to the typical configuration of Fig 4.
Under these conditions only the critical components R_1 and R_2 are used to determine the voltage gain of the integrator. It is recommended to use good stability resistors with tracking temperature coefficient. (See Fig. 3 and 4.)

BAND DRIVER – Fully decoded outputs for tuner band switching are provided at outputs VHF 1 (pin 3), VHF III (pin 1), UHF (pin 2) according to the following logic table. See also MC14425/9 data sheet.

Input Code		Decoded Output		
Pin 4	Pin 5	Pin 3	Pin 1	Pin 2
0	0	X	X	H
1	0	X	H	X
0	1	H	X	X
1	1	X	X	X

NOTES:

[1] X state correspond to an open PNP collector.

[2] The control circuit supplying the coded band information can be looped-back to skip the following codes: (11) for three band only and (11) (10) for two band only.

FLYBACK – (pin 13.) This input is driven by the positive line flyback signal commonly available in TV sets. In conjunction with the SYNC signal controls TIME BASE output.
It is recommended to differentiate the flyback pulse to insure that coincidence between sync pulses and flyback occurs only when the picture is actually synchronised (see Fig. 4).

SYNC – (pin 12.) This input is driven by the video signal (negative modulation/positive going sync) through the sync separator network of Fig. 4.
Should separate positive sync pulses be available they can be used to drive pin 12 directly.

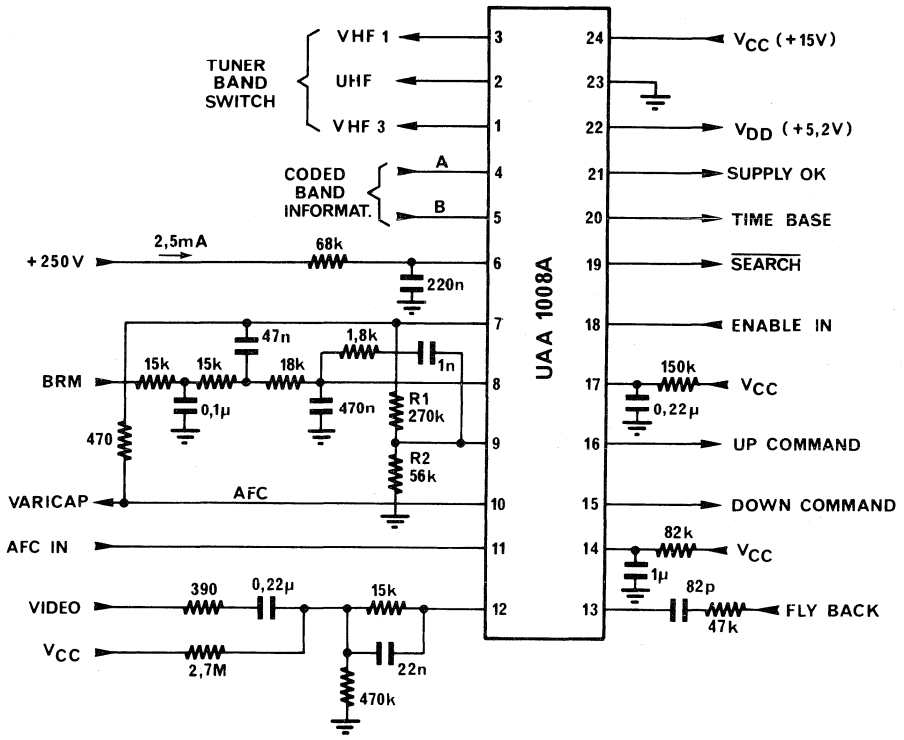
TIME BASE – (pin 20.) This output goes to high whenever coincidence is detected between flyback and sync signals, it is an indication of the presence of a valid TV signal.
It is possible to activate time base output also in absence of the above signals by grounding pin 17 via a 10K resistor.
Presence of Time Base is checked at the end of the verification time in the control circuit MC14425/9 to definetly activate the AFC output at pin 10.

SUPPLY OK – (pin 21.) Purpose of this function is to protect the memory contents in case of failure or discontinuity of any supply voltage.
Should the 34 V varicap supply fail or the power supply V_{CC} fall below 10 V, SUPPLY OK output, normally at V_{DD} (5.2 V) will immediately drop to zero volts.
This function is normally used to enable data cycling in the memory circuit MC14426 and the UP/DOWN counter in the control circuit MC14425/9.

ENABLE IN – (pin 18.) This function is provided by the control circuit MC14425/9 and is primarly used to turn off and on the AFC output in conjunction with TIME BASE, as shown in the enable functional table.
Enable-in goes high whenever a ramp is started and returns to low as soon as an UP/DOWN overlap is detected. It also insures that following an UP/DOWN overlap the UP delay is removed.

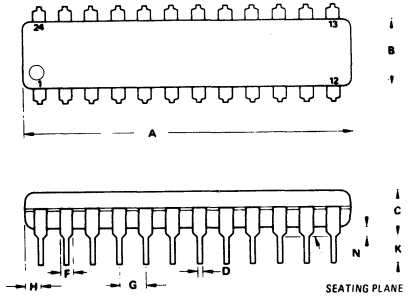
$\overline{\text{SEARCH}}$ – (pin 19) this output goes to low whenever the system is in the search mode and can be used to control external functions as necessary.

FIGURE 4 – TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 724



NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM. "D").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.260	1.286
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.35	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040

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